ISSUE: June 2020

How Application-Driven Performance And Reliability Requirements Shape Design and Qualification Of GaN Power Devices

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Transistors based on wide-bandgap semiconductors contribute to improved performance and efficiency in mainstream applications such as switched-mode power supplies (SMPSs) for telecom and computing, as well as compact adapters and wireless power chargers. Gallium nitride (GaN) devices, in particular, lend themselves to higher efficiency and power density achieved by high-frequency switching up to and beyond 1 MHz.

With the goal of serving applications at medium and low power levels, Infineon now provides 600-V and 400-V GaN devices, with near term plans to add 100-V and 200-V families to its portfolio. Similarly rated GaN devices are available from other semiconductor vendors. The structures of all these GaN devices and their operating mechanisms differ from those of the more familiar silicon (Si) power MOSFETs.

These differences account for the performance advantages of the GaN transistors, but also impose different gate-drive requirements and imply different failure mechanisms. And even among the GaN transistors themselves, there are different device designs, which vendors have adopted to enable normally off operation, which is the defacto standard for Si power MOSFETs.

This article describes how GaN power transistors (or power switches) differ in structure and performance from their Si counterparts, the different approaches to achieving normally off operation (cascode versus enhancement-mode design) and the two types of gate structures (Schottky or ohmic) used to design enhancement-mode GaN power transistors. The impact of these gate structures on gate-drive requirements is explained and different circuit options for driving the ohmic (or current driven) gates employed by Infineon's CoolGaN devices are discussed.

These devices, which are also referred to here as gate injection transistors, have undergone extensive testing to evaluate their reliability. The last part of this article, describes the tests conducted by Infineon to confirm the robustness of the gate structure and to qualify these new devices for in-field applications, particularly telecom power supplies which represent the most stringent requirements.

These tests include both those already employed to evaluate the reliability of silicon MOSFETs as well as the newer tests developed in the new wide-bandgap JEDEC standards to address the distinct failure modes of GaN devices. These GaN-specific failure modes are explained and the associated reliability test results obtained for Infineon parts are discussed.

Comparing GaN And Si Device Characteristics

A GaN high electron mobility transistor (HEMT) is a planar device with lateral current flow (Fig. 1). Compared to a silicon (Si) superjunction MOSFET, it has no reverse-recovery charge, which enables the bridgeless totem-pole PFC topology to reach ~99% efficiency. The Si MOSFET is not suitable for totem-pole PFC because of its body diode's relatively high Q_{rr} and low robustness.

GaN devices also exhibit a more linear output capacitance (C_{oss}) and consequently a much lower output charge (Q_{oss}). This shortens the required dead time in ZVS topologies such as resonant LLC and enables higher frequency and higher power density with less power loss than with Si. Other features such as ~7x lower gate charge and 20% lower R_{DS}-temperature coefficient than the most advanced superjunction MOSFETs improve energy efficiency and/or power density.

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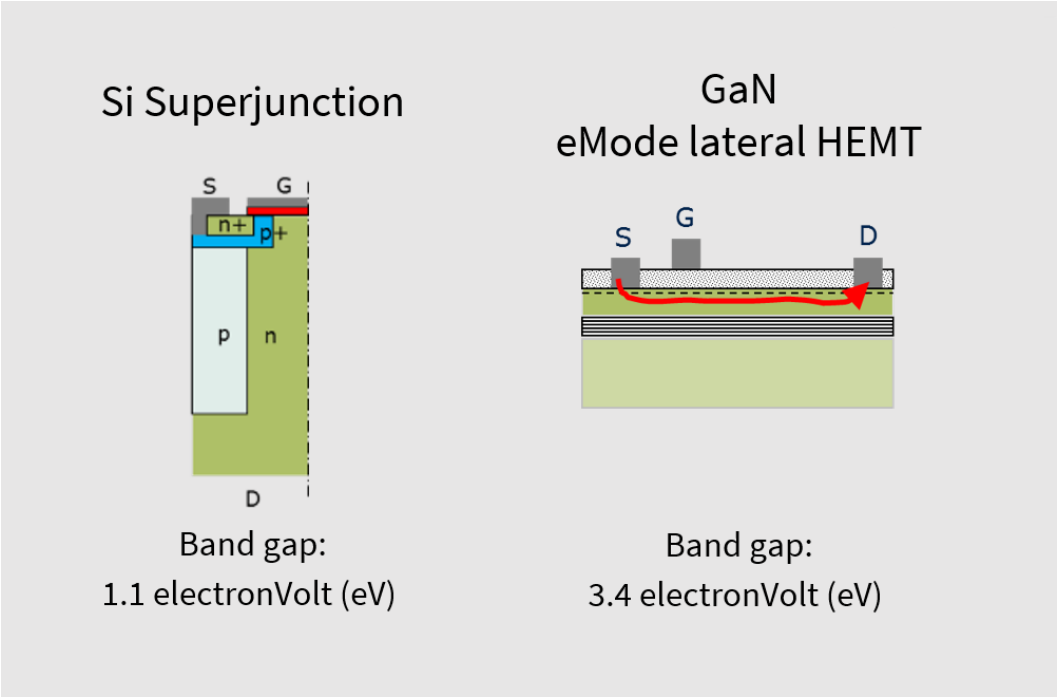

Fig. 1. Si superjunction MOSFET versus GaN HEMT. While current flows vertically in the superjunction MOSFET, it flows laterally in the GaN HEMT. Higher bandgap voltage, lack of reverse-recovery charge and lower output charge in the GaN HEMT contribute to its performance advantages as a power switch.

The conducting channel of a GaN HEMT is a highly-conductive two-dimensional gas (2DEG) formed at the AlGaN/GaN interface. There are no physical pn-junctions, so a GaN transistor can operate both as a power switch and in the reverse direction as a diode with zero reverse-recovery charge. Since the gas is formed with no applied external voltage, a GaN HEMT is normally on and negative voltage at the gate is required to achieve an off state. This has the potential to cause destructive behavior when power is not applied.

In order to implement a safe normally off device, two principal architectures are employed in today's commercially available GaN-on-Si power switches—enhancement mode (eMode) and cascode.

In an eMode device, control of the normally on state is achieved with particular features of the gate structure that vary between manufacturers, which we will explore in a moment.

Alternatively, in a cascode device, the GaN HEMT is paired with a low-voltage silicon MOSFET that is used to turn the HEMT on and off. This creates a two-chip solution with characteristics similar to a Si MOSFET, with some tradeoffs in several figures-of-merit (FOMs), in order to achieve simpler use with standard MOSFET gate drivers.

Manufacturers of eMode HEMTs have adopted one of two gate structures: either Schottky or ohmic (Fig. 2). A p-GaN HEMT with Schottky junction implemented with titanium nitride (TiN) is extremely sensitive to overvoltage. Schottky gate HEMTs need to be driven to 5 V to 6 V for full enhancement of the 2DEG, but must not exceed the max rating of 7 V to 10 V or else the device's lifetime will be shortened. Typically, external snubbers or clamp circuits are recommended to prevent overshoot voltage.

The ohmic alternative, also referred to as a hybrid drain-gate injection transistor (HD-GIT), uses titanium as the gate metal attached to a p-GaN doped layer, thus forming an ohmic contact with no insulating layer under the gate. As a result, the gate current is driven and self-clamped with no concern for gate overvoltage. This is the approach taken by Infineon in its normally-off eMode 600-V GaN devices (marketed under the CoolGaN name).

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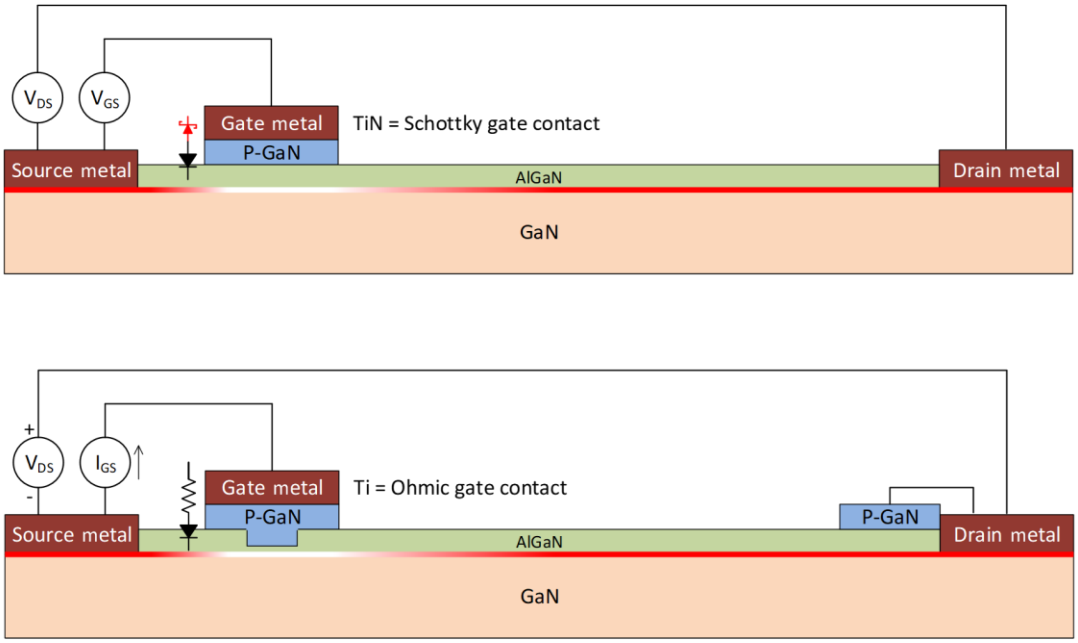

Fig. 2 A Schottky gate contact used by competitors (top) is voltage-driven. An ohmic gate contact used by Infineon (bottom) is current-driven, enabling it to self-protect.

Gate-Drive Requirements

The characteristics of the GIT gate structure (Fig. 3a) have significant impact on the driving method implemented for these devices. The gate ohmic contact with no insulating layer under the gate shifts the device's threshold voltage to a relatively low value at about 1.2 V. The gate also forms a p-n diode with a forward voltage of about 3 V (Fig. 3b). This is best driven by a current-source with an initially high peak current to rapidly charge the gate, followed by a steady-state current in the milliamp range to maintain the proper bias.

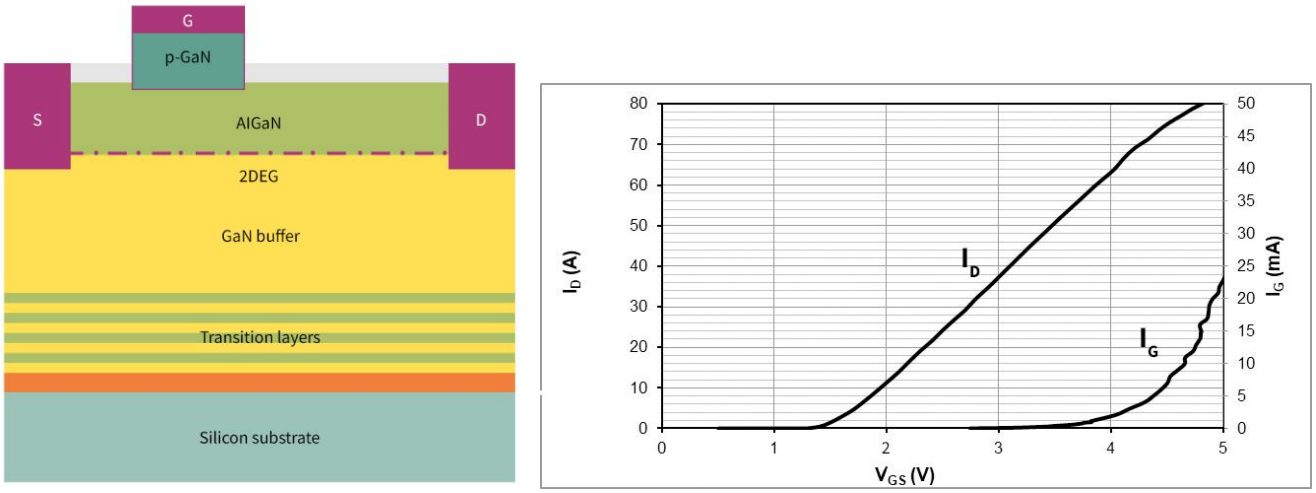

Fig. 3. Cross-section (a) and transfer characteristics (b) of p-GaN transistor.

The circuit depiction of a GaN switch (Fig. 4a) is similar to an ideal MOSFET with voltage-dependent capacitances C_{GS}, C_{GD} and C_{DS} and an internal gate resistor R_{int}. The main difference is the additional two diodes

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(in red) from gate-to-source and gate-to-drain. Although these diodes prevent the circuit from being driven like a conventional MOSFET, the switching process takes place as with a conventional MOSFET. The difference in driving the gate is that after reaching the Miller plateau, the gate node is clamped by the diode forward voltage V_F, and a small steady state (I_{ss}) is required to keep the device turned on (Fig. 4c).

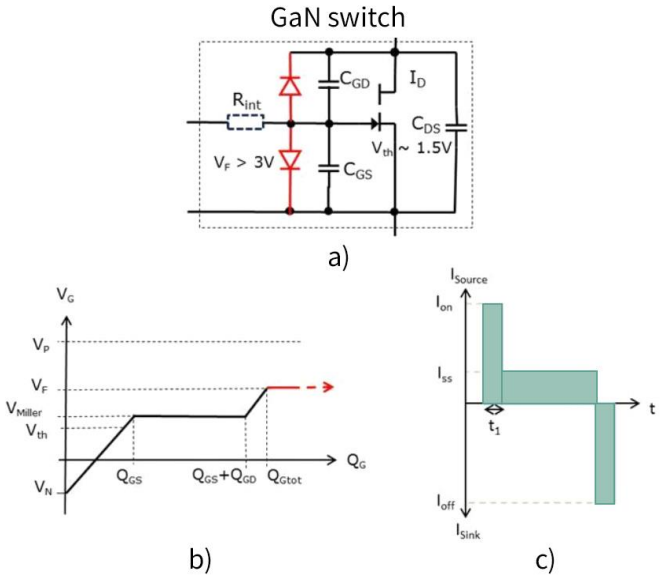

Fig. 4 E-mode GaN HEMT: equivalent circuit (a), gate-charge characteristic (b) and gate current (c).

By driving the gate with a current rather than a voltage, the conduction voltage drop (or $R_{DS(ON)}$) and the saturation current are dependent on the steady-state current (I_{ss}) according to the I/V characteristic curves in Fig. 5.

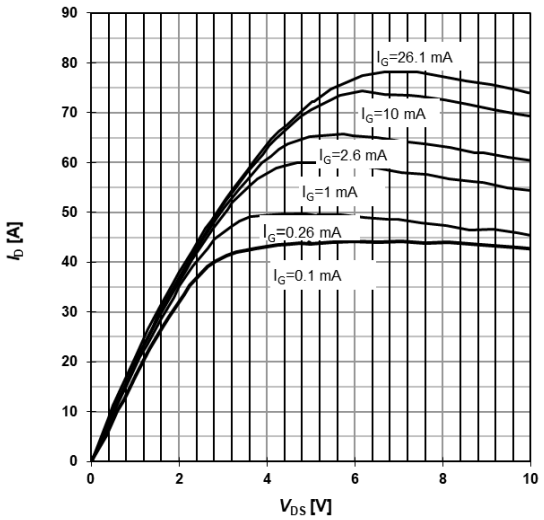

Fig. 5. Typical output characteristics for an E-mode GaN HEMT.

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To accommodate the gate-drive requirements of the eMode HEMT, the gate resistor (R_{on}) of the classic drive concept is replaced with an RC network that provides two parallel paths (Fig. 6). A small resistor R_{on} is coupled to the gate via a capacitance C_{on}, while a high resistor R_{ss} provides a direct path. The on-transient current I_{on} is defined by R_{on}, while R_{ss} determines the steady-state diode current.

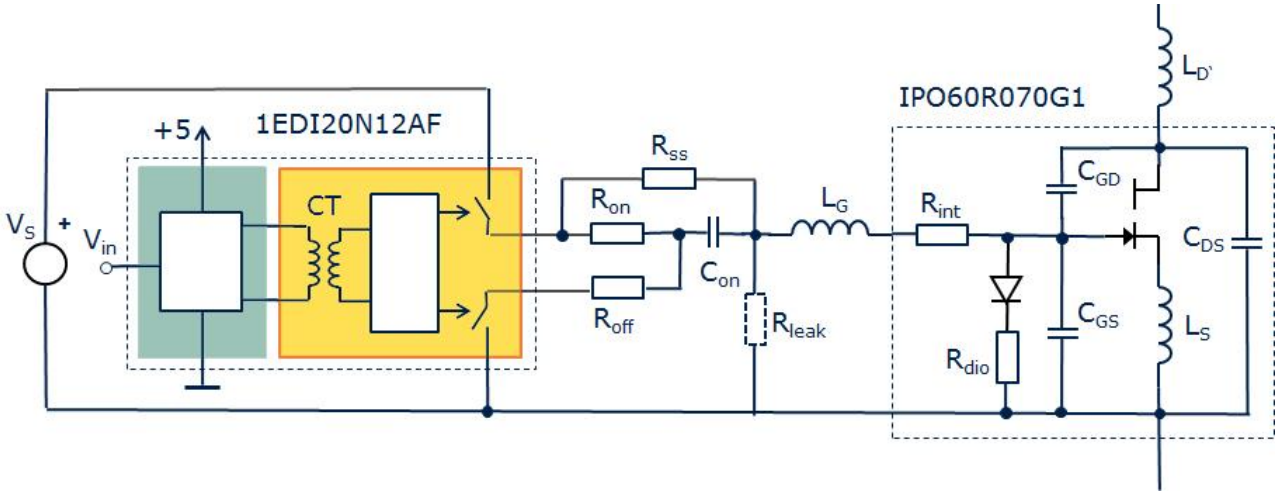

Fig. 6. 600-V CoolGaN driver scheme.

The 600-V CoolGaN driver scheme shown in Fig. 6 can use either a conventional gate driver (Fig. 7a) or a GaN-specific gate driver (Fig. 7b) that has added features to further improve performance.

Using the conventional gate drive (Fig. 7a), with a +9-V and -3-V supply and an RC network, will provide the proper drive levels to ensure full turn-on and off under all conditions. However, with the driver constantly biased to -3 V in the off-state, the reverse conduction behavior in the third quadrant will have an effective voltage of 3 V + 1.2 V = 4.2 V. This can lead to high power dissipation when reverse current is large. The dead time is also longer than necessary, which is often the case without adaptive dead-time management.

On the other hand, the GaN-specific gate driver (Fig. 7b) has a three-level output stage that drives the turn-off to the necessary negative voltage to prevent false turn-on. Then the gate voltage returns to zero to provide the best performance. This will minimize the third-quadrant voltage drop to only ~1.2 V during dead time, as shown in the key waveforms.

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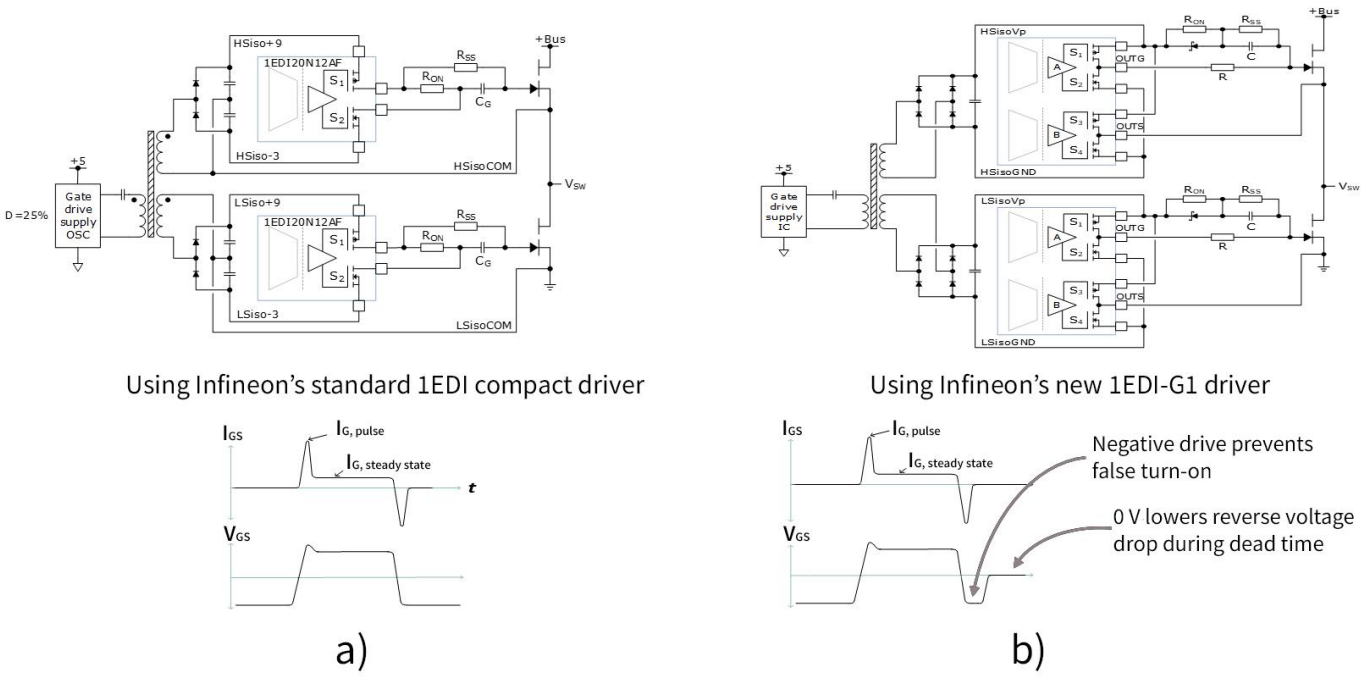

Fig. 7. Typical 600-V CoolGaN HEMT gate-drive circuits and gate I/V waveforms.

Evaluating Device Reliability

Infineon's evaluation of the robustness of the GIT gate structure design included high-temperature current testing, as well as both current and voltage dynamic stress testing. The results of a p-GaN gate module driven at constant (or steady state) 50 mA for 2000 hours (beyond the typical product qualification testing of 1000 hours) at 150°C on a 70-mΩ GaN product showed no drift in threshold voltage, gate diode forward voltage, reverse voltage drop and $R_{DS(ON)}$. Dynamic current and dynamic voltage stress testing of the gate structure over a 1000-hour period similarly showed negligible drift in specifications or device degradation.

Ruggedness testing of the GIT gate structure is an evaluation of potential intrinsic failure mode, and is just one part of the reliability and qualification process for GaN HEMT devices. Due to defects or process variability, extrinsic failure modes are also considered as part of reliability investigations in the initial development of devices. As a new device category, it is not surprising that GaN qualification testing has been expanded greatly by Infineon in comparison to testing of traditional silicon-based power semiconductors.

Evaluation and understanding of failure modes were key steps in the commercialization of GaN at Infineon. The next stage in device evaluation involved qualification for in-field applications of new devices.

Beginning with the established qualification protocols for silicon as defined by JEDEC and automotive-specific evaluations such as Q101, this expanded evaluation incorporated new assessment points that address specific differences between GaN and silicon devices, including those that arise due to the different device structure and operating physics. In addition, particular attention was paid to tests addressing the challenges of the intended applications and the expected lifetime.

The selected application profiles for qualification processes were biased to the most stressful operating conditions, such as the requirements for telecom ac-dc power converters. Telecom systems are expected to operate for long periods in highly dynamic field conditions, including broad variations in temperature and humidity, as well as demanding duty cycles. Satisfactory evaluation based on a typical profile (Table 1) created for a 600-V GaN HEMT device thus can apply to similar applications across a broad range of end systems.

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Table 1. High-level summary of an application profile for a telecom ac-dc power converter.

Telecom rectifier ac-dc socket	
Key device parameters, topology	2.5 kW, 230 V line, CM hard-switching
Expected lifetime	15 years
Operating lifetime	100%
Environmental conditions	
Relative humidity	85%
Profile of ambient temperature (in the box), % of operating time at each temperature	15% @-27.5°C 60% @15°C 25% @72.5°C
Profile of load conditions, % of operating time at each load condition	5% standby, no load 40% @ 10% to 30% load 50% @ 30% to 80% load 5% @ 80% to 100% load
Device electrical conditions	
Drain source voltage (V_{DS})	Average during off = 400 V Peak depends on I_{LOAD} (max = 460 V)
I_{GS+}	Average = 15 mA Peak= 625 mA for 50 ns
V_{GS}	Average = -3 V Peak= -10 V for 10 ns
I_D	Load current average 50% duty cycle
PWM frequency	65 kHz

There are four key points of evaluation for GaN devices that differ from their silicon equivalents: potential failure mode tests for dc bias failure, avalanche failure conditions, switching safe operating area (SOA) and dynamic on-state resistance.

For example, dc bias failure over lifetime in GaN HEMTs arises from different causes than those responsible for these failures in silicon-based devices. As such, tests to establish ruggedness are designed differently, with GaN tests seeking to measure time-dependent dielectric breakdown (TDDB) driven by voltage. Refer to the evaluation of time to failure for a 600-V e-mode HEMT under excessive voltage and temperature conditions in Fig. 8.

Another difference concerns avalanche failure resistance, which is significantly higher in GaN than in silicon (Fig. 9.) For GaN, the actual failure mode is a function both of thermal limits and TDDB (time-dependent dielectric breakdown).

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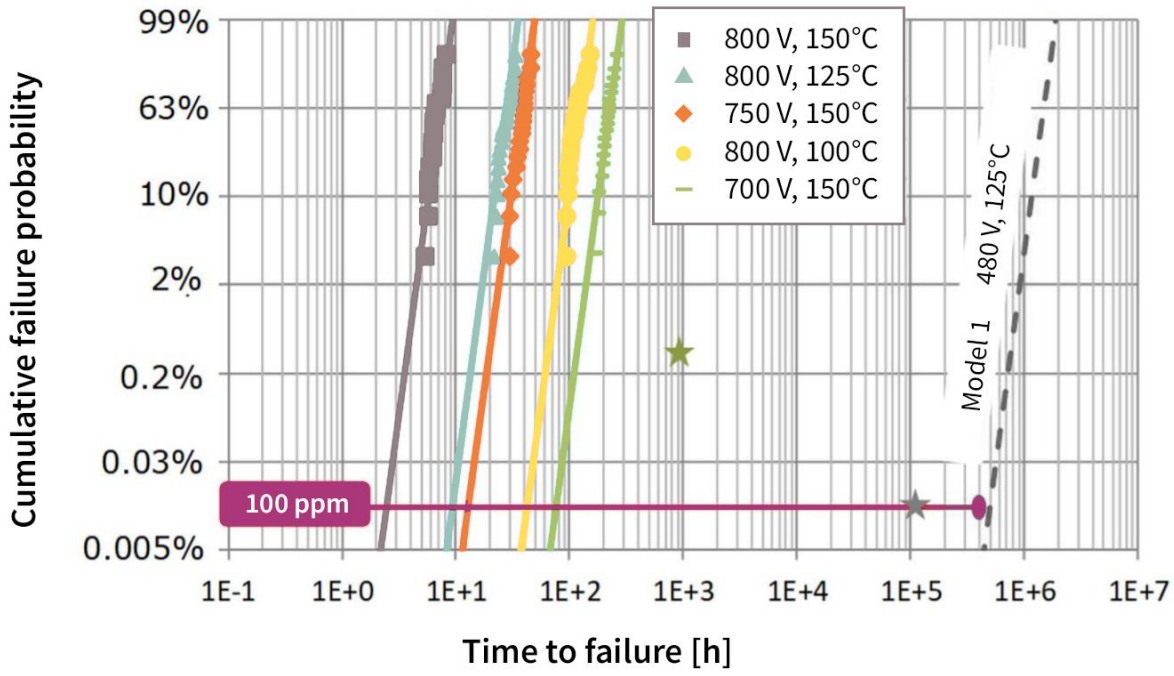

Fig. 8 Infineon's Weibull plot for dc bias time to failure for a matrix of voltage and temperature.

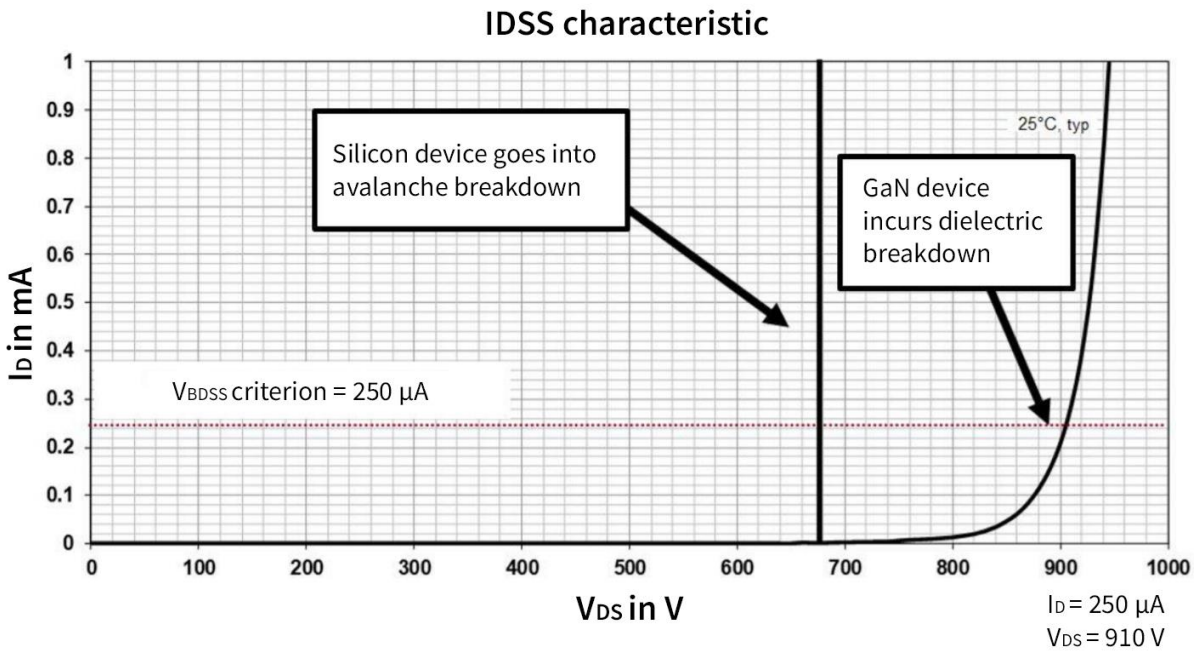

Fig. 9. Overlay of drain current versus drain voltage traces for a 600-V-rated GaN HEMT and a 650-V-rated silicon superjunction MOSFET.

Switching SOA, or dynamic high-temperature operating life, is a new degradation mechanism applicable to GaN devices. Infineon's tests have demonstrated stable device operation in hard switching applications from 1000 to 3000 hours (500 V dc link, 100 kHz). In compliance with JEDEC's JEP180 Guideline For Switching Reliability

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Evaluation Procedures For Gallium Nitride Power Conversion Devices,[1] accelerated testing at higher than designed voltage and current has been conducted by Infineon to extend the estimated lifetime far beyond these findings.

Dynamic on-state resistance is another potential failure mechanism that applies to GaN devices and not to silicon. This is because electron movement in the 2DEG transmissive layer can be transiently trapped by the solid layers between which it sits, causing a temporary increase in $R_{DS(ON)}$.

A plot of this effect (Fig. 10) compares an Infineon device to a competitor, evaluated under hard-switching conditions at 20 A in accordance with the first-ever wide-bandgap JEDEC publication, JEP173, Dynamic On-Resistance Test Method Guidelines For GaN HEMT Based Power Conversion Devices, Version 1.0.[2] Infineon is a key contributor and one of the proud sponsors for the development of JEP173.

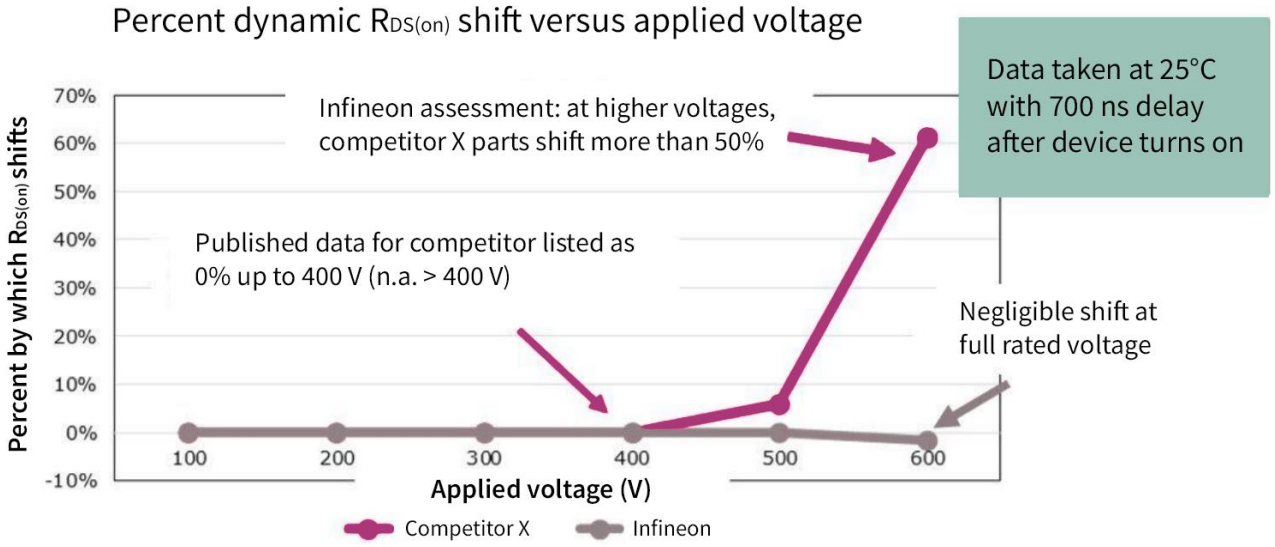

Fig. 10. Dynamic $R_{DS(on)}$ as a function of drain voltage for Infineon and competitor "X" device. Testing was done under hard-switching conditions at 20 A. Note that some suppliers publish data taken under soft-switching conditions, which is not as stressful on devices.

Application-Specific Qualification

Infineon qualification test suites for GaN devices today incorporate the nine basic JEDEC tests used for silicon devices and ten additional tests to ensure that potential failure mechanisms are managed and that design lifetime and failure rate requirements are met. The telecom rectifier application profile mentioned above considers various topologies for PFC (CCM totem pole) and dc-dc (LLC). Other applications where data has been collected include half-bridge-based flyback chargers/adapters (< 70 W); PV inverters; hard-switched motor control applications; soft-switched, high-frequency Class E wireless power; hard-switching Class D audio and phase-shifted full-bridge topology dc-dc converters.

The end goal of this effort is to ensure that engineers are provided with the knowledge required to successfully reap the energy efficiency, density and lower system cost benefits of GaN power devices. Knowing when the material properties and functional characteristics of these devices are best deployed versus alternative silicon-based devices is a first step for successful projects.

References

1. https://www.jedec.org/standards-documents/docs/jep180

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2. https://www.jedec.org/standards-documents/docs/jep173

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For more information on designing power converters with SiC & GaN semiconductors, see the How2Power Design Guide, locate the Popular Topics category and select "Silicon Carbide and Gallium Nitride".

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