Second-Gen Technology Boosts Performance Of 650-V GaN FET Devices

Nexperia's new GaN FET devices feature the company's next-generation high-voltage GaN HEMT technology in both TO-247 packages and the company's proprietary CCPAK surface-mount packages. These H2 Gen devices achieve superior switching figures-of-merit (FOMs) and on-state performance with improved stability versus the company's H1 Gen devices, which were released last year.

The new GaN technology employs through-epi vias, reducing defects and shrinking die size by 24% versus the H1 gen devices. The initial release of the H2 Gen technology is in a traditional TO-247 (part number GAN041-650WSB). In this GaN FET, $R_{DS(ON)}$ is reduced to just 41 mΩ (max., 35 mΩ typ. at 25°C)—which represents an 18% improvement versus the H1 Gen device. This new part also offers a high threshold voltage and low diode forward voltage.

The H1 Gen device used for comparison here is the GAN063-650WSA, a 650-V, 50-mΩ GaN FET in a TO-247. The reduction in $R_{DS(ON)}$ will continue to 39 mΩ (max., 33 mΩ typ. at 25°C) with surface-mount versions of the device in the company's CCPAK package (part numbers GAN039-650NTB/NBB) (see the figure).

Both the TO-247 and CCPAK versions meet the demands of AEC-Q101 for automotive applications. (The AEC-Q101 qualified CCPAK devices will be available in 2021.)

According to Michael LeGoff, general manager GaN at Nexperia, the H2 technology will enable further improvements in $R_{DS(ON)}$, pushing performance to <20 mΩ and then <10 mΩ. These reductions in on-resistance will push the company's GaN devices into higher power ranges of 3.3 to 8 kW in the case of the sub 20-mΩ transistors and up to 150 kW with the sub 10-mΩ transistors. These devices are expected to be released by the end of 2021.

Dilder Chowdhury, Nexperia's GaN strategic marketing director commented, "Customers need a highly-efficient, cost-effective solution for high-power conversion at 650 V and around the 30- to 40- mΩ $R_{DS(ON)}$, where applications include on-board chargers, dc-dc converters and traction inverters in electric vehicles, and industrial power supplies in the 1.5- to 5-kW range for titanium-grade rack mounted telecoms, 5G and datacenters. Nexperia continues to invest in the development and expansion of its range of products using next-generation GaN processes, initially releasing traditional TO-247 versions and bare die format for power module makers, followed by our high-performance surface-mount CCPAK packages."

Nexperia's CCPAK surface-mount packaging adopts the company's proven innovative copper-clip package technology to replace internal bond wires. This reduces parasitic losses, optimizes electrical and thermal performance, and improves reliability. CCPAK GaN FETs are available in top- or bottom-cooled configurations making them very versatile and help further improving heat dissipation. The table below outlines the advantages of the CCPAK devices.

Like their H1 generation predecessors, the H2 Gen parts come in the familiar cascode configuration with a silicon MOSFET. This simplifies gate-drive requirements versus that of the GaN HEMT by itself. According to the company, the cascode approach also avoids compromises in device design, specifically the imposition of a special gate structure, that are required to support enhancement-mode operation. The cascode benefit mainly applies to devices rated at 400 V and above.

LeGoff observes that taking the cascode approach gives Nexperia "a clearer path" to migrating their GaN technology to higher voltage ratings such as 900 V and 1200 V as well as to achieving the lower on-resistance levels (such as sub 10 mΩ) on their roadmap.

The GAN041-650WSB in a TO-247 and the GAN039-650NBB in a CCPAK are sampling now. More information including product specs and datasheets is available at www.nexperia.com/gan-fets.

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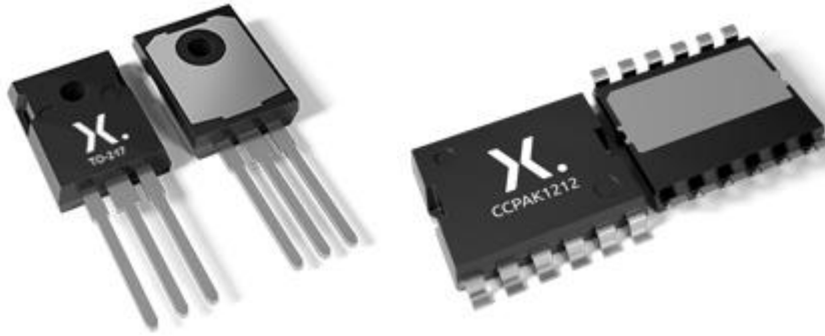

Figure. After releasing a 50-mΩ, 650-V, GaN power device in the TO-247 last year, the company has leveraged its new H2 GaN HEMT technology to produce a 41-mΩ device. Putting the same new die into the company's copper clip surface-mount package reduces on-resistance even further, down to 41 mΩ. The latter also offers top- and bottom-side cooling options.

Table. Benefits of Nexperia's copper-clip (CCPAK) packaging.

Copper clip	3x lower parasitic inductances for lower switching losses and EMI
	Higher reliability vs. wire-bond solution
Thermal performance	Low $R_{th(j-mb)}$ typ (<0.5 K/W) for optimal cooling
	175°C T_j max
Manufacturability and robustness	Flexible leads for temperature-cycling reliability
	Flexible gull-winged leads for robust board-level reliability
	Compatible with SMD soldering and AOI (automated optical inspection)

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