Kit Speeds Design Of Rad Hard Power ICs And Other Mixed-Signal Chips

Apogee Semiconductor, a provider of technologies and products for space and other extreme environments, has announced that its Transistor-Adjusted-Layout for Radiation (TalRad) Process Design Kit (PDK) is available for evaluation. The TalRad Process Design Kit is a rad-hard process design methodology that improves the radiation performance of commercial process technologies, enabling the rapid creation of rad-hard IC designs in a fraction of the time and effort previously required. Apogee Semiconductor and TSI Semiconductors have partnered to implement this kit in TSI's 180-nm CMOS high-voltage silicon process.

"Our products and services are targeted towards enabling small-satellites and large constellations that require high performance, small form factors and radiation resilience at a lower cost," states Anton Quiroz, CEO of Apogee Semiconductor. "We partnered with TSI Semiconductors to implement TalRad to increase the TID (total ionizing dose) performance of the baseline process by up to 10x, with little to no design performance penalties or process integration effort. The implementation of TalRad PDK includes the development of design-rule-checker and layout-vs-schematic rule decks, PCELLs and characterizing the radiation performance and reliability of the new components."

"It has been exciting to work with TSI Semiconductors to implement a rad-hard process that will make it significantly easier for IC designers to create cutting edge technologies for the space industry. We look forward to a continued partnership with TSI," continues Quiroz.

"This strategic partnership with Apogee will enable system designers to produce RAD Hard technology across a wide range of products for logic, high voltage, RF, analog, and mixed-signal applications." Now that the Apogee TalRadTM PDK is implemented and silicon qualified in our foundry, this technology can be evaluated using our MPW shuttle program prior to product qualification across a wide range of RAD Hard market segments, says Wilbur Catabay, SVP of TSI Corporate Strategy.

According to Quiroz, up until now, the options for IC design companies to design rad hard ICs when working with foundries have been limited. For example, if a company wants to design a data converter or PWM chip, they can download a process design kit from the fab, however, the components in that kit have not been characterized for radiation performance. "Even if you try to characterize them, they tend to be very weak," says Quiroz.

He adds "This generally happens in processes like 180 nm, where you want to do power design because it allows a decent amount of digital integration while also providing the high-voltage components that allow you to do power design."

Because the components provided in the standard process were unacceptable in terms of radiation hardness, the companies doing IC design were forced to do process development work. "If you wanted to do a rad hard design, you would essentially have to do your own layouts and make your own components. And those components would generally violate a bunch of rules, so there'd be a lot of custom work that you'd have to do. You would have to take their rule files and modify them," says Quiroz. It was a time consuming process.

"There would be many months of effort generally to get a process ready before you could even start an IC design. That's what we've short circuited by developing the TalRad Process Design Kit. Now you can start IC design right away."

By partnering with TSI Semiconductors, Apogee was able to take their commercial 180-nm process and develop new radiation hardened components within it, which then went into the new PDK. "So now if you want to do rad hard design you just use those rad hard transistors. You have a better chance of getting your rad hard design right," says Quiroz.

Apogee originally developed this process design kit so it could design its own rad hard ICs. For example, the company is currently in the process of developing a PWM-based converter to support use of GaN power devices in the next generation of space applications.

The PDK includes a couple of transistor-level features that support rad hard power design. First it provides a transistor with an annular layout. Essentially, that encloses the gate of the transistor to mitigate a critical leakage path that occurs under radiation. However, since that type of transistor can be problematic for analog circuits that require tight matching, the kit provides a new type, which it calls the TalRad transistor.

According to Quiroz, "it looks and feels like the standard transistor but we worked with the fab to modify the layout to mitigate the leakage path, so that that transistor is more radiation tolerant. And that's one that would help enable power supplies because you're looking at a more finely tuned transistor structure that you can use for your analog designs, which are obviously important for the type of matched components required in a PWM".

The company is still in the process of qualifying the PDK, so that it can be considered fully released. This qualification process requires extraction of Spice and other models. Therefore the kit is considered to be in the evaluation phase. But Quiroz adds that it is ready for customers to begin IC designs with as "all the components are locked down now."

If you are interested in an evaluation license for the TalRad rad-hard PDK or want more information, e-mail sales@apogeesemi.com or see the website.

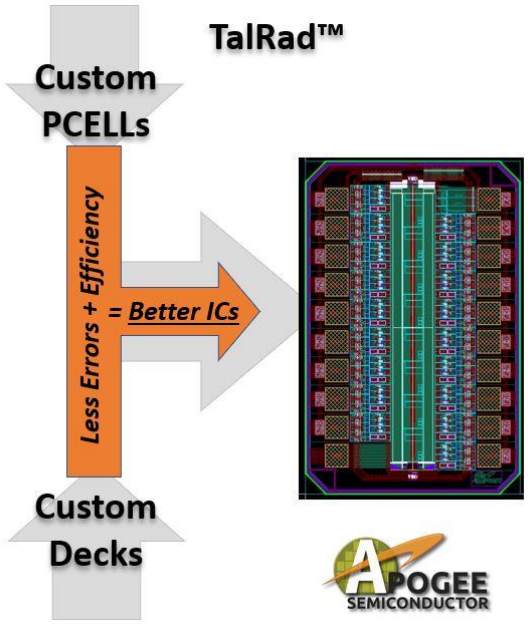

Figure. The TalRad Process Design Kit is a rad-hard process design methodology that improves the radiation performance of commercial IC process technologies, enabling much faster creation of rad-hard IC designs. This kit is implemented in TSI Semiconductors' 180-nm CMOS high-voltage silicon process, which offers both a high level of integration and the high-voltage components needed for power design. Using this kit, IC designers no longer have to do their own process development (i.e. doing their own transistor layouts and component development) to achieve radiation hardness when working with a commercial IC foundry.