HOW2POWER TODAY
Your Power Design Newsletter

**Focus on Magnetics**
Sponsored by Payton Planar

ISSUE: November 2020

# *Determining Design Power Over An Input Voltage Range (Part 1): Maximum Inductor Power*

*by Dennis Feucht, Innovatia Laboratories, Cayo, Belize*

The power ratings of components in converters depend on the range of input voltage over which the circuit is specified to operate. Designs are often rated based on a fixed input voltage, $V_g$ but for many applications with input power from batteries, the power line, or any source with a variable input voltage, the power requirements increase. This is typically the case with inductors and transformers used in power supply designs, and it results in oversizing or undersizing of these components during the magnetics design.

However, if the inductor and transformer transfer power are evaluated for a given PWM-switch configuration, it's possible to specify the device's power rating more accurately and better optimize component size. Yet, determining the magnetic component's maximum power consumption alone is not quite sufficient for optimizing the power rating and therefore the device size.

With that in mind, this article series introduces a new concept that I refer to as design power, which is the product of the max current seen by the component across the voltage range and the maximum range voltage. Though the component will never experience these values at the same time, it must still be able to handle both, which increases its size and power handling ability. Hence the need to derive this new parameter, which we can use to optimally rate the components.

In this three-part series, the design formulas for the design power of inductors and transformers are derived and their use in design is explained. Here in part 1, the maximum power requirement relative to maximum input power for an inductor of a PWM-switch power-transfer circuit is derived for the three PWM-based converter configurations. In this part 1, we derive equations for the maximum transfer power for an inductor within the $V_g$ range, and determine the $V_g$ at which this maximum power occurs. This will lead to derivation of the design power formula for an inductor in part 2, with the discussion extended to transformers in part 3.

## *Design Power For A $V_g$ Range*

$V_g$ is often specified over a range of allowable values. This increases the design value used for power in magnetics sizing. Usually the converter output is a fixed voltage or current as is the maximum average output power, $\overline{P}_o$. However, the inductor power rating in PWM-switch converters is related to the converter transfer power.

The *PWM-switch*, shown in Fig. 1, is a three-terminal device, the central feature of many converter power circuits.

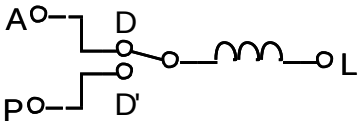


*Fig.1. The equivalent circuit model of a PWM-switch, the active component of most switching converters.*

As a three-terminal active device like a transistor, it has three two-port configurations:

- common active (CA) or *boost*
- common passive (CP) or *buck*
- common inductor (CL) or *boost-buck.*

The two ports are input and output port and the ports share a common terminal which identifies the configuration.

Some PWM-switch converters are not so easy to associate with one of the three configurations because they use circuit-isolating transformers. Some of these configurations are *boost push-pull* (transformer-coupled, center-tapped primary CA), *forward* (transformer-coupled CP), and *flyback* (common coupled-inductor, CL) converters. (We'll discuss the transformer-based configurations more in part 3.)

Ćuk-derived converters are CL converters with current steering. If in doubt, the converter configuration can be identified by its transfer function. The passive switch state is typically implemented by a diode and the active state by a transistor.

## Power Flows

PWM-switch converter power flow is diagrammed in Fig. 2 for constant converter input and output power.

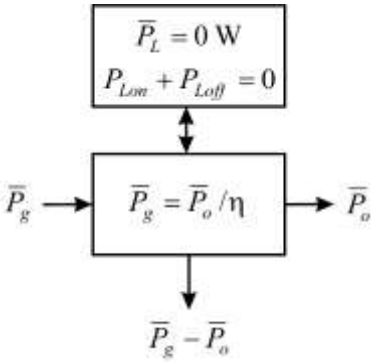


*Fig. 2. Power flows in a PWM-switch converter. The inductor stores energy (upper block) within a cycle.*

Power loss in the converter, dissipated as heat and attributed to inefficiency, is

$$\overline{P}_g - \overline{P}_o = \overline{P}_g \cdot (1-\eta)$$

where $\eta$ = efficiency. For design, $\eta_{\min}$ is the specified minimum $\eta$, which includes power loss in the inductor. The design value of $\overline{P}_g$ is the maximum required by $\eta_{\min}$ and $\overline{P}_o$.

If the power of both converter ports is accounted for, then as shown in Fig. 2, the net power flow of the inductor must be zero: $\overline{P}_L = 0\ \mathrm{W}$. The inductor *does* involve power flow, of course, and is a means by which power is transferred from input to output. During on- and off-times, $P_L \neq 0$ W, and

$$\overline{P}_L = P_{Lon} + P_{Loff} = 0\ \mathrm{W} \Rightarrow P_{Lon} = -P_{Loff}$$

The power the inductor sinks (stores) during the on-time as input is then sourced as output power during the off-time. The power flows are the algebraic opposite of each other, though their magnitudes are equal. Inductor power over a steady-state cycle is continual (≥ 0 W) for continuous-current (CCM) operation.

The converter output usually has a fixed output voltage or current with a maximum average output power specification, $\overline{P}_o$. If converter efficiency, $\eta$ is constant with power, then the maximum output power, with a voltage-source output at the maximum $I_o$ or a current-source output at the maximum $V_o$, relates to maximum input power through $\eta$ as $\overline{P}_g$.

## Input Port Power

The $V_g$ input voltage range is

$$V_g \in [V_{g\min}, V_{g\mathrm{mid}}, V_{g\max}]$$

At the input port, the average power for constant voltage, $V_g$ and varying current is

$$\overline{P}_g = V_g \cdot \bar{i}_g$$

The average converter input current, $\bar{i}_g$ is $i_g$ averaged over the switching cycle and is related to the on-time current amplitude, $I_g$ by

$$I_g = \bar{i}_g / D \ , \text{CP, CL}$$

$$I_g = \bar{i}_g \ , \text{CA}$$

The converter average input power is then expressed in $D$ as

$$\overline{P}_g = V_g \cdot \bar{i}_g = V_g \cdot (D \cdot I_g) = D \cdot (V_g \cdot I_g) = D \cdot P_g \ , \text{CP, CL}$$

$$\overline{P}_g = V_g \cdot \bar{i}_g = V_g \cdot I_g = P_g \ , \text{CA}$$

where $P_g$ is the on-time power amplitude.

At constant input power, $\bar{i}_g$ as a design parameter varies inversely with $V_g$ as

$$\bar{i}_g = \frac{\overline{P}_g}{V_g}$$

so that if $V_g$ has a range of $r$, so will $\bar{i}_g$;

$$r = \frac{V_{g\max}}{V_{g\min}} = \frac{\bar{i}_{g\max}}{\bar{i}_{g\min}}, \text{ constant } \overline{P}_g$$

The input current range varies inversely with the $V_g$ range. Ordering the extreme values to correspond with those in $V_g$,

$$\bar{i}_g \in [\bar{i}_{g\max}, \bar{i}_{g\text{mid}}, \bar{i}_{g\min}]$$

### *Inductor Power*

Average inductor power is

$$\overline{P}_L = \bar{v}_L \cdot I_L$$

In actual circuits during on-time or off-time intervals, inductor current amplitude, $I_L$ does vary somewhat, but if the *small-ripple approximation* (ripple amplitude << average) holds (as it does for large inductance), the $I_L$ amplitude is approximated as the average of the current over the on- or off-time interval. For any value within its range, the input port has a constant $V_g$ while the inductor is considered to have constant $I_L$.

Inductor current under the small-ripple approximation is constant and is the amplitude of $i_g$ during $D$, the on-time fraction of the cycle. $I_L = I_g$ but in the CP (buck) and CL (boost-buck) configurations, $i_L \approx I_L \neq i_g$ because $i_g$

is not constant but is zero during off-time. Only CA (boost) input current is continuous and constant ($i_g = I_L$) but its output current is zero during on-time with an average,

$$\bar{i}_o = D' \cdot I_g = D' \cdot I_L \text{ , CA, CL}$$

The relationships between $\bar{i}_L = I_L$ and $\bar{i}_g$ for the three configurations are

$$\bar{i}_L = \bar{i}_g \text{ , CA} \quad ; \quad \bar{i}_L = \bar{i}_g / D \text{ , CP, CL}$$

The average on-time or off-time inductor voltage magnitude is

$$\bar{v}_L = D \cdot V_g \text{ , CA, CL} \quad ; \quad \bar{v}_L = D \cdot (V_g - V_o) = D \cdot D' \cdot V_g \text{ , CP}$$

Both cycle-average inductor power and voltage across the inductor are zero, though for both they are equal in magnitude for on- and off-times while opposite in polarity. The average inductor power magnitude during both on-time and off-time is

$$\overline{P}_L = \bar{v}_L \cdot I_L = (D \cdot V_g) \cdot I_g = D \cdot P_g = D \cdot \overline{P}_g \text{ , CA}$$

$$\overline{P}_L = \bar{v}_L \cdot I_L = (D \cdot D' \cdot V_g) \cdot (\bar{i}_g / D) = D' \cdot (V_g \cdot \bar{i}_g) = D' \cdot \overline{P}_g \text{ , CP}$$

$$\overline{P}_L = \bar{v}_L \cdot I_L = (D \cdot V_g) \cdot I_g = D \cdot P_g = \overline{P}_g \text{ , CL}$$

Over a $V_g$ range, we are interested in finding $\overline{P}_{L\max}$.

The inductor-power fraction of converter transfer power is found by substitution for $D$ as expressed in port voltages, given in the table. The maximum inductor power as a fraction of input power for a given circuit of the three configurations is expressed at the maximum end of its range.

Table. Maximum inductor power over $V_g$, expressed as a fraction of input power.

| *Configuration* | *Duty ratio, D* | *Max inductor power,* $\overline{P}_{L\max}$ | *Max inductor power vs. input power,* $\frac{\overline{P}_{L\max}}{\overline{P}_g}$ |
|---|---|---|---|
| *CA (boost)* | $1 - \frac{V_g}{V_o}$ | $D_{\max} \cdot \overline{P}_g$ | $D_{\max} = 1 - \frac{V_{g\min}}{V_o}$ |
| *CP (buck)* | $\frac{V_o}{V_g}$ | $D'_{\max} \cdot \overline{P}_g$ | $D'_{\max} = 1 - D_{\min} = 1 - \frac{V_o}{V_{g\max}}$ |
| *CL (boost-buck)* | $\frac{V_o}{V_o + V_g}$ | $\overline{P}_g$ | *1* |

$\overline{P}_{L\max}$ occurs at different ends of the range of *D* and $V_g$ for the CA and CP configurations. For the CA, it is at minimum $V_g$ and for the CP, it is at maximum $V_g$. The CL configuration does not depend on *D*, and $\overline{P}_{L\max} = \overline{P}_g$ over its entire $V_g$ range. This includes the transductor of Ćuk-derived converters.

Plots of $D(V_g, V_o)$ for the three configurations are shown in Fig. 2. All monotonically decrease with $V_g$ and are maximum at $V_{g\min}$ and minimum at $V_{g\max}$. They are all equal to ⅓ at $V_{g\text{mid}}$ = 20 V.

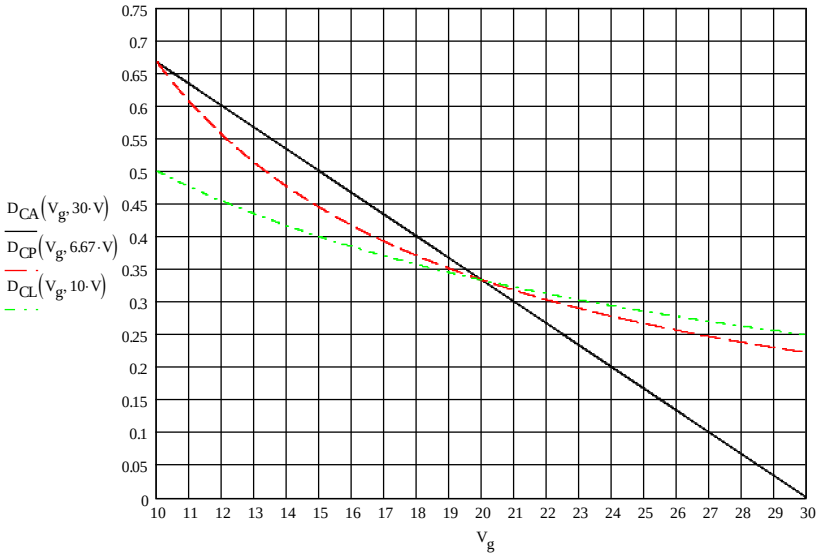


*Fig 2. Duty ratio plotted versus converter input voltage for each PWM-switch configuration.*

A CA (boost) converter with $V_o$ = 50 V has

$$\frac{\overline{P}_{L\max}}{\overline{P}_g} = D_{\max} = 1 - \frac{V_{g\min}}{V_o} = 1 - \frac{10\text{ V}}{50\text{ V}} = 0.8$$

The maximum inductor power is 80% of the input power, whereas at the midrange $V_g$ = 20 V, $\overline{P}_L = 0.6 \cdot \overline{P}_g$, or 25% less in power rating. For a CP with $V_o$ = 5 V,

$$\frac{\overline{P}_{L\max}}{\overline{P}_g} = D'_{\max} = 1 - \frac{V_o}{V_{g\max}} = 1 - \frac{5\text{ V}}{30\text{ V}} \approx 0.833$$

whereas at the midrange $V_g$, the power ratio is 0.75, a 10% reduction in power. And for the trivial case, a CL (such as a Ćuk converter) with $V_g$ = 20 V has $\overline{P}_L = \overline{P}_g$. For all configurations,

$$\overline{P}_{L\max} \le \overline{P}_g$$

$\overline{P}_{L\max}$ is the maximum power for the inductor, but it must be rated or sized for power over the $V_g$ range and not only at the $V_g$ of $\overline{P}_{L\max}$. In part 2, we will determine how much this *design power* needs to be.

## About The Author

*Dennis Feucht has been involved in power electronics for 35 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.*

For more on magnetics design, see these How2Power Design Guide search results.