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Raising The Plateau Level In Valley-Fill PFC Circuits Improves Efficiency

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Most equipment that connects to the ac power grid must comply with the IEC 61000-3-2 basic international EMC standard dealing with the limitation of harmonic currents injected onto the grid. The standard applies to equipment with a rated current of up to 16 A and specifies limits on the harmonic components of the input current that can be produced by the equipment. The reason for such limits is that the conversion of ac power is typically associated with harmonic distortion of the supply current which can cause mains voltage distortion and affect operation of other devices coupled to the same ac mains.

There are four classes of equipment defined in this standard. Balanced three-phase equipment and information technology equipment are typical examples of the class A devices, which are subject to the strictest limits on harmonic levels. Classes C through D devices are required to meet less stringent limits on harmonics. Class B devices include portable tools and arc welding equipment, while class C covers lighting equipment. The last category, class D, covers equipment that has a specified power consumption less than or equal to 600 W, such as personal computers or personal computer monitors.

For class A equipment, active (boost) power factor correction (PFC) circuits[1] shape the current wave into a sinusoid and are used to comply with the IEC standard. For equipment in classes C through D and especially higher-power-rated equipment connected to the upstream points of common coupling in electricity distribution systems, which is covered by IEC6100-3-12, the less strict harmonic limits allow for a different approach. For these types of equipment, cheaper and more robust passive PFC stages can represent a more attractive and cost-effective solution.

The passive capacitive PFC circuit, which employs capacitor-diode networks in the valley-fill (VF) PFC configuration, can improve power factor and reduce harmonic distortion of the input line current with a reduction in volume versus active PFC circuits.[2] However, the operating principle of the existing VF-PFC circuit causes excessive supply voltage variations resulting in higher current magnitudes and higher power dissipation in the power conversion stages that follow the PFC stage. These losses are influenced by the so-called plateau level in the VF-PFC waveforms.

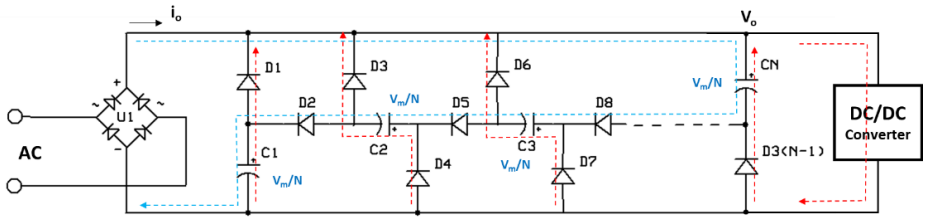
After reviewing the operation, characteristics and benefits of conventional implementations of the VF-PFC circuit, in which the plateau level is typically one half of the peak ac voltage or less, this article discusses the efficiency improvement made possible by a novel implementation of the VF-PFC in which a higher plateau level is employed. An analysis of power losses in the dc-dc converter that follows the VF-PFC reveals which higher plateau levels are optimum in practice.

Valley-Fill PFC With Plateau Levels Not Exceeding 0.5 V_m

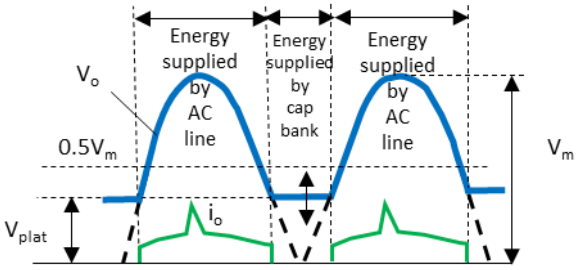
Since dc voltage is required for the operation of any active power conversion stage, a bridge rectifier that provides full-wave rectification from a two-wire ac input has become an integral component of ac power conversion stages. Such rectifiers are widely used in linear and switch-mode power supplies, arc welding and lighting systems, electronic ballasts, etc. The simplest and most common configuration of this rectifier with capacitive filter produces harmonic distortion in the input current waveform that may not be suitable for many applications.

A valley-fill capacitor-diode (C-D) network is a type of passive PFC circuit that is intended to improve the current shape in a conventional rectifier. The method it implements is based on expanding the conduction angle of the bridge rectifier diodes and creating different paths for charge (in series) and discharge (in parallel) of stored energy using an *electrically dispersed capacitor bank*. In such an arrangement, there is no direct electrical connection between the capacitors and they get coupled to the output only when certain diodes conduct.

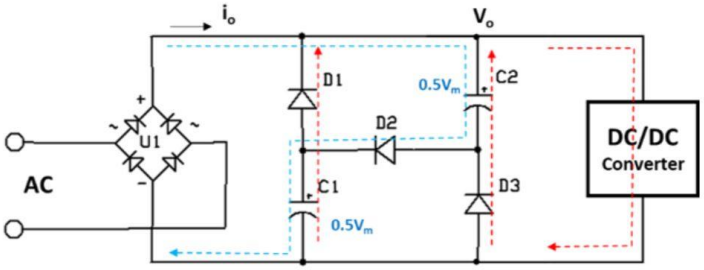
A basic valley-fill PFC technique that implements this method is shown in Fig. 1a, for plateau levels not exceeding 50% of the peak ac voltage V_m. The associated voltage (blue) and current (green) waveforms are shown in Fig. 1b. Fig. 1c shows the most commonly used $0.5V_m$ plateau configuration[2] and the associated voltage and current waveforms are shown in Fig. 1d.



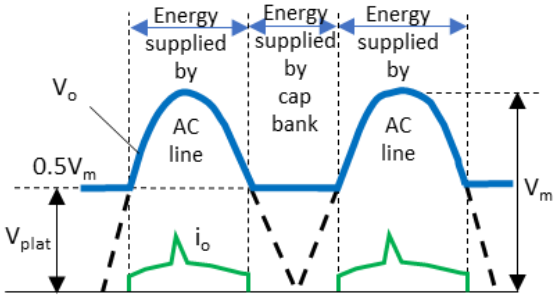
(a) General case. The VF circuit contains N energy storing caps and 3(N-1) diodes to create a supply ac voltage plateau at a level of $V_{plat} \leq V_m/2$.



(b) Example voltage (blue) and current (green) waveforms for the general case VF circuit where $V_{plat} = V_m/N$.



(c) Special case. The simplest valley-fill PFC circuit has a plateau of $V_{plat} = V_m/2$.



(d) Example output voltage (and current) waveforms for the $V_{plat} = V_m/2$ VF circuit.

Fig. 1. Valley-fill PFC arrangements with plateau levels below or equal to 50% of the peak ac voltage V_m.

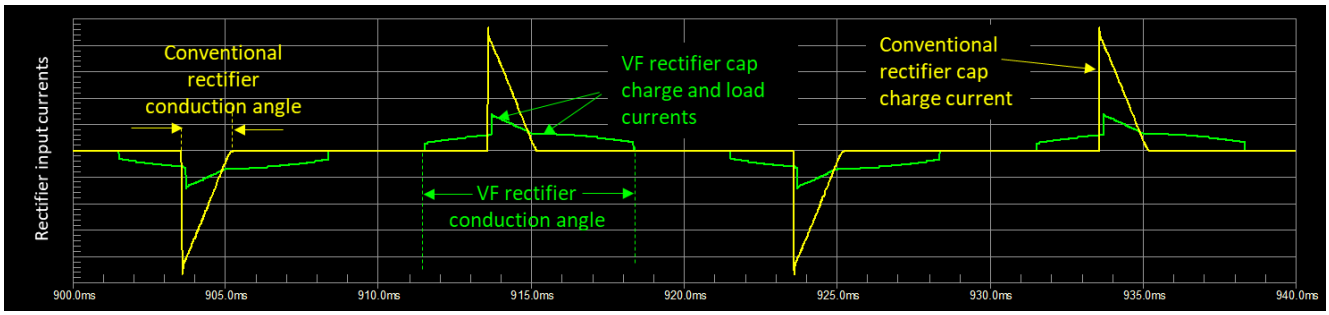
In Fig. 1a, cap charge current (shown with the dashed blue line) flows from the bridge rectifier U1, through a series capacitor and diode chain of C1, D2, C2…CN. Caps C1-CN discharge in parallel through the load via corresponding diodes when the line voltage drops below the plateau level $V_{plat} = V_m/N$. The discharge current paths are shown in Fig. 1a with dashed red lines.

The paths for capacitor bank charge and discharge currents in the most widely used $V_{plat} = V_m/2$ circuit (Fig. 1c) are also shown with dashed blue and red lines, respectively. The current and voltage waveforms in VF circuits are given in Fig. 1b and d.

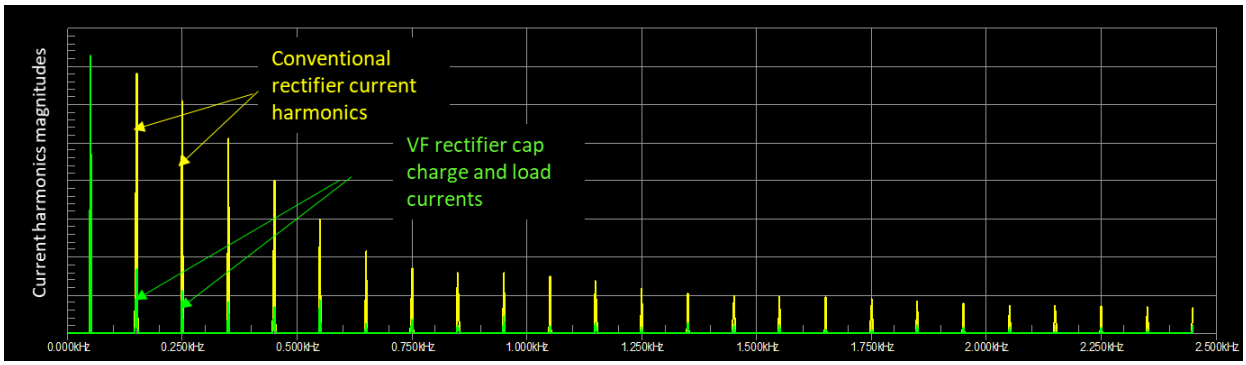
When the ac line voltage is below the plateau level, energy to the load is supplied by the cap bank. Once the ac voltage exceeds the plateau level (V_m/N), the VF network diodes become reverse biased and the rectifier output current i_o flows through the load. When line voltage approaches the V_m level, the caps get charged and the rectifier current has a distinctive spike as indicated by the green waveforms (Fig. 1b and d). The lower the plateau level, the longer energy is supplied directly from the ac line to the load over each line cycle.

Benefits Of Valley-Fill Circuit

To illustrate the benefit of the VF PFC circuit let's compare harmonic current levels in conventional and valley-fill $V_{plat} = 0.5V_m$ rectifiers operating in constant-resistance mode. This comparison at identical power and capacitor ripple levels is illustrated in Fig. 2.



(a)



(b)

Fig. 2. Comparison of valley-fill rectifier (green lines) and conventional rectifier with capacitive filter (yellow lines): input current waveforms (a) and current harmonic magnitudes (b).

The current spectrums in Fig. 2b show that the VF topology has significant advantages over the conventional rectification case. In order to make this comparison more quantitative and apparent let's compute the power factor (PF) for each of these cases using the standard equation for a non-linear load case:

$$F = \frac{I_{1RMS}\cos\varphi}{\sqrt{\sum_{k=1}^{\infty} I_{kRMS}^2}} \qquad (1)$$

where I_{1rms} and I_{krms} are RMS values of the first (fundamental) current harmonic and the kth-order current harmonic, respectively, and $\cos\varphi$ is the cosine of the angle between the input voltage and the fundamental current waves.

This computation yields PFs of 0.482 and 0.932 respectively, such that using valley-fill architecture allows us to increase the power factor by 45%. The harmonic content can be further decreased by making minor modifications to this circuit, such as adding a voltage doubler or smoothing components.[2-4] Such improvements in many cases allow users to reduce the RMS current drawn by equipment from the ac line, and thereby meet the requirements of the IEC standard, making the equipment acceptable for connection to the power grid.

Comparing the waveforms in Fig. 2a we find that such a significant power factor improvement is achieved by increasing the conduction angle of the bridge rectifier diodes. It is also apparent that the lower the plateau level the larger the conduction angle and the larger the power factor that can be provided. Such an approach is applicable to relatively small constant power (CP) loads and loads operating in constant-resistance mode.

However, for high-power loads operating in CP mode, the current shape will change and higher harmonics will become more significant. Although the impact of these higher harmonics can be counterbalanced by lowering the plateau level and increasing the conduction angle of the bridge rectifier diodes, the drawback of this approach in CP mode is the increase in converter current and the associated power loss in the power conversion stage that follows the PFC circuit.

This point is illustrated in Fig. 3 where two cases with plateau levels of $V_m/2$ and $V_m/3$ are given for comparison. Fig. 3 waveforms show that lowering the plateau level from $V_m/2$ to $V_m/3$ causes 1.5 times higher average current drawn by the power conversion stage and leads to increased stress on the dc-dc converter's active components.

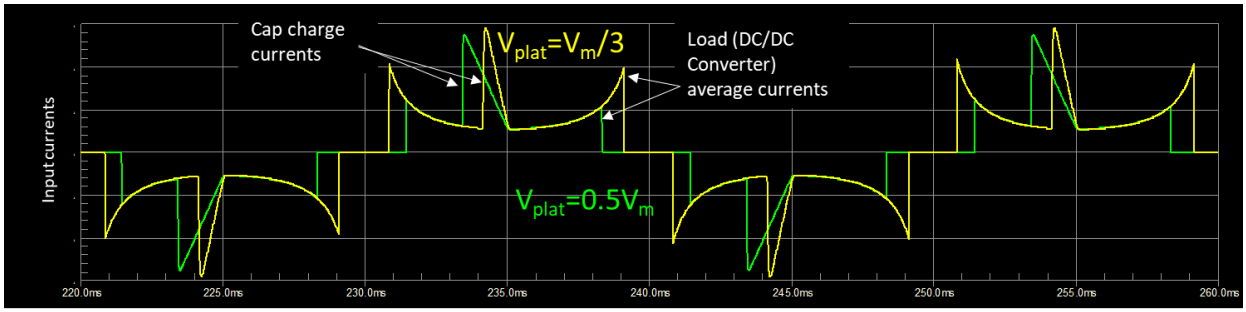


Fig. 3. In constant-power mode, lowering the plateau level to increase the conduction angle of the rectifier has a side effect—an increase of the current stress on the dc-dc converter's active components as reflected by the higher average input currents to the converter.

Another shortcoming associated with constant-power mode operation is that even at $V_{plat} = V_m/2$ converter, the variation in average current (2X) is so significant that a VF circuit with such a plateau level can be considered feasible only for relatively low power applications in which such variation does not noticeably impact device size and cost.

For high-power applications of several kilowatts or more, in which power losses directly impact equipment dimensions, utilizing low plateau levels becomes practically prohibitive due to such current variations. To overcome this obstacle for high-power applications, it becomes more important to consider the means for power loss reduction in the converter following the VF rectifier. Thus, the option of raising the plateau level needs to

be evaluated and weighed against the traditional low-level VF techniques to see if it could provide considerable power loss reduction.

Power Loss Reduction Opportunities With Higher Plateau Levels

Fig. 3 shows that the maximum average current drawn by the dc-dc converter from the VF rectifier in CP mode decreases when the plateau level is raised. At the same time, when the converter supply voltage is at its minimum level (in VF case $V_{o.min} = V_{plat}$), in a higher plateau case, the converter switches operate at their maximum duty ratio for a longer time which somewhat offsets the current magnitude reduction.

Let's examine if a noticeable overall power loss reduction could be achieved by elevating the plateau from the baseline ($V_{plat} = 0.5V_m$) to higher levels and compare the losses for these two cases. For simplicity, let's assume that the rectifier storage caps are large enough that the converter supply voltage V_o remains constant over the plateau time interval, that the converter contains one active switching component, and that conduction losses in the dc-dc converter are dominating because it uses one of the soft-switching topologies (ZVS or ZCS).

These assumptions are justified because in multi-switch converters the losses will be equally split between their active components without changing the comparison results and for hard-switching topologies switching loss will be reduced proportionally to the reduction of the switch current magnitude. Thus, in this case the average power loss in the converter switch over the plateau time interval can be determined as follows:

$$P_{loss.avg.plat} = I_m^2 r D_{max}$$

where I_m is the switch current magnitude, r is the switch resistance in the on-state and D_{max} is the maximum duty ratio of the converter switch current corresponding to the minimum (plateau) voltage supplied by the VF rectifier.

Once the supply voltage enters the sine wave region and starts to rise, in order to keep the load power unchanged, the duty ratio will need to change in inverse proportion to the supplied voltage level. For the sinewave time interval, the switch conduction power loss over each switching cycle will be determined by the instantaneous voltage supplied to the converter. So, based on this condition, average power loss over one switching cycle can be determined as follows:

$$P_{loss.avg.i} = I_m^2 r \frac{D_{max} \cdot V_{plat}}{V_m \sin 2\pi F_L t_i}$$

where i is the switching cycle number, F_L is the line frequency, t_i is switching cycle time counted from the crossing point $t_i = i/F_{sw}$, and F_{sw} is switching frequency. Average power loss over the V_o sine wave time interval can be determined by dividing the sum of all $P_{loss.avg.i}$ computed over this interval by the number of switching cycles n in it:

$$P_{loss.avg.sine} = \frac{I_m^2 r D_{max} \cdot V_{plat}/V_m}{n} \cdot \sum_{i=1}^{n} \frac{1}{\sin(i \cdot 2\pi F_L/F_{sw} + \sin^{-1} V_{plat}/V_m)} \qquad (2)$$

where $\sin^{-1} V_{plat}/V_m$ is the sine wave phase at the plateau crossing point. The number of switching cycles n in the supply voltage sinusoidal region depends on the current conduction angle θ_{cond}, line F_L and switching F_{SW} frequencies:

$$n = F_{SW}\, \theta_{cond}/2\pi F_L \qquad (3)$$

The current conduction angle θ_{cond} (see Fig. 4) can be computed as:

$$\theta_{cond} = 2 \cos^{-1}(V_{plat}/V_m) \qquad (4)$$

Using a term defined for equation (2), the sinewave phase at the plateau-sinewave crossing is labeled in Fig. 4 as $\sin^{-1} V_{plat}/V_m$.

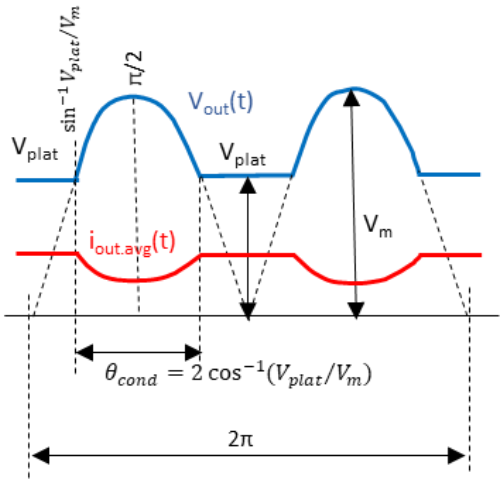


Fig. 4. VF rectifier output voltage and converter average current waveforms in CP mode.

Substituting equation (3) into (2) we can get an expression for average power loss over the $V_o(t)$ sine wave time interval at different plateau levels and their corresponding conduction angles as determined by equation (4):

$$P_{loss.avg.sine} = P_{loss.avg.plat} \cdot K(V_{plat}/V_m) \qquad (5)$$

where $K(V_{plat}/V_m)$ is the power loss factor determined by the following equation:

$$K(V_{plat}/V_m) = \frac{V_{plat}/V_m}{F_{SW}\theta_{cond}/2\pi F_L} \cdot \sum_{i=1}^{n} \frac{1}{\sin(i \cdot 2\pi F_L/F_{sw} + \sin^{-1}V_{plat}/V_m)} \qquad (6)$$

Average conduction power loss can be computed as the average power over a full rectified voltage cycle based on the relative time intervals of the plateau and the sinewave regions:

$$P_{loss.avg} = P_{loss.avg.plat} \cdot D_{plat} + P_{loss.avg.plat} \cdot K\left(V_{plat}/V_m\right) \cdot (1 - D_{plat}) \qquad (7)$$

where D_{plat} is the ratio of the plateau time to the rectified-voltage cycle time.

VF rectifier parameter data for different plateau levels obtained with equations (5) through (7) are provided in Table 1 below. At practical high switching frequencies (F_{sw} >> F_L) the power loss factor does not depend on the number of switching cycles, so for simplicity $K(V_{plat}/V_m)$ in Table 1 was computed under the assumption that the switching to line frequency ratio F_{sw}/F_L equals 1000.

Using $P_{loss.avg}/P_{loss.avg.plat}$ ratios and assuming that converter design is optimized for a given supplied voltage range, i.e., that its active component current magnitude is inversely proportional to the plateau voltage level $I_{m1}/I_{m2} = V_{plat2}/V_{plat1}$, we can find the total relative conduction power losses for each of the plateau cases. This data in the normalized form (relative to the V_{plat}/V_m=0.5 case) is provided in Table 2.

Data in Table 2 shows that elevating the VF plateau level from 1/2 to 2/3 or to 3/4 of V_m provides a significant conduction power loss reduction in the dc-dc converter—by 35% and 46%, respectively, and makes VF rectifiers with higher plateau levels an attractive option for high-power applications.

Table 1. VF rectifier and dc-dc converter parameters calculated at different plateau levels.

V_{plat}/V_m	1/4	1/3	1/2	2/3	3/4	4/5
Conduction angle, θ_{cond}, rad	2.64	2.46	2.09	1.68	1.45	1.29
Number of switching cycles in the sinewave, n	420	392	333	268	230	205
Sine wave region P_{loss} factor $K(V_{plat}/V_m)$	0.392	0.477	0.627	0.764	0.825	0.859
Plateau duty, D_{plat}	0.161	0.216	0.333	0.465	0.540	0.590
Full rectified voltage cycle $P_{loss.avg}/P_{loss.avg.plat}$	0.490	0.590	0.751	0.874	0.919	0.942
$P_{loss.avg}/P_{loss.avg.plat}$ normalized over V_{plat}/V_m = 0.5 case	0.652	0.786	1.000	1.163	1.224	1.254

Table 2. Dc-dc converter conduction power losses at different plateau levels for the VF rectifier.

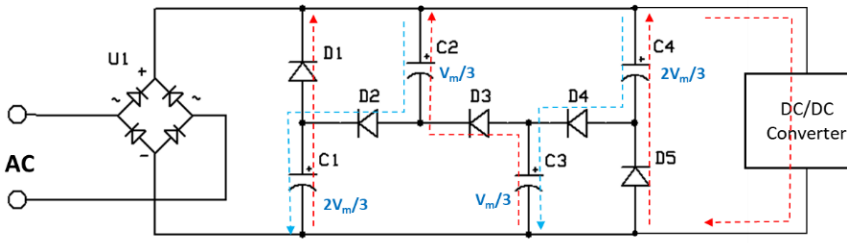
V_{plat}/V_m	1/4	1/3	1/2	2/3	3/4	4/5
Conduction power loss normalized over V_{plat}/V_m = 0.5 case	2.61	1.77	1.00	0.65	0.54	0.49

Higher Plateau Levels

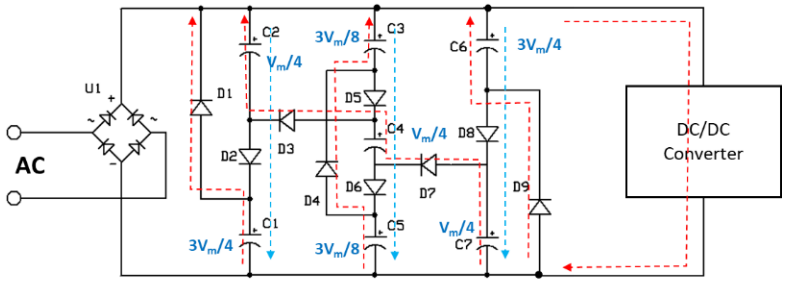
The VF plateau can theoretically be raised to any level not exceeding the ac voltage magnitude V_m, but would require an increase in parts count, especially at a V_{plat} level approaching V_m. Unlike the case of the low plateau level, the capacitor bank for $V_{plat} > 0.5V_m$ cases needs to be split into several series C-D branches operating in parallel on cap charge and discharge time intervals. Each of such implementations would require using (4X-7) diodes and (3X-5) caps, where X is the denominator of a fraction that represents the relative plateau level as a portion of the V_m value, such that $X = V_m/(V_m - V_{plat})$. This is why the electrical characteristics of VF-PFC circuits change discretely with X and the corresponding number of parts used.

As can be seen from Table 2, approaching V_m with the plateau provides diminishing returns in power loss reduction for the plateau levels exceeding $0.75V_m$. This means that the topologies that can be recommended for energy efficient use are $V_{plat} = 2/3V_m$ and $V_{plat} = 3/4V_m$. They are shown in Fig. 5a and Fig.5b, respectively. The VF topology with $V_{plat} = 4/5V_m$ is shown in Fig. 5c for reference purposes.

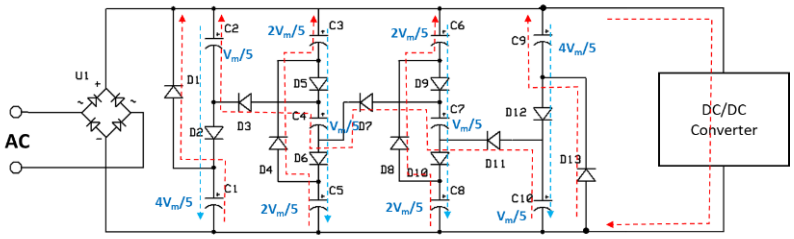
As can be seen from Table 1, the conduction angle shrinks as V_{plat} approaches V_m. This means that besides the diminishing returns in power loss reduction in the dc-dc converter stage, higher-order harmonics will receive higher weight. In other words, effective utilization of VF rectifiers with high plateau levels may be considered reasonable for higher power ranges for which the IEC 61000-3-12 standard with its less strict harmonics requirements is applicable.



(a) V_{plat}= 2/3V_m, C_1 = C_4 = C, and C_2 = C_3 = 2C.



(b) V_{plat} = 3/4V_m, C_1 = C_6 = C, C_3 = C_5 = 2C and C_2 = C_4 = C_7 = 3C.



(c) V_{plat} = 4/5V_m, C_1 = C_9 = C, C_3 = C_5 = C_6 = C_8 = 2C and C_2 = C_4 = C_7 = C_{10} = 4C.

Fig. 5. Valley-fill rectifier topologies with plateau levels raised above 0.5V_m.

Similar to the low plateau level cases, the paths for capacitor charge and discharge currents are shown in Fig. 5 with dashed blue and red lines. The capacitance used in the VF cap bank should be large enough to keep the output voltage drop over the plateau time interval below the specified value ΔV_p:

$$C_{eqv} = \frac{P_o}{F_L V_m^2} \frac{\sin^{-1} V_{plat}/V_m + \sin^{-1}[(1-\widehat{\Delta V})\cdot V_{plat}/V_m]}{2\pi (V_{plat}/V_m)^2 (2-\widehat{\Delta V})\widehat{\Delta V}} \qquad (8)$$

where P_o is the rectifier output power level and $\widehat{\Delta V}$ is the specified output voltage drop over the plateau time interval normalized versus the V_{plat} level, $\widehat{\Delta V} = \Delta V_p/V_{plat}$.

For example, for P_o = 1 kW, $\widehat{\Delta V}$ = 0.1, F_L = 50 Hz we can determine with equation (8) the required C_{eqv} or equivalent specific capacitance (C_s = C_{eqv}/P_o) values for different plateau levels. These are given in Table 3 below.

Table 3. Equivalent specific capacitance values for different plateau levels ($\widehat{\Delta V}$ = 0.1, F_L = 50 Hz).

V_{plat}/V_m	0.50	0.67	0.75	0.80	0.90
C_s, μF/W	0.737	0.573	0.525	0.503	0.474

The nominal operating voltage for each bank capacitor as well as its nominal capacitance value for the recommended VF rectifier topologies can be determined based on the ratios and labels provided in Fig. 5.

References

1. "What's the Difference Between Passive and Active Power-Factor Correctors?" by Maria Guerra, Electronic Design, December 2015.
2. "Electronic Fluorescent Ballast using a Power Factor Correction Technique for Loads Greater than 300 Watts" by Jim Spangler, Badruzzaman Hussain and Anup K. Behera, Proceedings of the Sixth Annual Applied Power Electronics Conf., March 10-15, 1991, pp. 393-399.
3. "Improved Valley-Fill Passive Current Shaper" by K. Kit Sum, Power Systems World '97, pp.1-8.
4. "An improved Valley-Fill passive Power-Factor-Correction circuit for electronic ballast" by Jiří Drápela and Jaromír Bok, Proceedings of the 9th International Scientific Conference on Electric Power Engineering 2008, EPE 2008, 2008, pp. 149-155.

About The Author

Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

For more on designing PFC stages, see How2Power's Design Guide, locate the "Popular Topics" category and select "Power Factor Correction".