750-V SiC FETs Boast A Low On-Resistance Of 6 mΩ

UnitedSiC's expanded family of 750-V SiC FETs include a device with an on-resistance of just 6 mΩ, which is said to be less than half the $R_{DS(ON)}$ of the nearest SiC MOSFET competitor (see Fig. 1). This device, part number UJ4SC075006K4S, also provides a robust short-circuit withstand time rating of 5 µs (Fig. 2).

The 6-mΩ device is just one of nine new device/package options in the 750-V SiC FET series, rated at 6, 9, 11, 23, 33, and 44 mΩ. All devices are available in the TO-247-4L package while the devices with 18, 23, 33, 44, and 60 mΩ also come in the TO-247-3L. Fig. 3 compares these various $R_{DS(ON)}$ against those of existing SiC MOSFETs available at 650 V or 750 V.

Complemented by the already available 18- and 60-mΩ devices, which were released last December, this 750-V expanded series provides designers with more device options, enabling greater design flexibility to achieve an optimum cost/efficiency tradeoff while maintaining generous design margins and circuit robustness.

According to Chris Dries, president and CEO of UnitedSiC, automotive requirements were a key driver for development of a SiC FET with the 750-V rating. Dries notes that automotive customers wanted a device that provided more headroom in EV applications using 400-V batteries. So the 750-V devices fill that need in comparison with the more common 650-V devices. The table shows how the 750-V Gen 4 SiC FETs stack up against 650-V Gen 3 and Gen 2 SiC MOSFETs in the EV traction inverter application with respect to chip area, losses and junction temperature.

Gen 4 SiC FETs from UnitedSiC are a cascode of a SiC JFET and a co-packaged silicon MOSFET. According to the vendor, these together provide the full advantages of wide bandgap technology—high speed and low losses with high-temperature operation, while retaining an easy, stable, and robust gate drive with integral ESD protection. The advantages are quantified by figures of merit (FoMs) such as $R_{DS(on)}$ x A, a measure of conduction losses per unit die area. Gen 4 SiC FETs achieve the lowest values in the market for this FOM at both high and low die temperatures, says the vendor.

Another notable FOM is $R_{DS(on)}$ x E_{OSS}/Q_{OSS}, which is important in hard-switching applications. With regard to this FOM, the company notes that their devices have values that are half those of the nearest competitor. They also say that their SiC FETs have an advantage in terms of $R_{DS(on)}$ x $C_{OSS(tr)}$, a FoM that is critical in soft-switching applications. UnitedSiC device values for this FOM, even at 750 V, are said to be around 30% less than those of competitors' 650-V parts.

For hard switching applications, the integral body diode of SiC FETs is superior to that of competing Si MOSFETs or SiC MOSFETs in terms of recovery speed and forward voltage drop, according to United SiC. Another advantage incorporated into the Gen 4 technology is its reduced thermal resistance from die to case, achieved by advanced wafer thinning techniques and silver-sinter die-attach. These features enable maximum power output for low die temperature rise in demanding applications.

With their latest improvements in switching efficiency and on-resistance, the new UnitedSiC SiC FETs are well suited for challenging, emerging applications. These include traction drives and on- and off-board chargers in electric vehicles and all stages of uni- and bi-directional power conversion in renewable energy inverters, power factor correction stages, telecoms converters and ac-dc or dc-dc power conversion generally. Established applications also benefit from use of the devices for an easy boost in efficiency with their backwards compatibility with Si MOSFET and IGBT gate drives and established TO-247 packaging.

As Chris Dries, states, "The UnitedSiC Gen 4 SiC FETs are unquestionably the performance leaders within competing technologies and set a new benchmark in wide bandgap switch technology. The new range additions now provide further options for all performance and budget specifications, and a wider range of applications."

Unit pricing in quantities of 1000 for the new 750-V Gen 4 SiC FETs range from $4.15 for the UJ4C075044K3S, to $23.46 for the UJ4SC075006K4S. All devices are available from authorized distributors. For more information, see the website.

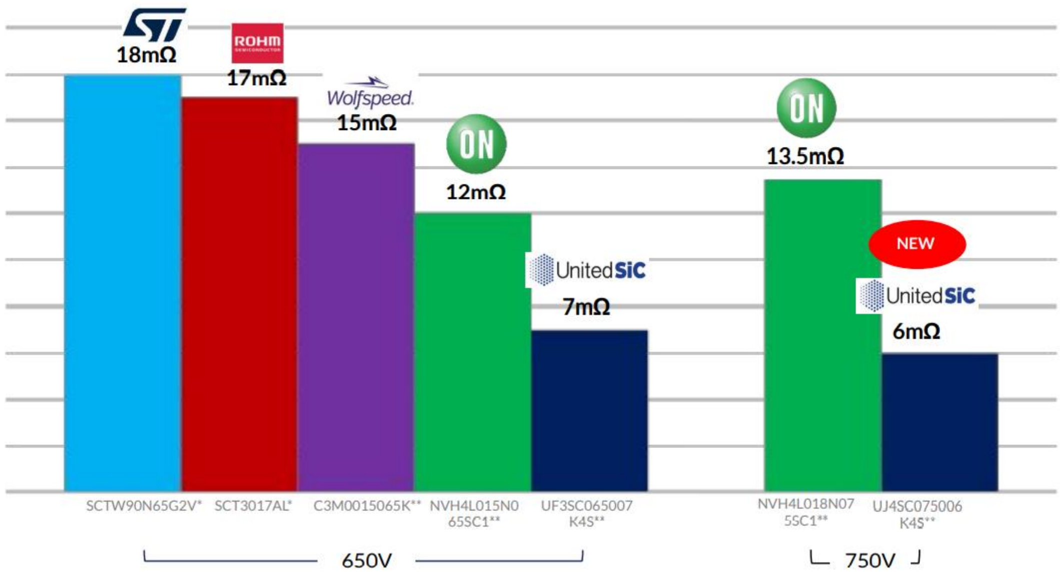

Fig. 1. When compared against existing 650-V and 750-V SiC MOSFETs, a UnitedSiC Gen 4, 6-mΩ 750-V SiC FET is said to offer significantly lower on-resistance. It also offers an improvement versus the company's own 650-V SiC FET, a Gen 3 device with an on-resistance of 7 mΩ.

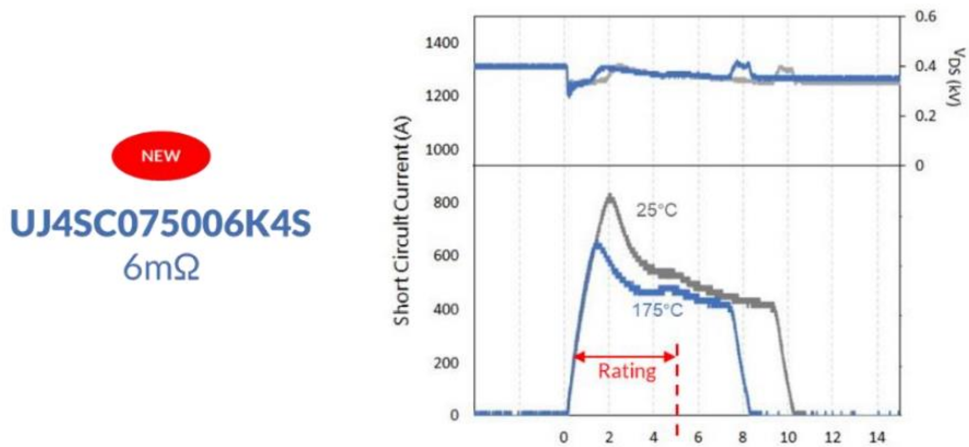

Fig. 2. Despite its low on-resistance, the 6-mΩ 750-V SiC FET specifies a short-circuit withstand time of 5 µs, which is superior to that offered by SiC MOSFETs, according to the vendor.

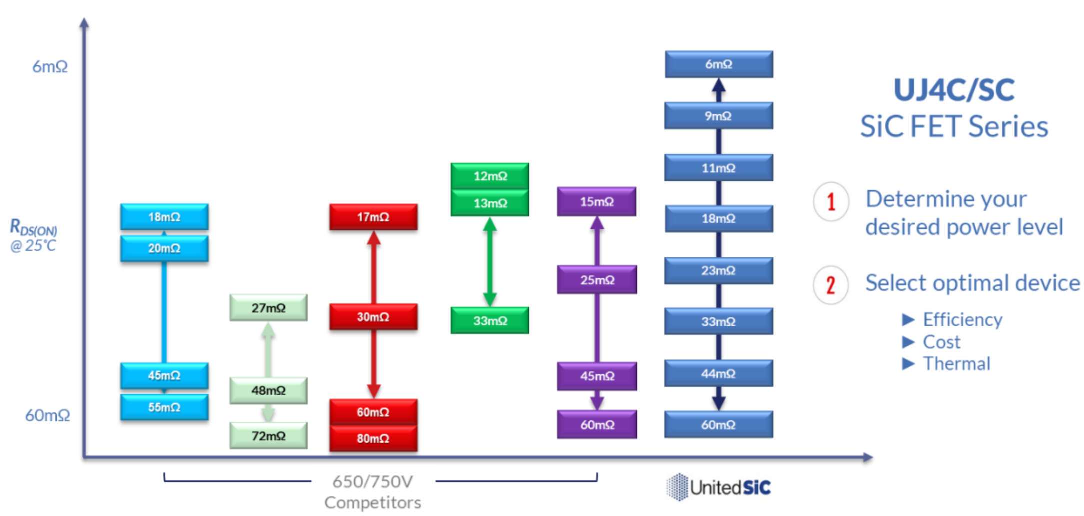

Fig. 3. Comparing $R_{DS(ON)}$ values of United SiC's Gen 4 750-V devices with those of existing SiC MOSFET devices.

Table. Comparing SiC FETs vs. SiC MOSFETs in traction inverters—chip area, losses and junction temperature. Depending on the generation of SiC MOSFETs considered, there may also be a difference in how many devices must be paralleled. A simplified diagram of the inverter is shown below for reference.

Voltage Class	Devices used	No of paralleled FETs	Bus Voltage (V)	Freq(kHz)	Total Chip area all phases(mm2)	Total Semi Loss(W)	TJ (Celsius)
750	G4 SICFET 11m, 750V	7	350	8	462	3579	159
750		9	350	8	594	2287	122
750		11	350	8	726	1753	108
650	G3 SiCMOS 15m, 650V	7	350	8	760.2	2857.5	154
650		9	350	8	977.4	2129.3	125
650		11	350	8	1194.6	1720.6	112
650	G2 SiC MOS 20m, 650V	8	350	8	1032	4007.2	164
650		10	350	8	1290	2825.8	130
650		12	350	8	1548	2254.7	115

Test conditions
- Heatsink temp @ 85°C liquid cooled
- Assume 0.6°C/W adder per chip to fluid TO247 area
- PF=1
- Input power = 200kW
- Bus voltage = 350V