Designing An Open-Source Power Inverter (Part 5): Kilowatt Inverter Circuit Design

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This series has introduced the design objectives, considerations and a proposed circuit architecture for an open-source power inverter dubbed the Volksinverter.[1] It has also analyzed key design choices such as output waveshape selection,[2,4] and explored variations on the proposed two-stage inverter architecture.[3] In the last part, [4] the analysis of waveshape selection led to a discussion of PWM switching techniques that can be applied to the inverter output stage (INV401).

This article delves further into the design of the inverter output stage by presenting a detailed circuit implementation capable of delivering 1.2 kW of output power. The INV401 inverter functional diagram is shown below in Fig. 1 within the system-level block diagram for the Volksinverter. This part 5 specifically explains the design and operation of the gate-drivers, ground fault protection and current sensing and overprotection.

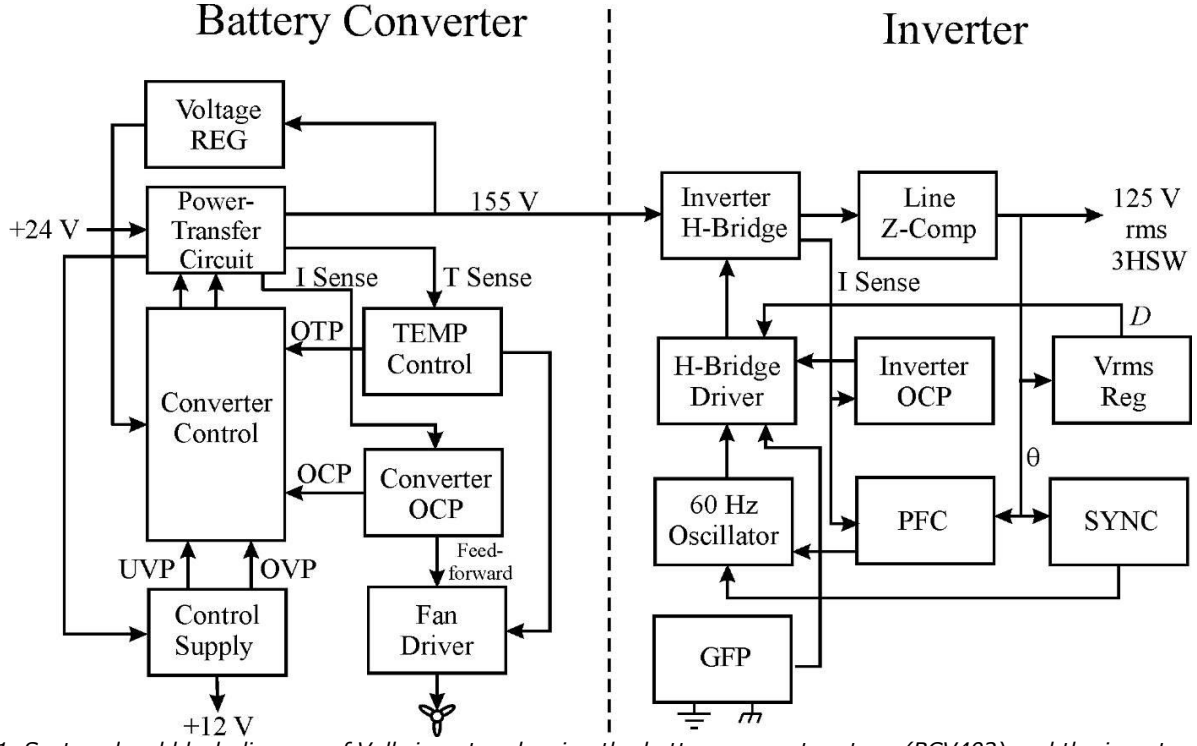

Fig. 1. System-level block diagram of Volksinverter showing the battery converter stage (BCV402) and the inverter stage (INV401). The control & control power supply stage (BCV401) is not included here. This design includes protection functions such as overcurrent (OCP), overtemperature (OTP), undervoltage (UVP), overvoltage (OVP) and ground fault protection (GFP).

Gate Drivers

The circuit diagram of the H-bridge power circuit is shown in Fig. 2. The low-side H-bridge switches, Q1 and Q5 are driven by gate driver IC U9, powered by a 12-V supply for sufficient on-voltage drive to the MOSFETs. The shunt R-D components in series with the gate, R42 and D2 on the N-output side of the bridge, and R43 and D3 cause the low-side MOSFETs to switch on slower than they switch off.

Diodes D2 and D3 provide a low-resistance path for pulling charge out of the gates quickly, while R42 and R43 form an RC integrator with gate capacitance that increases pulse on-edge risetime. This switch delay gives the

high-side switch of the same half-bridge time to shut off before the low-side switch conducts. Otherwise, for both switches to be on while transitioning between their states causes *shoot-through*, a momentary shorting of the bridge supply.

The TC1426 inverting gate drivers (or MC34151) have an output resistance of R_o = 18 Ω. To reach their on threshold voltage of 10 V, Fairchild FDP52N20 MOSFETs must charge their gate charge of Q_{GT} = 50 nC, which corresponds to an input capacitance of C_{in} = 50 nC/10 V = 5 nF. Then the on and off time constants are

$$\tau_{on} = R_G \cdot C_{in} = (620\ \Omega + 18\ \Omega) \cdot (5\,\text{nF}) = 3.2\,\mu\text{s}$$

$$\tau_{off} \approx (18\,\Omega) \cdot (5\,\text{nF}) = 90\,\text{ns}$$

Although the gate R-C integrator increases switching on-time and hence switching loss in the low-side MOSFETs, the switching frequency is the power-line frequency—low enough that switching loss is negligible, leaving conduction loss as the dominant switch loss.

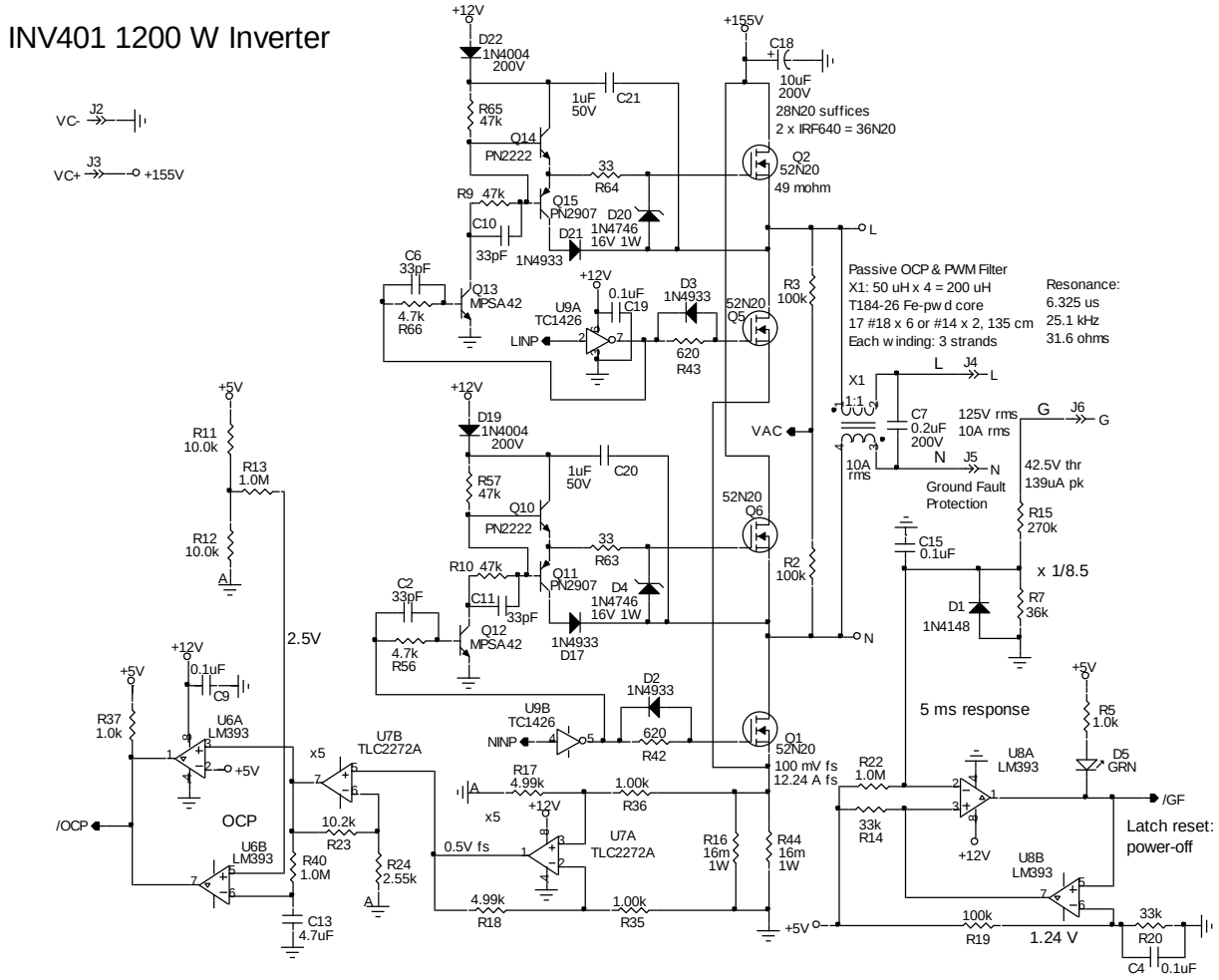

Fig. 2. INV401 inverter power-transfer circuitry. Q1 and Q5 are the H-bridge low-side switches, while Q2 and Q6 are the high-side switches, R16 in parallel with R44 equals R_s, U7 is the current-sense amplifier, U6 is overcurrent protection (OCP) comparator and U8 is ground-fault protection (GFP). X1 is the output common-mode inductor.

The high-side gate drivers are designed with discrete BJTs, though integrated high-side drivers could have been used instead. Q12 and Q13 translate from the low-side gate driver output up to the high-side voltage. When a U9 output goes low, Q12 or Q13 shut off, and Q14 or Q10 conduct, charging the gate capacitance through R63 or R64. D4 or D20 are overvoltage protection of the MOSFET gate-source inputs for both polarities.

When the high-side MOSFET shuts off, charge is removed from C_{GS} by conduction of Q11 or Q15. D17 and D21 prevent forward-biasing of the Q1 and Q14 c-b junctions during a high output undergoing a high-to-low transition. Q12 and Q13 switch on to bring their half-bridge outputs low, but while they are still high, a conduction path otherwise exists through Q11 and Q15 c-b junctions.

The cathodes of diodes D19 and D22 are at V_{GH} and are elevated above +155 V by the voltage across C20 and C21. When the output of the half-bridge is low, C20 or C21 charges through D19 or D22 to V_{GH} = 12 V – $V_D \approx$ 11.2 V. The 52N20 MOSFET gate charge over the total ΔV_G is $Q_G \leq$ 200 nC, or $C_G \leq$ 5 nF. Switching occurs at $f_g \geq$ 50 Hz. For C20 = C21 = 1 µF, the ripple voltage across them is ΔV_{GH} = (50 nC)/(1 µF) = 50 mV, leaving an acceptable V_{GH} = 11.15 V.

The switch-on time constant is thus $\tau_{on} \approx$ (33 Ω)·(5 nF) = 165 ns. Q12 and Q13 are MPSA42A having f_T = 50 MHz at 10 mA and $\beta_0 \approx$ 40. Q10 and Q14 are PN2222A with $\beta_0 + 1 \geq 100$. The on-time and off-time gate currents are

$$I_G(\text{on}) \approx \frac{10\ \text{V}}{47\ \text{k}\Omega} \cdot (100) = 21.3\ \text{mA} \Rightarrow t_{sw}(\text{on}) \approx \frac{(10\ \text{V}) \cdot (5\ \text{nF})}{21.3\ \text{mA}} = 2.35\ \mu\text{s}$$

$$I_G(\text{off}) \approx \frac{155\ \text{V}}{47\ \text{k}\Omega} \cdot (100) = (3.30\ \text{mA}) \cdot (100) = 330\ \text{mA}$$

However, at switch-off, Q11, R63, and D17, and also Q15, R64, and D21, are the paths discharging gate-source capacitance, limited to a discharge current of

$$I_G \geq [V_{GS}(\text{on}) - V_D]/R_G = 9\ \text{V}/33\ \Omega = 0.27\ \text{A} \Rightarrow t_{sw}(\text{off}) \leq (50\ \text{nC})/(0.27\ \text{A}) = 185\ \text{ns}$$

Thus, t_{sw}(on) << t_{sw}(off) and there is no H-bridge shoot-through current.

Ground-Fault Protection

The power-line third wire for the safety ground is marked G and reduces its voltage relative to the inverter system ground by ×1/8.5. Op-amp U8A forms a bistable circuit with U8B. At power-on, R5 to +5 V pulls the U8B noninverting (+) input high, driving the output high, pulled up to 5 V by R14. R22 also pulls the input of U8A up to +5 V, but more slowly because of C15 and the large value of R22.

A ground fault occurs when green-wire current exceeds 140 µA peak. It drops 42.5 V across input divider resistance R15 and R7, and then the U8A inverting input exceeds the 5 V of the U8B output, causing the U8A output to change state to near 0 V. The U8B inverting input is fixed at 1.24 V by divider R19 and R20, and its output is also driven low, sustaining U8A in a low output state, even when the ground fault is removed. The only way to reset the inverter from a ground fault is to recycle its power.

At power-off, the GFP latch is reset. This is intentional because a ground fault is a serious safety event that requires powering down the inverter as an electric source to correct it. The threshold value of 42.5 V was the UL safety standard for the boundary between safe and unsafe voltages until 48-V batteries came into vogue and the human body evolved quickly to accommodate a higher safe voltage.

This threshold can be placed lower for greater safety margin. The lower its value, the more likely that false GFP events will occur, requiring power recycling. The output of U8A is the ground-fault line, /GF to the INV401 system fault bus line and /FAULT which disables the converter.

Current Sensing And Overcurrent Protection

The H-bridge current-sense resistors R16 and R44 are two parallel 16-mΩ (12 mΩ in this prototype) manganin-wire resistors that drop 100 mV at the full scale peak current of 12.24 A. This voltage is sensed differentially by a one-op-amp diff-amp, U7A from input resistors R35 and R36. The sense resistors are shown in the partial view of the circuit-board in Fig. 3.

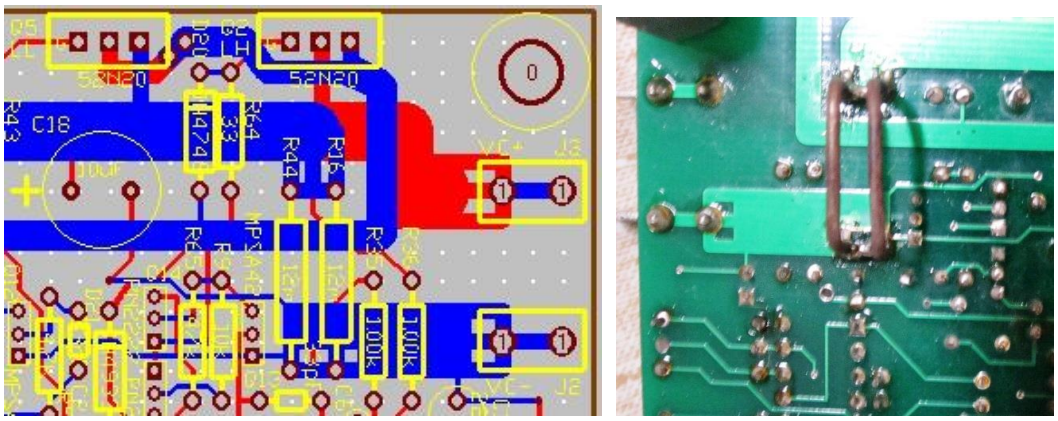

Fig. 3. In the partial top side view of the board layout (left), traces on both sides (red = top, blue = bottom) of the input connections (VC±) on the right side of the INV401 circuit-board carry the H-bridge current through sense resistors R16 and R44. The bottom view of the board (right) shows the attached (12-mΩ) manganin-wire sense resistors R16 and R44 in parallel.

Fig. 4 shows a topside view of the full INV401 circuit-board layout. The board layout shows the four-terminal drive-sense scheme. The op-amp input resistors R3 and R36 input the voltage across R16 and R44 from traces that connect to the centers between the R16 and R44 terminals to avoid sensing across parasitic series resistance from the power traces.

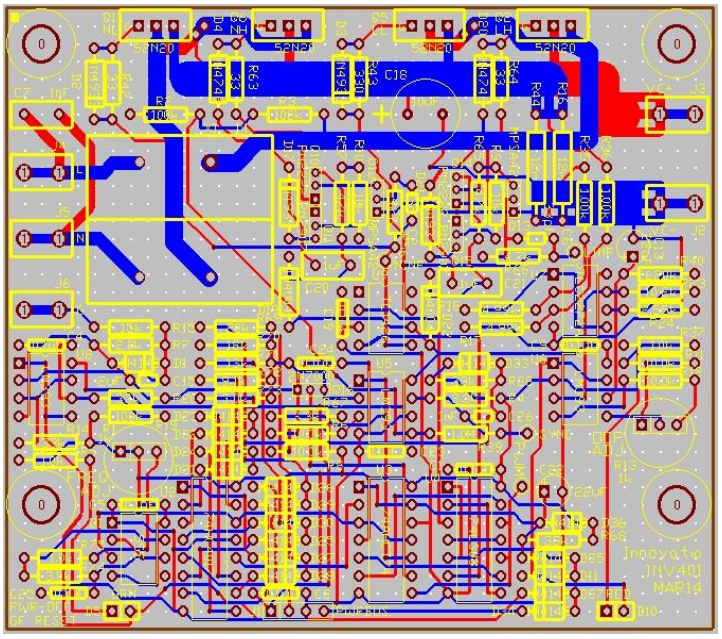

Fig. 4. Full top side view of the INV401 circuit-board layout. In this drawing the screen print is in yellow; the top layer copper is red; the bottom layer, blue; and the brown layer shows the board boundary and vias. Board dimensions are 3 in. × 5 in. Mounting holes are placed to stack 3-in. × 4-in. boards.

The one-op-amp diff-amp, U7A has a gain of ×5, followed by a noninverting single-sided op-amp, also with a gain of ×5. The return of the op-amp input loop—the bottom of R24—is to analog ground, a ground kept as free as possible from other currents that introduce voltage error into the loop. The ground traces for R17, R24, and C13 connect near the sense-resistor ground node by J2 (VC–) on the layout in Fig. 4 and nowhere else.

Overcurrent protection (OCP) has three protection time intervals:

1. Passive—0 to 3 µs, during which the OCP active circuits have yet to respond and provide no protection;
2. Transient—3 µs to 1 s, during which the active OCP loop limits the current to I_{tr};
3. Thermal—>1 s, during which the active OCP loop limits current to the acceptable steady-state value of I_{ss}.

During the passive protection interval, the power circuit must protect itself from failure. Protection is provided by X1, the output transductor between the H-bridge and power-line output. In steady-state (or *continuous*) operation, the ideal output parameters of X1, as specified or calculated, are

- $\tilde{v}_o(\text{nom}) = 125\ \text{V}$ and $\hat{v}_o(\text{nom}) = 155\ \text{V}$
- $\tilde{i}_o(\text{max}) = 10\ \text{A}$ and $\hat{i}_o(\text{max}) = 12.24\ \text{A}$
- $\overline{P}_o(\text{max}) = 1250\ \text{W}$ and $\hat{P}_o(\text{max}) = 1875\ \text{W}$.

The first interval depends on X1 for protection and X1 also provides the line interface. U6 and U7 comprise the active OCP; U6A has a fast, second-interval response that can effect protection as quickly as the OCP circuits allow. U6B has a lower current threshold and controls the thermal response of the third interval (see Fig. 5).

R2 and R3 sense the output waveform and feed it back (as Vac) for detection of zero-crossings, to synchronize the INV401 with the power-line if it is already being driven by another source. X1 is a coupled inductor that, along with C7, both filters out higher-frequency harmonics from PWM of the 3HSW and provides an impedance interface between the H-bridge output and a possibly reactive power-line. Its third function is to limit *di*/*dt* during power-line shorts causing overcurrent events, to give the active OCP time to shut off the H-bridge. As can be seen from a photo of an INV401 in Fig. 6, the prototype has an imposing inductor.

The addition of X1 accrues additional cost to the design and is not found in low-cost cut-rate inverters. This is one of the reasons they are characteristically unreliable. Under some conditions, transient load current can exceed the operational limits of the power switches and failure in them occurs.

No electronic solution exists except to provide very fast analog amplifier and comparator circuitry. Not only does this add to the cost with its wider bandwidth, it is difficult in a power circuit to keep switching noise from interfering with circuits sensing relatively small voltages quickly. Consequently, the passive inductive component was chosen as a better alternative because it is not noise-sensitive, is not prone to fail from transient overcurrent, and provides a second function of matching the H-bridge to the power distribution line interface.

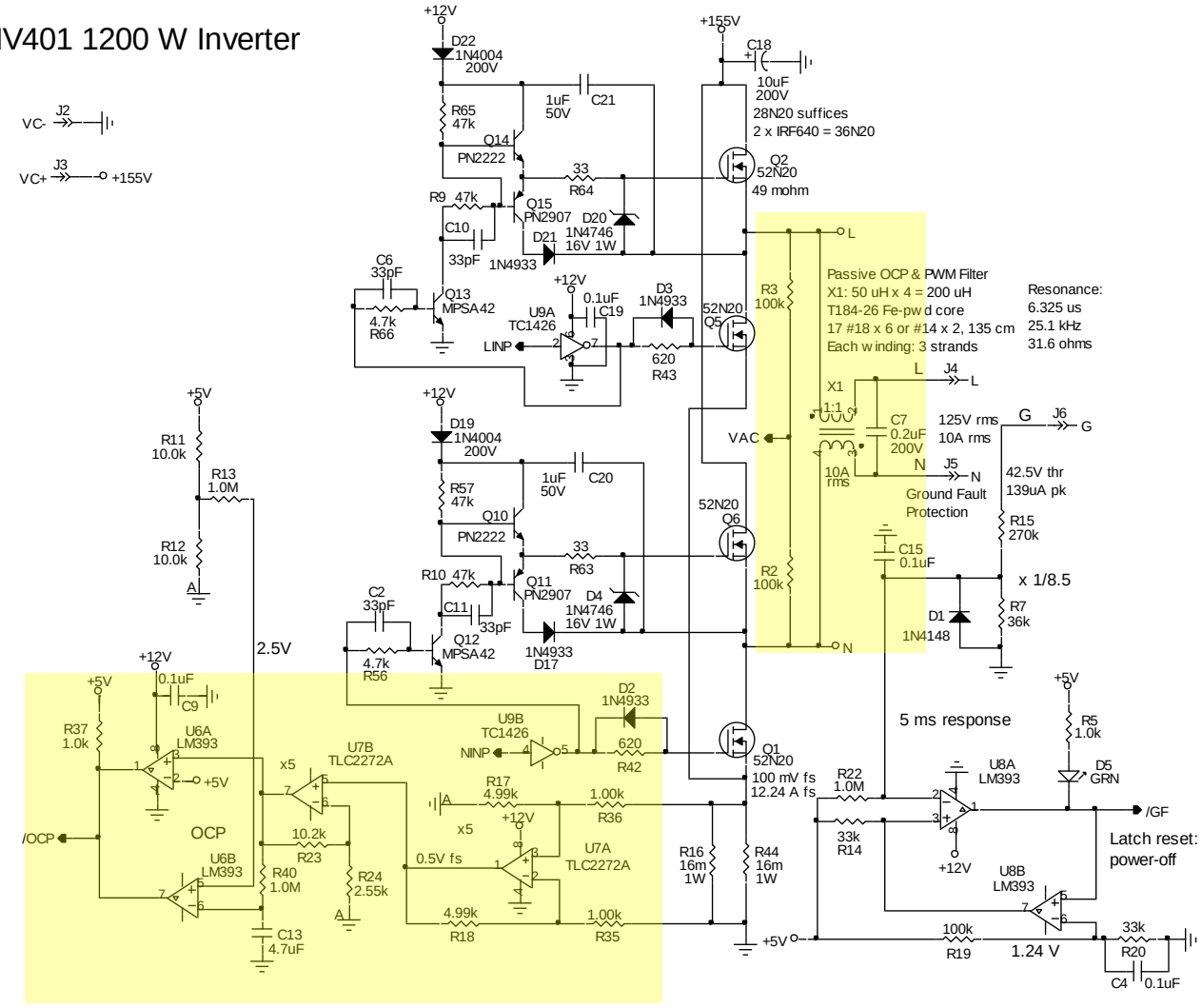

Fig 5. INV401 inverter power-transfer circuitry with protection circuitry highlighted.

During the passive first OCP interval, the circuit of Fig. 7 applies to the transient analysis. The worst case of peak current occurs when the output waveform is at its peak and a load short occurs. The passive OCP time delay is t_{cd} and is set for the OCP circuits at $t_{cd} \leq 3$ µs. The worst-case output voltage when the load fault occurs is at the 3HSW peak of 155 V corresponding to 12.24 A. The worst-case (maximum) fault current is chosen to be 25 A. It occurs when the load is shorted at the moment of the peak output current, or

$$\hat{i}_{cd} = \hat{i}_o(\max) + \Delta i_{cd} = 12.24\ \text{A} + 12.76\ \text{A} = 25\ \text{A}$$

Then the output inductor must have a minimum inductance to constrain i_{cd} to Δi_{cd} = 12.76 A of

$$L \geq \frac{\hat{v}_o(\max) \cdot t_{cd}}{\Delta i_{cd}} = \frac{(155\ \text{V}) \cdot (3\ \mu\text{s})}{12.76\ \text{A}} = 36.44\ \mu\text{H}$$

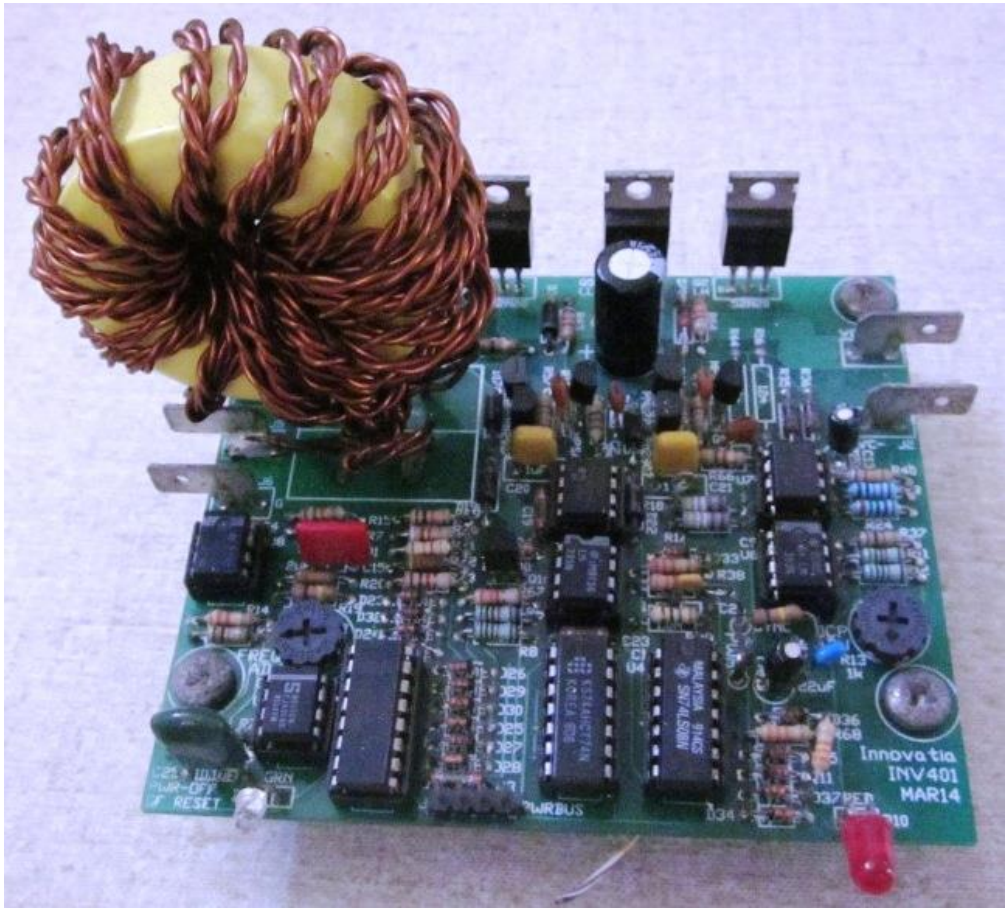

Fig. 6. Top view of a prototype INV401 circuit-board. QDCs input 155 V on the right and output to the power-line L and N nodes on the left. LEDs indicate GFP and OCP faults. The large output inductor needs to be mechanically mounted more securely in a succeeding iteration of the board design and also shrunk. The BCV401 supplies control supplies, +12 V, +5 V and the fault bus, /FAULT through the four-pin square-pin connector on the front edge. The power MOSFETs are along the rear of the board where they can be attached to a heat sink.

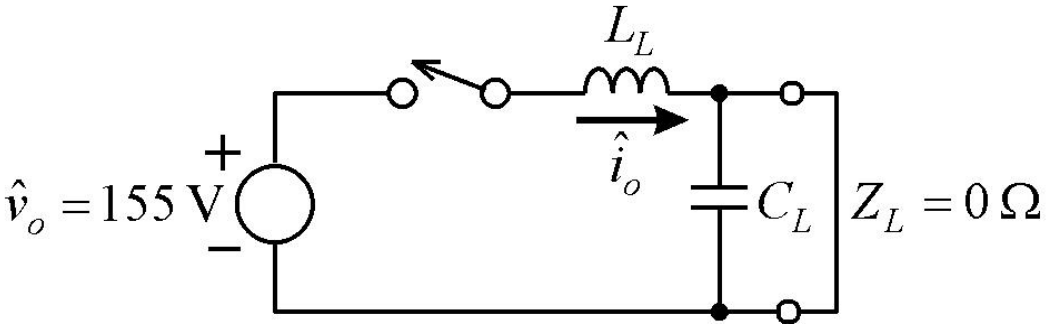

Fig. 7. Transient response of the passive OCP output circuit, where X1 has magnetizing inductance, L_L. The output is shorted for worst-case peak current response. Peak allowable current is chosen to be $\hat{i}_o \le 25\ \mathrm{A}$.

At the full-scale (fs) output values, the inverter power-circuit output resistance is a minimum of

$$Z_L \geq \frac{155\,\text{V}}{12.24\,\text{A}} = 12.66\,\Omega$$

For f_g = 60 Hz, the X1 inductance, L_L and C_L = C7 values at a reactance of the minimum Z_L must be

$$C_L << \frac{1}{\omega_g \cdot Z_L} = \frac{1}{(377\,\text{s}^{-1}) \cdot (12.66\,\Omega)} = 206\,\mu\text{F} \;\; ; \;\; L_L << \frac{Z_L}{\omega_g} = \frac{12.66\,\Omega}{377\,\text{s}^{-1}} = 33.6\,\text{mH}$$

To minimize filter attenuation of output power, L_L and C_L are chosen as ≤0.1% of the above limit value. Then C_L = 0.2 µF and $X_C(\omega_g)$ = 13.3 kΩ. Minimum L_L is constrained so that $L_L \geq$ 36.44 µH. Choose L_L = 40 µH at 25 A. Then $X_L(\omega_g)$ = 15.1 mΩ. The voltage drop across L_L at ω_g = 377 s^{-1} is $v_L(\omega_g)$ = 0.185 V peak. The LC resonance is

$$Z_n = \sqrt{\frac{L_L}{C_L}} = 14.14\,\Omega \;\; , \;\; \tau_n = \sqrt{L_L \cdot C_L} = 2.83\,\mu\text{s} \;\Rightarrow f_n = 1/2{\cdot}\pi{\cdot}\tau_n = 56.3\ \text{kHz}$$

The two windings of the X1 transductor have polarities that aid as a coupled inductor with L_L/4 per winding, forming an output filter. The LC filter has transfer function,

$$M(s) = \frac{v_o}{v_i} = \frac{1/s \cdot C}{s \cdot L + 1/s \cdot C} = \frac{1/s \cdot C}{Z_i(\text{oc})} = \frac{1}{s^2 \cdot L \cdot C + 1} = \frac{1}{(s/\omega_n)^2 + 1}$$

The $M(j{\cdot}\omega)$ magnitude has a break frequency at f_n and rolls off at a log-log slope of −2 with possible peaking at f_n. The LC filter input and output impedances are

$$Z_i(\text{oc}) = s \cdot L + 1/s \cdot C = -j \cdot X_C / M(j \cdot \omega) \;\; ; \;\; Z_o(\text{sc}) = s \cdot L \,||\, (1/s \cdot C) = \frac{s^2 \cdot L \cdot C + 1}{s \cdot C} = j \cdot X_L \cdot M(j \cdot \omega)$$

The input impedance is with the output open-circuited (no load) and the output impedance into the LC filter output is with the input short-circuited as a voltage source. The converter output storage capacitor, C_s has, because of PWMing of the converter power circuit, an effective capacitance from the inverter output of C_s/D' >> C and is approximately a voltage source with no series resistance.

Now that we know the component values of the output filter, we can proceed to the inductor design. But before we do that, the control circuit that generates the 3HSW will be described in the next part.

References

1. "Designing An Open-Source Power Inverter (Part 1): Goals And Specifications" by Dennis Feucht, How2Power Today, May 2021.
2. "Designing An Open-Source Power Inverter (Part 2): Waveshape Selection" by Dennis Feucht, How2Power Today, September 2021.
3. "Designing An Open-Source Power Inverter (Part 3): Power-Transfer Circuit Options" by Dennis Feucht, How2Power Today, April 2022.
4. "Designing An Open-Source Power Inverter (Part 4): The Optimal Power-Line Waveshape" by Dennis Feucht, How2Power Today, May 2022.
5. "Improving Reliability Of Low-Cost Power-Source Inverters" by Dennis Feucht, How2Power Today, October 2020.

About The Author

Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

For further reading on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC power inverters."