Designing An Open-Source Power Inverter (Part 6): Kilowatt Inverter Control Circuits

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In the most recent installment of this series,[1-5] the design of the inverter output stage for a 1.2-kW output was explained. That part 5[5] focused on the gate drivers and protection circuitry. Here in part 6, discussion of the inverter stage design continues as the control circuits driving the power-transfer circuit are described.

The control circuit diagram for the inverter stage is shown in Fig. 1. Its three functions are generation of the third-harmonic sine-wave (3HSW), fault protection (in conjunction with the circuitry described in part 5), and synchronization with an existing output waveform.

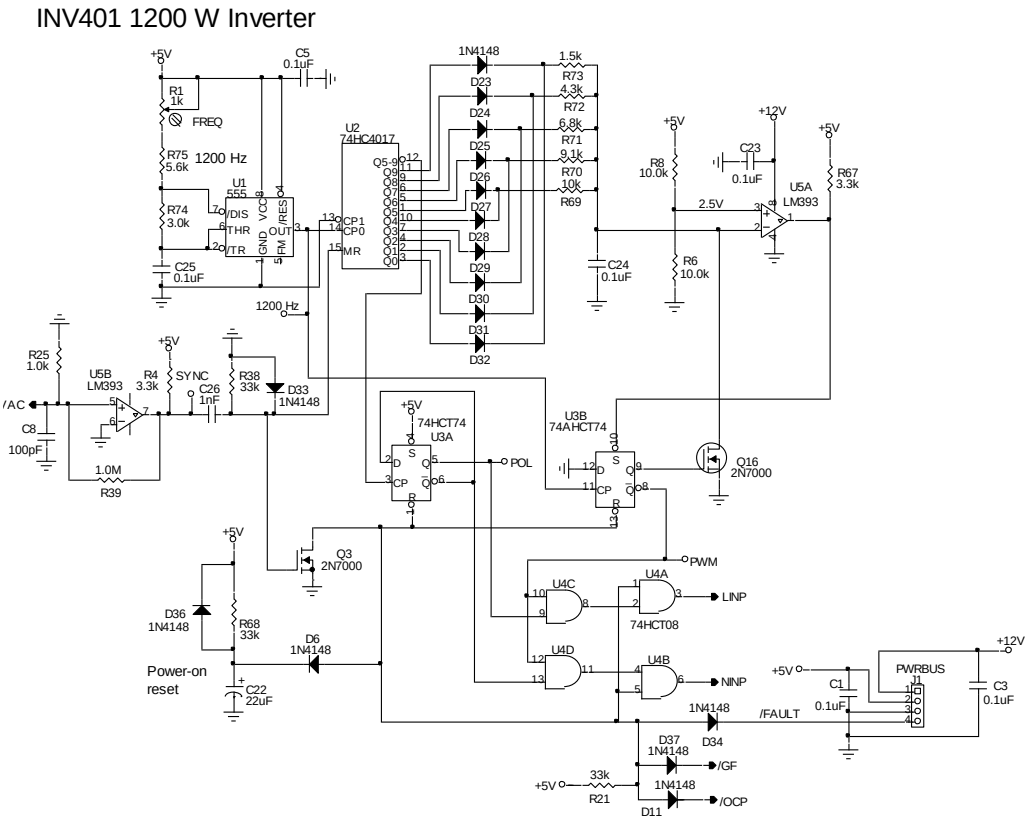

Fig. 1. INV401 inverter control circuitry. U1 is the 1200-Hz source from which 20 segments of the 60-Hz output waveform are generated by U2, diodes, U3, Q16 and U5A. U5B synchronizes 3HSW generation to the power-line for paralleling multiple INV401 modules; U4 and diodes generate H-bridge PWM drive and shut off drive for faults.

Control Circuit Design

The clock generator driving waveform synthesis is a 555 timer. A functional diagram of the 555 timer is shown in Fig. 2. In the INV401, it functions as an astable timer (AST).

C25 charges through R1, R75, and R74 until the THR threshold of $\frac{2}{3}\cdot V_{CC} \approx 3.33$ V is reached, the comparator changes state to high and the NOR-gate RS flop is flipped. OUT goes low, /DIS pulls low and discharges C25 through R74. When the exponential sawtooth waveform on C25 decreases to $\frac{1}{3}\cdot V_{CC} \approx 1.67$ V, the TRIG

comparator output changes high, the RS flop changes state, OUT goes high and /DIS becomes open, allowing C25 to once again charge. The circuit oscillates at 1200 Hz.

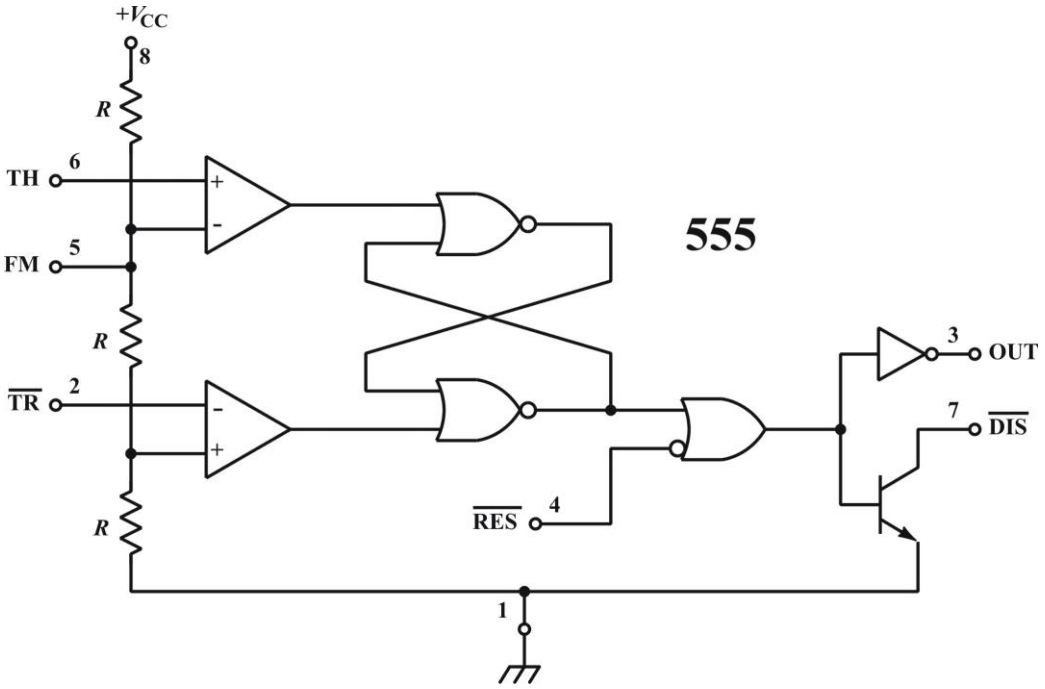

Fig. 2. The venerable 555 timer. Its functional diagram is inexplicably absent from part specifications. The pin 7 /DIS output is open-collector (high level open node) and pulls down to ground for the low level, in phase with OUT. CMOS 555s have higher values of R but for all 555s, the FM pin is at ⅔·V_{CC} and the trigger threshold is at ⅓·V_{CC}.

The design formulas for the AST are

$$t_{on} = (0.693)\cdot(R_U + R_L)\cdot C_T \;;\; t_{off} = (0.693)\cdot(R_L \cdot C_T) \;;\; T_s = t_{on} + t_{off} = (0.693)\cdot(R_U + 2\cdot R_L)\cdot C_T \;;\; f_s = 1/T_s$$

where R_U = R1 + R75, R_L = R74, and C_T = C25. Set R_L = 3.0 kΩ, C_T = 0.1 µF, and $T_s = 1/f_s$ = 833.3 µs. Then

$$R_U = \frac{T_s}{(0.693)\cdot C_T} - 2\cdot R_L = 6.02\,\text{k}\Omega = 500\ \Omega + 5.6\ \text{k}\Omega$$

where 500 Ω is the mid-scale setting of R1 = 1 kΩ. Resistors are 5% tolerance. The duty-ratio, $D \geq 0.5$ and is

$$D = \frac{t_{on}}{T_s} = \frac{R_U + R_L}{R_U + 2\cdot R_L} = \frac{9.02\,\text{k}\Omega}{12.02\,\text{k}\Omega} = 0.75$$

The U1 output drives U2. U2 is a counter driving 1 of 10 decoder logic. Only one of the 10 outputs of the 74HC4017 is high at any one time. The high output diode—one of D23 through D32—conducts, placing 5 V minus a diode drop on the top side of a timing resistor (R69 through R73). Its timing current charges C24 exponentially.

When the C24 voltage reaches 2.5 V, set by the divider, R8 and R6, the U5A comparator changes state, setting U3B D flop through its RS-flop input at /S to high. Q16 is switched on and C24 is discharged. The /Q output of the U3B D flop is a PWM waveform that drives the U4 gates.

This circuitry, on the upper-right of Fig. 1, repeated below in Fig. 3, is a PWM generator. The pulse width is proportional to the value of the 3HSW over each half of the waveform. When the U2 counter overflows, it outputs an edge at Q5-9 (pin 12) that clocks U3A, a D flop configured to alternate its output state every clock. Its state, POL is the half-cycle polarity of the inverter output waveform.

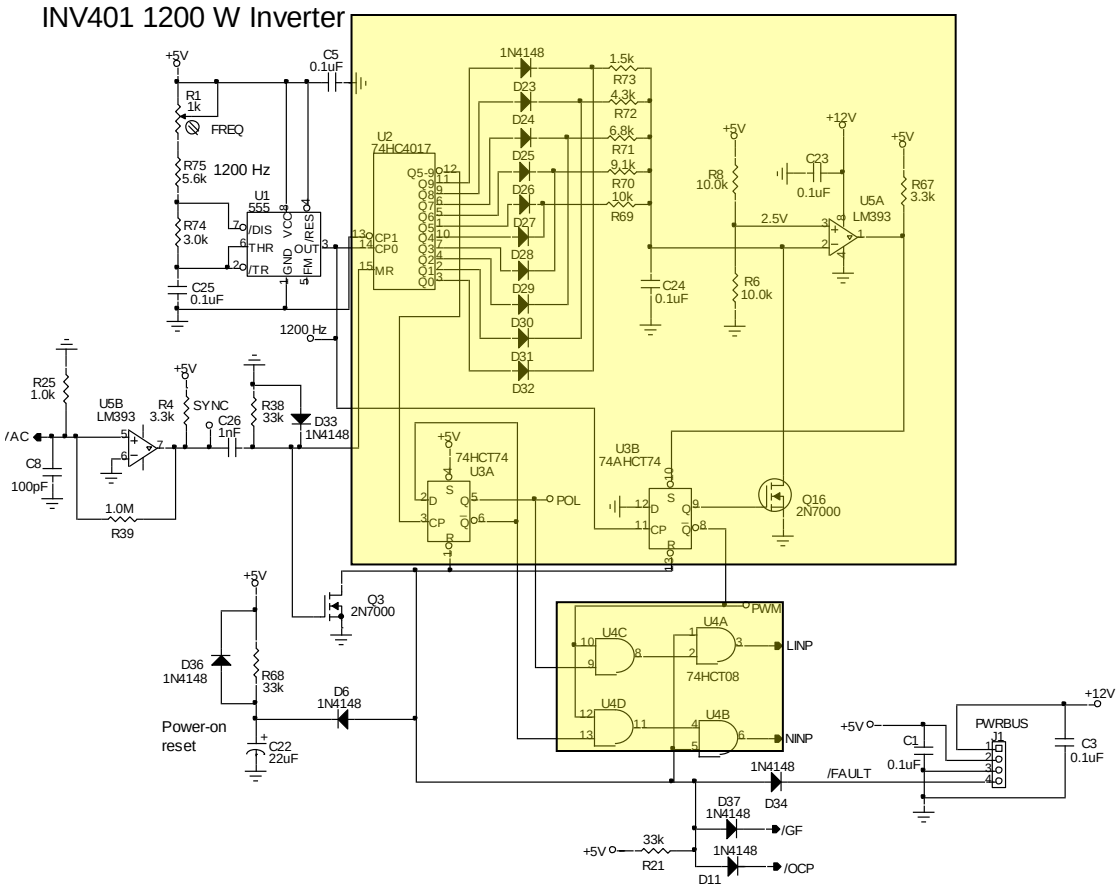

Fig. 3. INV401 inverter control circuitry with PWM generator components highlighted.

POL and /POL (from U3A /Q) select U4C and U4D to pass PWM to either the left or right half-bridge driver. U4A and U4B gate both drivers off if a fault occurs. /FAULT is the system fault bus that combines the faults from both inverter (INV401) and converter control (BCV401) to shut both down when a fault occurs. Diode OR logic is implemented with R21 and diodes D11, D34 and D37. D11 and D37 combine the OCP and GFP faults of the inverter; D34 includes the /FAULT bus from the converter.

Inverter power is scaled up by paralleling INV401 modules. To connect INV401 outputs in parallel, they must all be synchronized to the same phase. (In small electric power plants, this is done manually by connecting a light bulb between the power-line and the generator, and when the bulb goes off, the generator is switched onto the line.)

The output voltage to the power-line is sensed differentially as VAC across the L and N nodes by R2 and R3, which appear in the INV401 inverter power-transfer circuitry schematic from part 5, repeated here as Fig. 4.

They form a resistive divider with R25 (in the INV401 inverter control circuitry, repeated again in Fig. 5) for an approximate /100, with nominal 1.5-V peaks at the U5B comparator input. U5B senses the line output zero-crossings. Some hysteresis is applied by R39 for a single-edge output—a "clean" change of states. The active edge of interest is the edge corresponding to zero phase of the generated waveform—the positive (low-to-high)

edge, which is differentiated by C26 and R38 for a momentary pulse to the MR input of the counter in U2, and which also drives Q3 on and resets U3.

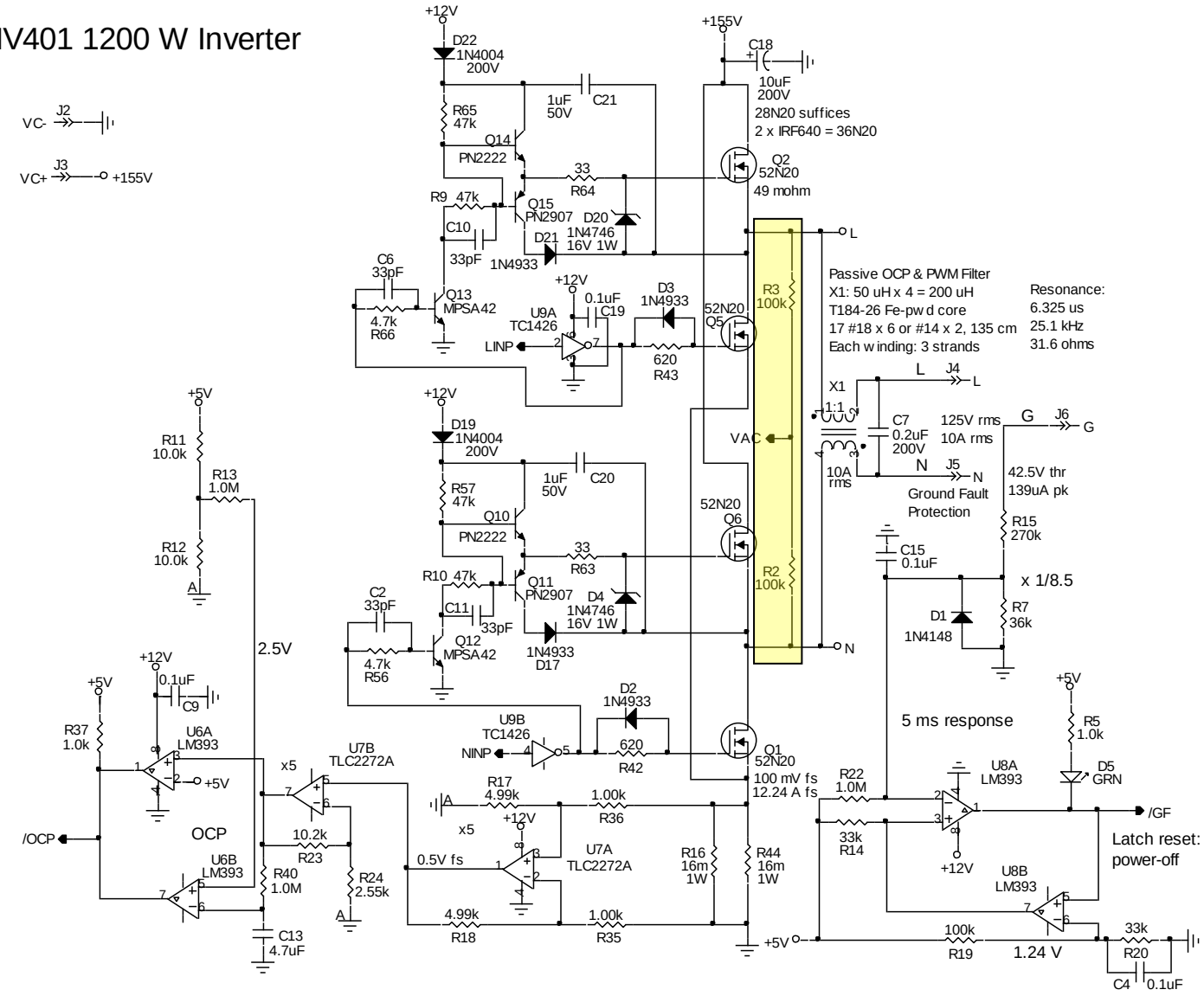

Fig. 4. INV401 inverter power-transfer circuitry. The inverter output voltage is sensed differentially as VAC across the L and N nodes by R2 and R3.

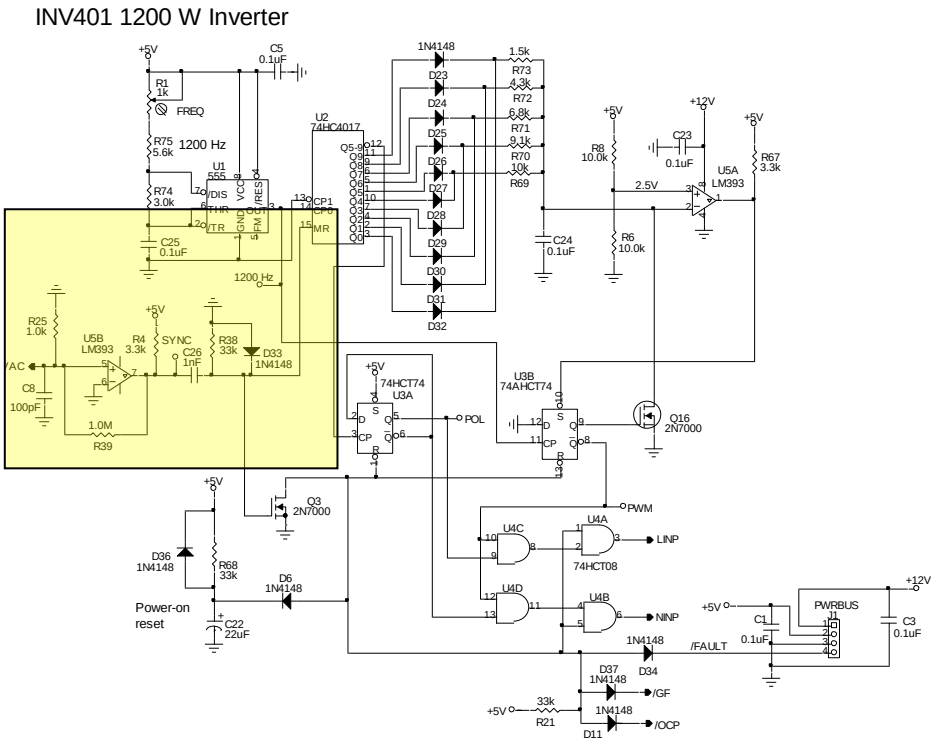

Fig. 5. INV401 inverter control circuitry with components used for detection of line-output zero-crossings highlighted.

Diode D33 is the quick recharge path for C26 when U5B output goes low. Thus, when the power-line waveform crosses zero phase, the 3HSW generator is reset to its zero-phase counter state. Both the half-cycle phase of U2 and its polarity, POL of U3A, are set to the zero-phase state of the output 3HSW.

Before this sync circuit can reset for the correct phase, a partial cycle can be out of phase and cause excessive current in the H-bridge. If this occurs, the OCP circuit causes all paralleled INV401s to shut off through their fault buses. Both low-side H-bridge switches are switched on, high-side switches shut off, and the L and N outputs remain at the inverter ground state until the fault is cleared and all INV401s are reset to the beginning of the cycle. At power-on, the reset circuit, R68 and C22 in the lower left corner of Fig. 5, resets the U3 flops. All INV401s are reset concurrently through the fault bus.

Ideally, synchronization is eliminated by scaling the INV401 as the BCV402 is scaled, by partitioning the INV401 into separate waveform-generation and power-transfer circuits. Then all power-transfer circuits are driven with the same waveform and are inherently in phase. The simplest way to achieve this is by scaling the MOSFETs and sense resistors. Then the synchronization circuit is superfluous. It can, however, be used in a cogeneration application, but that is beyond the scope of the Volksinverter series.

3HSW Waveform Design

For 60-Hz output and the 10 intervals, or *steps* of U2 per half-cycle, or 5 per quadrant, five timing-resistor values, R_T (R69 through R73), must be determined. The PWM generator outputs a pulse with duty-ratio, D proportional to the output waveform voltage. Choose C_T = C24 = 0.1 µF, a convenient decade value. The PWM generator RC timing charges C_T toward the target voltage of $V_{CC} - V_D \approx 4.35$ V, where $V_D \approx 0.65$ V is the on-voltage of the diodes in series with R_T. The PWM comparator threshold is set at 2.5 V. Then

$$t_{on} = -R_T \cdot C_T \cdot \ln\left(1 - \frac{2.5\,\text{V}}{4.35\,\text{V}}\right) \Rightarrow R_T = \frac{t_{on}}{(0.8850)\cdot C_T} = \frac{D \cdot T_s}{(0.8850)\cdot C_T} = (9.747\ \text{k}\Omega)\cdot D$$

Now that we have a formula for calculating the values of R_T, we need the values of D corresponding to the chosen waveshape. The 3HSW waveshape values for D are found as a modification of the values of a sine-wave. With five steps per quartile, the stepped (or *piecewise-linear*) approximation of a sine-wave is shown in Fig. 6.

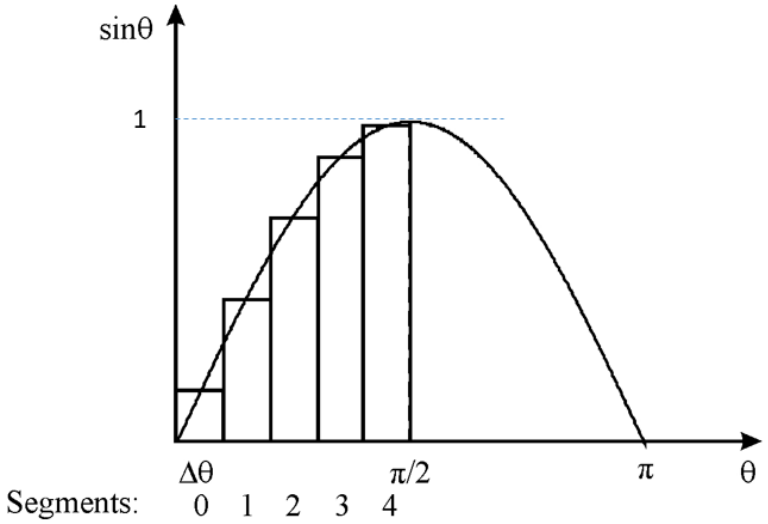

Fig. 6. Sine waveshape approximation by 5 regular intervals, or steps in the first quadrant. The two positive quadrants have even symmetry around the peak, and steps 5 through 9 have the same values as steps 4 through 0. The negative half-cycle has the same magnitude of waveform but with opposite polarity. By symmetry, only one quadrant need have timing R_T for D to be generated.

In Fig. 6, segments are numbered n = 0, 1, 2, …, N – 1, each with a width of

$$\Delta\theta = \frac{\pi/2}{N}$$

The value of a segment is the average value of the waveform between n and n + 1. For $y(\theta)$ = sinθ, the average is

$$\bar{y}(n) = \frac{1}{\Delta\theta} \cdot \int_{n\cdot\Delta\theta}^{(n+1)\cdot\Delta\theta} \sin(\theta) \cdot d\theta = \frac{2 \cdot N}{\pi} \cdot \left[\cos\left(\frac{\pi}{2} \cdot \frac{n}{N}\right) - \cos\left(\frac{\pi}{2} \cdot \frac{n+1}{N}\right) \right]$$

For N = 5, Table 2 lists the values of $\bar{y}(n)$.

Table 2. Values of steps for sine and 3HSW approximation, D and R_T values

∠, deg	n	$\bar{y}(n)$, D	3HSW(n), D	sine R_T, Ω	sine R_T, kΩ 1%, 5%	3HSW R_T, Ω
0, 18	0, 9	0.1558	0.1558	1519	1.50, 1.5	1519
18, 36	1, 8	0.4521	0.4521	4408	4.42, 4.3	4408
36, 54	2, 7	0.7042	0.7042	6866	6.81, 6.8	6866
54, 72	3, 6	0.8874	0.8874	8652	8.66, 9.1	8652
72, 90	4, 5	0.9836	0.8874	9590	9.53, 10	8652

The only difference between a five-step approximation of a sine-wave and a 3HSW-wave is that the 3HSW step is flattened to be equal to the fourth sine step. Therefore, the only change in the circuit between sine and 3HSW is the value of R69, which is 10 kΩ for a sine waveform and 9.1 kΩ, 5% for a 3HSW waveform. The two values could be jumpered for selection while heeding the caveat that a sine waveform requires an up-scaled inverter H-bridge and 170-V input instead of 155 V from an also up-scaled converter.

At the zero-crossings, a change of $2 \cdot \Delta\, \bar{y}(n)$ occurs, or (normalized) about $2 \cdot (0.1558) \approx 0.3116$. This "edge" of the zero-crossing step is large enough to definitively change the state of comparator U5B for synchronization. This is the largest step change of the waveform. At reset of the waveform generator, however, the output will not be 0 V but the value of the first (n = 0) step. The step from n = 0 (or 9) to 1 (or 8) is 0.4521 – 0.1558 = 0.2963, not quite as large as the zero-crossing step. The other steps are smaller as the waveform slope decreases.

References

1. "Designing An Open-Source Power Inverter (Part 1): Goals And Specifications" by Dennis Feucht, How2Power Today, May 2021.
2. "Designing An Open-Source Power Inverter (Part 2): Waveshape Selection" by Dennis Feucht, How2Power Today, September 2021.
3. "Designing An Open-Source Power Inverter (Part 3): Power-Transfer Circuit Options" by Dennis Feucht, How2Power Today, April 2022.
4. "Designing An Open-Source Power Inverter (Part 4): The Optimal Power-Line Waveshape" by Dennis Feucht, How2Power Today, May 2022.
5. "Designing An Open-Source Power Inverter (Part 5): Kilowatt Inverter Circuit Design" by Dennis Feucht, How2Power Today, July 2022.
6. "Improving Reliability Of Low-Cost Power-Source Inverters" by Dennis Feucht, How2Power Today, October 2020.

About The Author

Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

For further reading on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC power inverters."