ISSUE: November 2022

Designing An Open-Source Power Inverter (Part 8): Converter Control Power Supply

by Dennis Feucht, Innovatia Laboratories, Cayo, Belize

Having delved into the design of the inverter stage circuitry and its magnetics in recent installments in this series,[1-7] this article now turns its attention to another stage of the Volksinverter—the converter control power supply. As a converter controller, the BCV401 has its own 24-V-input switching supply that outputs +12 V to control circuits (Fig. 1).

The control power supply is a minimal-parts switching converter using generic components. The operation of this switching power supply will be described in the first section of this article and a prototype will be presented.

This converter uses hysteretic control, primarily in continuous conduction mode except at very light loading. In the second half of this article, hysteretic control will be explained and design equations for parameters such as output voltage ripple, inductance, and switching frequency will be given. Finally, measurements will be shown that reveal the effects of loop delay on output ripple and switching frequency, while also confirming that the prototype waveforms are in harmony with the derived waveforms.

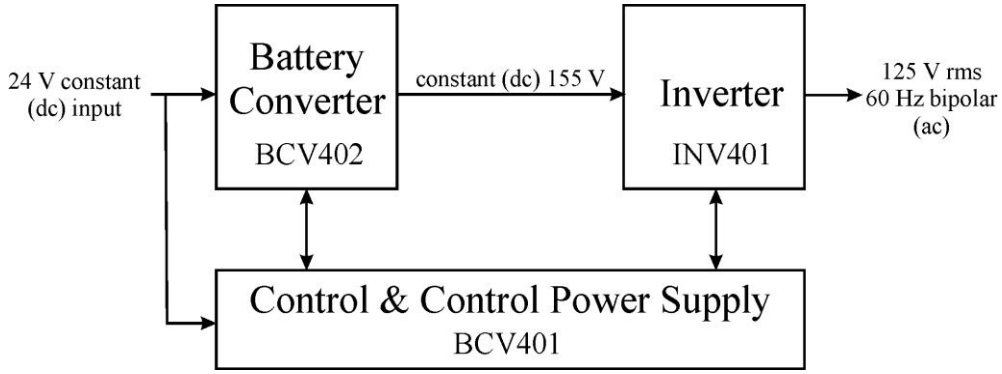

Fig. 1. The Volksinverter described in this series contains a separate stage—the control & control power supply stage, BCV401—for generating control signals and the +5-V and +12-V power rails for the control circuits. This part of the series discusses the design of the control power supply.

Power Supply Design

The 24-V to 12-V switching supply has a common-passive (CP or buck) power-transfer circuit as shown in Fig. 1. It is designed for an input voltage range of VBAT = $V_g \in$ [20 V, 30 V]. The load specification of the Volksinverter boards is

BCV401: +5 V at 25 mA, +12 V at 132 mA

BCV402: +5 V at 0 mA, +12 V at 1 mA

INV401: +5 V at 15 mA, +12 V at 15 mA

Then for 2-kW scaling, one BCV401, four BCV402, and two INV401 boards have a demand of

+5 V at 55 mA, +12 V at 166 mA

The 5-V supply is a linear supply based on U3, a TL431 IC shown with internal expansion in Fig. 2. This three-pin part is common in the industry and has a stable bandgap reference of 2.5 V that drives a comparator with

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an npn-output BJT Q1. The supply for both comparator and output are the same TL431 pin, and this must be recognized when designing with the part.

External BJT Q1 buffers the voltage output of U3, and the R7-R8 divider feeds back from the +5-V output, designed to supply 40 mA—enough for the 5-V control logic and to start the +12-V supply. R11 reduces Q1 power dissipation at 30-V input. It reduces efficiency, but the 5-V supply is low-power and not much power is lost.

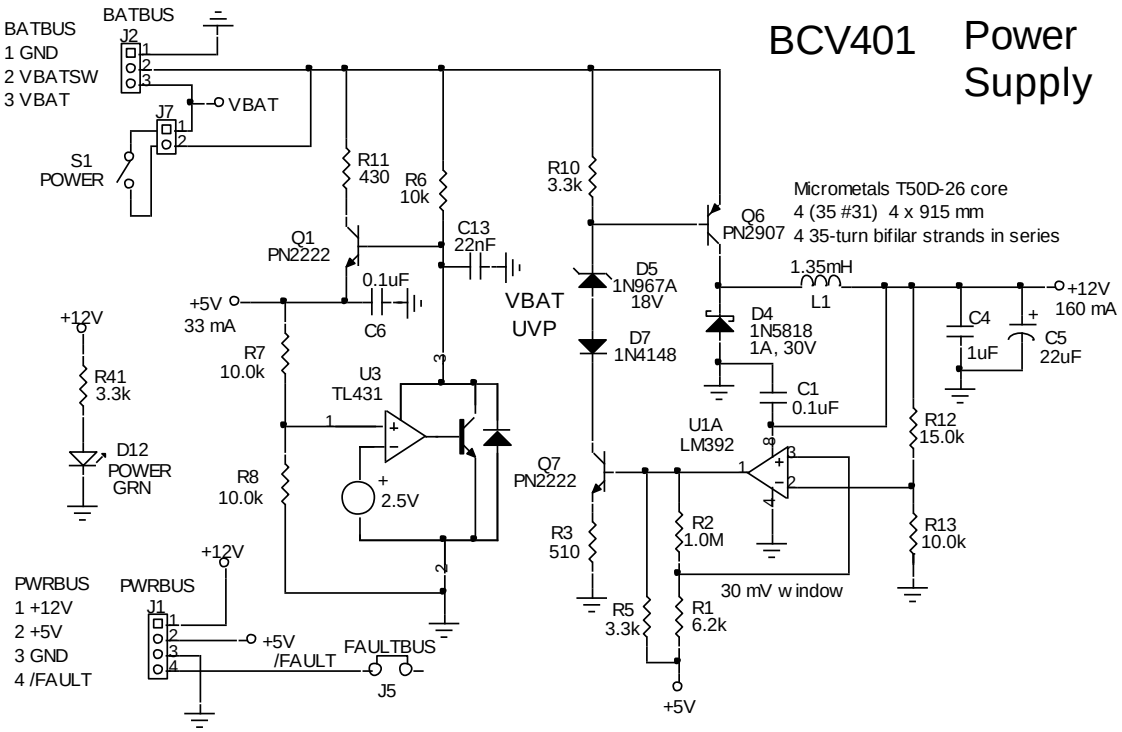

Fig. 2. Circuit diagram of the BCV401 power supply. It outputs to a four-pin power bus (PWRBUS) which includes the fault-bus line. The BATBUS connector brings in a nominal 24 V from the battery on VBAT which is switched by optionally off-board power switch S1. The L1 inductor winding is four strands of twisted #31 AWG wire 915 mm long. The four strands are connected in series external to the winding.

The rated supply outputs 12 V, 160 mA, and has a common-passive (CP or buck) PWM-switch configuration with active switch Q6 and passive switch D4 in series with L1. The voltage feedback from the output to the U1A commodity LM392 8-pin op-amp and comparator combination uses the comparator to switch BJT Q7 that drives Q6.

R5 from 5 V causes Q7 to conduct, causing Q6 to conduct and the 12-V supply starts. R1-R2 form a 30-mV hysteresis window at the divider output, and the comparator output switches at the high and low ends of this voltage window, making this a hysteretic controller. Its disadvantage is that it depends on a peak-to-peak 75-mV output ripple to function, but the ripple is always the same under varying load. What changes is switching frequency. The prototype BCV401 board photo is shown to the right in Fig. 3.

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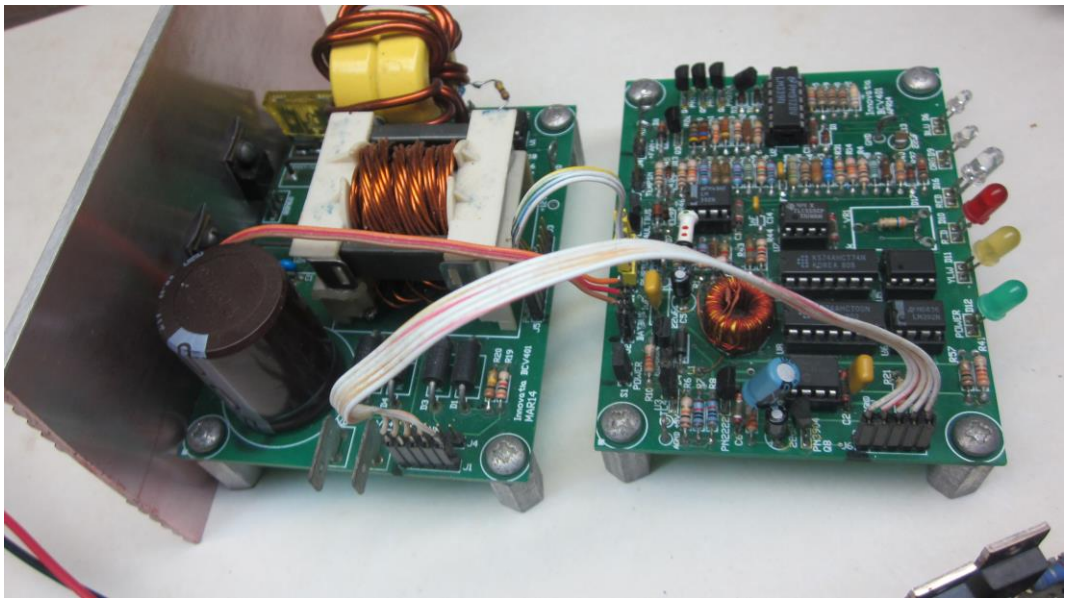

Fig. 3. Prototype BCV401 converter control board (right) drives the BCV402 (left, incorrectly marked as BCV401) converter power-transfer board. The square-pins and ribbon cables ease prototype bench work and modularize the system. The BCV401 supply inductor has a T50D toroid core. Indicator LEDs color-code faults and status in five colors, mounted on the right edge of the board.

Power supply diodes D5 and D7 translate the Q7 output voltage up to the high-side Q6 pnp switch. They also function as undervoltage protection (UVP) for the supply. The diodes do not conduct until there is at least 18.7 V across them, and with the 0.7 V needed across R10 to switch on Q6, the supply does not function with VBAT much less than 20 V.

When Q6 is off during off-time, C4 and C5 are discharging and the output voltage is decreasing. D4 is conducting and L1 is defluxing as its current ramps down. For Q6 to be off, Q7 must be off and the U1A output is pulled low to ground, sinking current from R5 || (R1 + R2). Thus, the comparator input at pin 3 has $v_+ < v_-$ at pin 2, and sets the lower hysteresis threshold voltage to the R1, R2 divider output voltage. From Fig. 4, comparator output voltage $v_C \approx 0$ V and at the comparator + input,

$$v_+ = \frac{1\,\text{M}\Omega}{1\,\text{M}\Omega + 6.2\,\text{k}\Omega} \cdot 5\ \text{V} = 4.969\ \text{V} \approx 4.97\ \text{V}$$

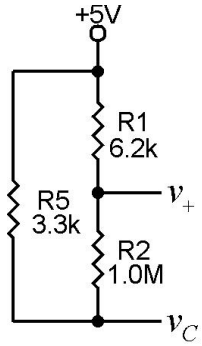

Fig. 4. BCV401 Power supply hysteresis circuit node at v_C is 30 mV below +5 V.

When the comparator output is high (open circuit or oc), R5 and the input resistance of Q7,

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$$(\beta_0 + 1)\cdot(r_e + R_E) = 150\cdot(536\ \Omega) = 80.4\ \text{k}\Omega$$

form an equivalent circuit of 4.803 V in series with 3170 Ω. This sets

$$v_+ = \frac{1003.17\ \text{k}\Omega}{1003.17\ \text{k}\Omega + 6.2\ \text{k}\Omega}\cdot(5\ \text{V} - 4.803\ \text{V}) + 4.803\ \text{V} = 4.999\ \text{V}$$

Thus the hysteresis window is calculated to be

$$\Delta v_+ = 4.999\ \text{V} - 4.969\ \text{V} = 30\ \text{mV}$$

Hysteretic CCM Voltage Control

Hysteretic control of voltage in CCM with output circuit Z_o having reactances L and C_o produces the waveforms shown in Fig. 5 with hysteresis levels $V_H = V_L = V_o$ (no hysteresis).

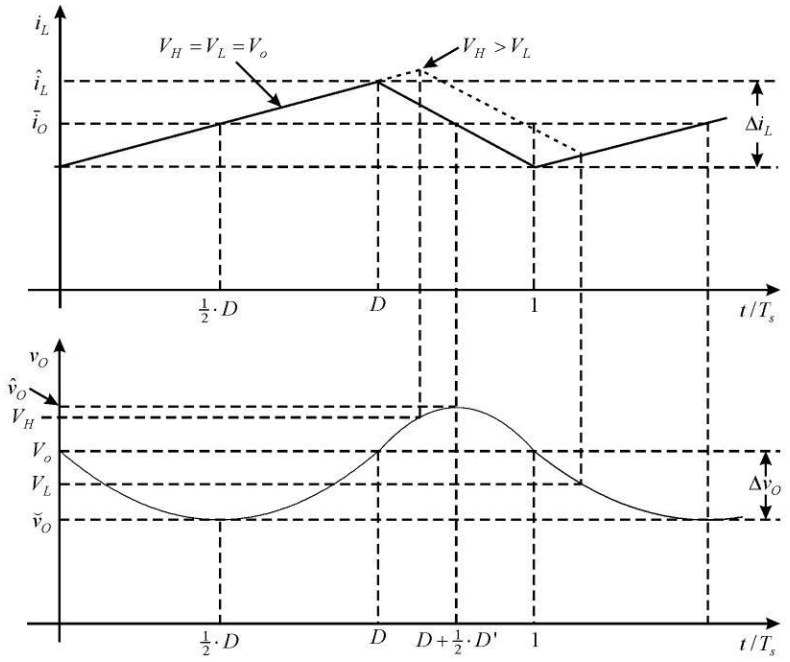

Fig. 5. Hysteretic voltage control in CCM of (upper graph) inductor current, and (lower graph) output voltage. The solid plot is without hysteresis ($V_H = V_L$) and for the dotted plot, $V_H > V_L$.

The triangle-wave inductor current i_L of the transfer-circuit charges Co = C4 + C5. In steady state, $\bar{i}_O = \bar{i}_L$. The areas of the plotted i_L waveform above and below $\bar{i}_O$ are equal for ΔiC = 0 C over a steady-state cycle.

During the first half of the on-time, i_L delivers insufficient current to maintain i_O, and the deficit comes from discharge of C_o by i_C. At ½·D, $i_L = \bar{i}_O$, i_C reverses, and C_o charges. Charging continues until i_L decreases to less than $\bar{i}_O$ at $D + ½\cdot D'$. Consequently, at the middle of on-time and off-time, i_C polarity reverses, as does the slope of C_o voltage $v_C = v_O$. C_o charges during the duty-ratio interval of [½·D, $D + ½\cdot D'$]. Thus, the voltage is shifted in phase π/2 or 90° from i_L—like a cosine-wave relative to i_L with extremes at $i_L(t) = \bar{i}_L = \bar{i}_O$.

Switching occurs in the graph of Fig. 5 at V_o with no separation between V_L and V_H. With hysteresis, $V_H > V_L$; the dashed current waveform corresponds to voltage levels of V_H and V_L. With or without hysteresis, the v_O

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waveform is not constrained to be between the V_L and V_H limits, and ripple is greater than the hysteresis window of $\Delta V = V_H - V_L$.

The series resonant circuit produces the v_O continuous segments shown in Fig. 5. These cosine voltage segments have segment waveshapes that are nearly parabolic because the resonant frequency $f_n << f_s$. Over small $\Delta\theta$,

$$\cos\theta \approx 1 - \theta^2/2\ ,\ \Delta\theta \approx 0$$

and is approximately parabolic.

A design equation for voltage ripple follows graphically from the sum of charge under the current waveform centered around $\bar{i}_O$;

$$\Delta v_O = \frac{q_-}{C_o} + \frac{q_+}{C_o} = \frac{\Delta i_L}{4} \cdot \frac{\left(\frac{1}{2}\cdot D + \frac{1}{2}\cdot D'\right)\cdot T_s}{C_o} = \frac{\Delta i_L \cdot T_s}{8 \cdot C_o}$$

where i_L ripple amplitude $\hat{i}_{L\sim} = \Delta i_L/2$ is the height of each of the four charge triangles. For a CP (buck) PWM-switch circuit, off-time inductor voltage is $V_o \cdot D'$;

$$\Delta i_L = \frac{\Delta\lambda}{L} = \frac{V_o \cdot D' \cdot T_s}{L} \Rightarrow \Delta v_O = \frac{V_o \cdot T_s^2}{8 \cdot L \cdot C_o} \cdot D' \Rightarrow$$

$$T_s^2 = \frac{8 \cdot L \cdot C_o}{D'} \cdot \frac{\Delta v_O}{V_o} = \frac{(2 \cdot \tau_n)^2}{D'} \cdot \frac{\Delta v_O / 2}{V_o} = \frac{(2 \cdot \tau_n)^2}{D'} \cdot \gamma(v_O) \Rightarrow$$

$$\boxed{f_s = \frac{1}{2 \cdot \sqrt{L \cdot C_o}} \cdot \sqrt{D' \cdot \left(\frac{V_o}{\Delta v_O / 2}\right)} = \frac{1}{2 \cdot \tau_n} \cdot \sqrt{D' \cdot \left(\frac{V_o}{\Delta v_O / 2}\right)} = \pi \cdot f_n \cdot \sqrt{\frac{D'}{\gamma(v_O)}}}\ ,\ \tau_n = \sqrt{L \cdot C_o}$$

where the output-voltage ripple factor is

$$\gamma(v_O) = \frac{\Delta v_O / 2}{V_o} = \left(\pi \cdot \frac{f_n}{f_s}\right)^2 \cdot D'$$

and τ_n is the resonant time-constant formed by L and C_o.

For design, f_s is chosen to be above the audible range but not by much, to minimize eddy-current loss. Solving for inductance from the f_s equation,

$$\boxed{L = \frac{D'}{8 \cdot C_o \cdot f_s^2} \cdot \left(\frac{V_o}{\Delta v_O}\right)}$$

The designed circuit has an unsaturated inductance of $L_0 \approx 1.35$ mH as given in the circuit diagram of Fig. 2.

The calculated values from the derived CCM design equations[9] are found by first solving for D' from the CP (buck) transfer ratio,

$$\frac{V_o}{V_g} = D \Rightarrow D' = 1 - \frac{V_o}{V_g},\ V_g \in [20\text{ V}, 25\text{ V}, 30\text{ V}] \Rightarrow D' \in [0.375, 0.5, 0.5833]$$

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where D = duty-ratio and D' = 1 – D. C_o is mainly C6, an electrolytic capacitor, having typical values of ¾ the rated value resulting in $C_o \approx 18$ µF. Then the resonant time constant is

$$\tau_n = \sqrt{(1.35\,\text{mH}) \cdot (18\,\mu\text{F})} = 156\ \mu\text{s} \Rightarrow 1/2{\cdot}\tau_n \approx 3207.5\ \text{Hz}$$

The switching frequency of the converter is

$$f_s = \frac{1}{2 \cdot \tau_n} \cdot \sqrt{D' \cdot \left(\frac{V_o}{\Delta v_O / 2} \right)} = \left[(3207.5\,\text{Hz}) \cdot \sqrt{\frac{12.5\,\text{V}}{75\,\text{mV}/2}} \right] \cdot \sqrt{D'} = (58.57\,\text{kHz}) \cdot \sqrt{D'}$$

Then for the three values in the V_g (input voltage) range,

Table. Switching frequency versus input voltage.

V_g, V	f_s, kHz
20	35.86
25	41.42
30	44.73

What is not included in the derivation of f_s is loop delay that also causes Δv_O to be larger and f_s lower. Instead of approximating the delay, the oscilloscope (OS) graph of Fig. 6 shows that the ripple peaks lag behind the comparator transitions by about 2 µs, resulting in $\Delta v_O \approx 100$ mV. Substituting this value and solving at midscale (V_g = 25 V, D' = 0.5),

$$f_s = \frac{1}{2 \cdot \tau_n} \cdot \sqrt{D' \cdot \left(\frac{V_o}{\Delta v_O / 2} \right)} = (3207.5\,\text{Hz}) \cdot (15.81) \cdot \sqrt{D'} = (50.715\,\text{kHz}) \cdot \sqrt{0.5} = 35.86\,\text{kHz}$$

This value compares favorably with the OS frequency measurements of the two waveform traces. Control supply ripple and comparator switching are shown in Fig. 6.

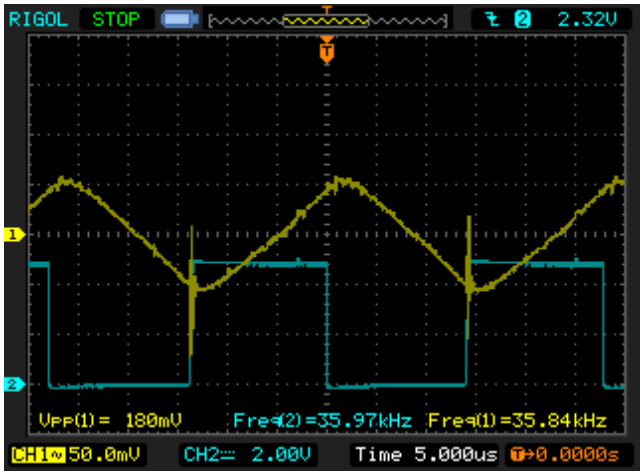

Fig. 6. BCV401 Power Supply DSO traces: 1 (yellow): Output ripple of $v_{\sim} \approx 100$ mV; 2 (blue): Comparator output with levels of 0 V and 4.8 V at a switching frequency of 36 kHz. Extrema are delayed slightly from comparator changes.

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Under light output loading, the switching frequency is high as the hysteretic converter operates deep in CCM and the parabolic waveshape of the output voltage ripple becomes more linear. The ripple reaches its peak about 2 µs after the fifth time division, where the switch transition occurs.

The parabolic waveshape of Fig. 5 becomes more evident at lower frequencies as shown in Fig. 7. The input is at a test voltage of V_g = 14.5 V (well below the rated input minimum of 20 V) and the output is loaded by a resistance of R_L = 100 Ω, or with an output current of 120 mA. Under these conditions, the switching frequency is about a decade lower, the converter is operating slightly in DCM (in the sixth time division on the OS screen of Fig. 7), and the parabolic waveshape derived above is apparent. At the sixth division, the power switch conducts and as inductor current increases, output voltage ripple turns upward.

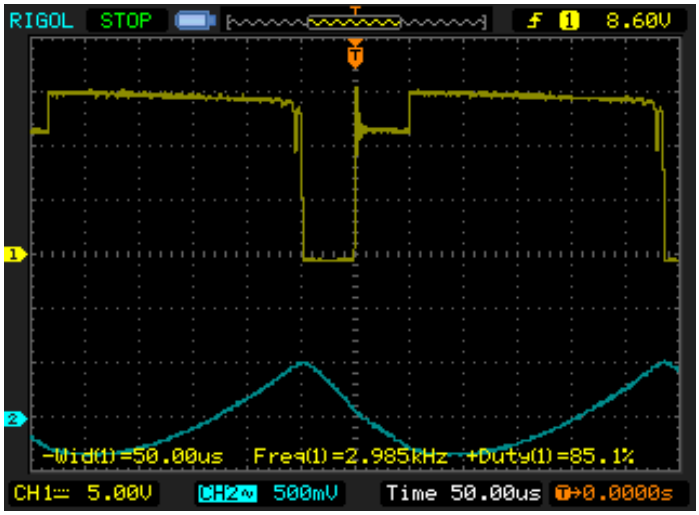

Fig. 7. Converter 12-V switching supply: trace 1: v_{SW} (D4 cathode); trace 2: v_O at 12 V with a load of R_L = 100 Ω. The input test voltage is $V_g \approx 14.5$ V.

The next task is to design the switching supply inductor, the subject of the next part of the Volksinverter series.

References

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9. Derivations and explanations of hysteretic control design equations for both CCM and DCM operation are given in more detail in the section "Hysteresis Voltage Control" in the chapter "Converter Control" in the third volume *Converter Dynamics* of *Power Converter Design Optimization*, Dennis L. Feucht, Innovatia, www.innovatia.com.

About The Author

Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

For further reading on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC power inverters."

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