

## **Enhanced Switched Tank Converter Offers Flexible Fixed-Ratio Power Conversion For Data Centers**

by Paolo Sandri, STMicroelectronics, Santa Clara, Calif.

Data-center power consumption is reaching unprecedented levels, which poses great challenges to the environment and global CO<sub>2</sub> emissions. The International Energy Agency reported that global data centers used 220 to 320 TWh of electricity in 2021 (0.9% to 1.3% of global electricity demand), while data transmission networks consumed 260 to 340 TWh (1.1 to 1.4%).<sup>[1]</sup>

Machine learning (ML), another area of demand growth, has potentially significant implications for future data-center energy use. Overall, use of digital chipsets in data-center infrastructure, including CPUs, GPUs, and other specialized digital ASICs, is growing yearly, with a trend toward power levels of 1 kW per chipset for future GPUs. This power consumption trend requires ruthless attention to maximizing efficiency in energy distribution.

Data-center power consumption, measured in power usage effectiveness (PUE), is the ratio of total power consumed by the data center divided by the useful (server) power.<sup>[2]</sup> An ideal PUE—i.e., 100% efficiency—is 1 and says all consumed energy is used by equipment and there is no power distribution loss. Of course, this level of efficiency is impossible to achieve. However, real-world PUE values range from 1.1 for the most efficient data centers to 2 or more for less efficient ones. So, there are many opportunities to improve efficiency.

One way to improve efficiency is to change the rack bus-bar power distribution from the traditional 12 V to 48 V (nominal 54 V). This reduces distribution losses due to the lower current on the 48-V dc bus.<sup>[3]</sup> Recognizing this fact, data centers have been moving from 12-V to 48-V buses for in-rack power delivery for several years. For example, Google made this transition to 48 V several years ago, and this trend continues to grow among other data center/cloud computing companies. This move to 48 V, in turn, is driving innovations in power converter design.

Specifically, a 48-V dc input bus requires new power-delivery topologies that can efficiently manage power conversion from the 48-V input down to the traditional 12-V dc bus for local, on-board power delivery to the high-power chipsets. There are two ways to implement the down-conversion from the 48-V dc bus—with regulated topologies and with unregulated topologies, depending on the nature of the downstream load it supplies.

After a brief review of the tradeoffs between regulated and unregulated topologies for stepping down 48-V buses in data centers, this article discusses ST's recently developed hybrid switched tank converter (HSTC), an unregulated topology that takes advantage of recent changes in data-center power specifications from the Open Compute project to provide greater efficiency and higher stepdown ratios. These capabilities can be leveraged to generate 12-V or lower intermediate buses for powering multiphase voltage regulators and their processor or ASIC loads with further benefits in the design of the voltage regulators.

This article discusses the motivation for developing the HSTC topology, its principles of operation—which revolve around use of a transformer—and an analysis of its circuit operation. This analysis produces expressions for the transformer turns ratio for two likely stepdown ratios, and currents and voltages seen by the power MOSFETs for these stepdown ratios. A subsequent section of the article discusses design requirements for the two main capacitors used in this topology. Finally, a 700-W HSTC reference design is briefly described and its efficiency over load is presented.

### **Regulated Versus Unregulated Topologies**

When stepping down a 48-V bus, regulated topologies are best when the intermediate 12-V bus is the “arrival point” and must serve loads whose input needs to be a well-controlled 12 V. These include DDR5, HDD or PCIe cards. If the load can accept a wider range of 12-V input, such as when the intermediate bus is the input of a second-stage converter that converts the 12 V to the final POL voltage, such as for a CPU or other digital ASICs,

an “unregulated topology” can be appropriate. Fig. 1 illustrates these two cases and cites some example topologies used to generate the 12-V buses.

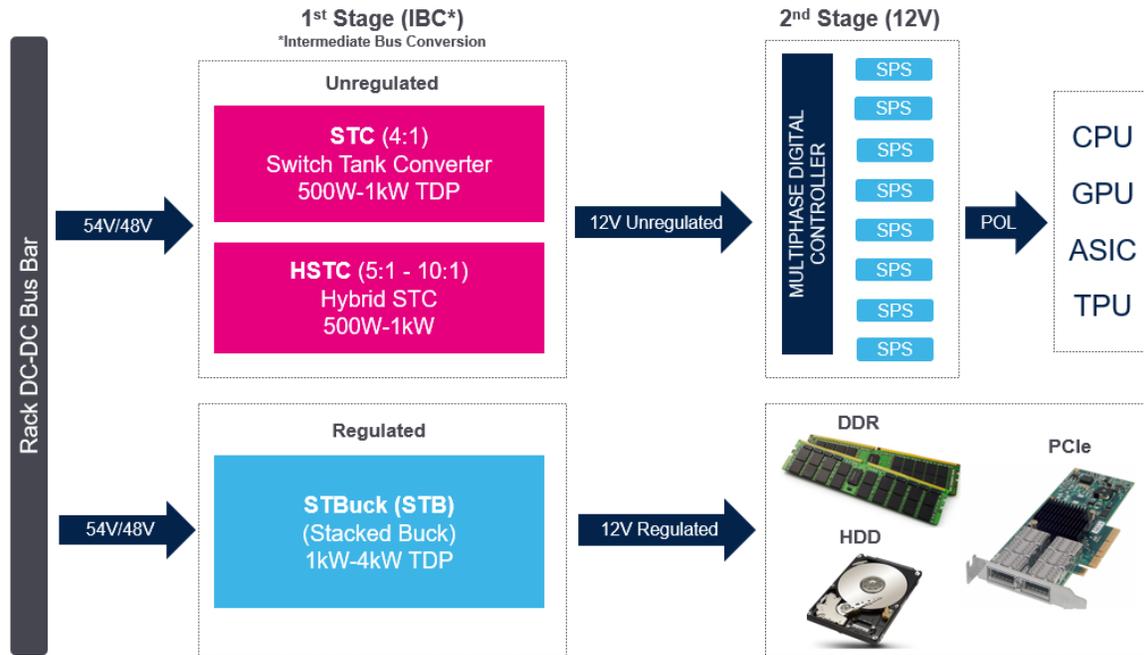


Fig. 1. Typical regulated and unregulated dc-dc power delivery from a 54-V bus.<sup>[4]</sup>

One consideration for the unregulated topology is how it responds to the wider input dc bus variation, typically from 40 V to 60 V, and how much the output voltage changes. For example, for a fixed conversion ratio of 4:1, the corresponding output voltage bus would range from 10 V to 15 V. This has implications for the design of the second stage that it powers.

Specifically, it requires a more careful selection of the downstream VR converter components compared to the more traditional case where a regulated 12-V is generated due to the higher input voltage the VR converter needs to sustain.

In summary, regulated topologies are better when requesting a controlled 12-V intermediate bus, typically when it is the destination point of regulation, while unregulated topologies can be used when they provide an intermediate voltage that will be further regulated by a second conversion stage to the specific POL (typically a CPU or digital ASIC). However, the requirements for this second power stage are evolving.

Recently, in the spirit of simplifying data-center power delivery and improving the data center’s total cost of ownership (TCO), the Open Compute Project organization (OCP) generated a new specification to drive the next generation of rack systems with a narrower 48-V input bus. The OCP Open Rack V3 specification, in fact, specifies that the new dc bus bar voltage in a server rack can range from 51 V at no load, to 50.5 V at full load, with an overall range from 47.5 V to 51 V.<sup>[5]</sup> This is a much narrower range compared to the current 40-V to 60-V one.

The transition to a narrower bus bar voltage creates new opportunities to use unregulated topologies in addition to the regulated ones. In fact, a narrower input voltage produces a correspondingly narrower output range when using a given fixed-ratio conversion topology. For example, if the conversion ratio is 4:1 the input voltage variation from 51 V to 47.5 V becomes an output voltage variation from 12.75 V to 11.875 V, a range much closer to the traditional 12-V regulated bus.

The narrower input range also encourages optimized component selection for the 12-V multiphase regulator delivering better efficiency and reliability, too. In essence the new specification enables use of lower-voltage power MOSFETs with lower  $R_{DS(ON)}$  and reduced voltage stress during switching.

Further, the narrow  $V_{in}$  specification also enables higher fixed-conversion ratios such as a conversion ratio of 5:1. With this conversion ratio, the OCP Open Rack V3 narrow input, which ranges from 51 V to 47.5 V, translates to an output voltage of 10.2 V to 9.5 V. As this intermediate voltage can drive a multiphase buck regulator delivering sub-voltage values (typically ranging from 1.8 V down to 0.8 V) to the digital ASICs, its more favorable duty-cycle positioning can enable higher efficiency performance than an equivalent 12-V input system.

So, this narrow  $V_{in}$  specification enables higher-ratio unregulated topologies, with several added benefits. These include enhanced second-stage multiphase efficiency conversion, use of a leaner and more efficient battery backup system, and ultimately, a move to address the modern data-center energy challenge.

In developing innovative 54-V to 12-V conversion topologies in both the regulated and unregulated domains, ST has focused on efficiency maximization across the full load range. In addition, solution TCO (total cost of ownership), power density, scalability, and off-the-shelf component enablement with multiple source options has also taken precedence.

ST's newly developed hybrid switched tank converter (HSTC) topology delivers a fixed-ratio 5:1 conversion with minimized BOM, high efficiency, and high density. This article highlights its principles of operation and the fundamental design guidelines to design and customize the HSTC architecture for specific power needs and optimized performance.

### ***A Combination Of Two Topologies***

The HSTC is an unregulated topology combining an STC (switched tank converter) and an LLC converter. In developing this new topology, we wanted to minimize the MOSFETs' losses and provide a fixed-ratio conversion with minimal BOM components for any conversion ratio and maximize conversion efficiency.

A disadvantage of traditional converters is that MOSFET switches must sustain both the (high) input voltage and the (high) output current. The HSTC topology uses a transformer to scale down the voltage seen by the output MOSFETs, enabling usage of much lower  $R_{DS(ON)}$  devices. Similarly, the current flowing in the input MOSFETs is a fraction of the output current, minimizing the overall conduction losses.

Experimental results confirmed that the efficiency performance of the HSTC using a 5:1 ratio is better than the traditional switched tank converter (STC) topology with the same conversion ratio. Using a 5:1 HSTC is also better from a cost point-of-view since it uses fewer components than the STC (five MOSFETs in the HSTC versus 13 MOSFETs in the STC).

The converter's output voltage is a fixed fraction of the input one, usually with ratios of 4:1 or 5:1. For example, with an input range of 47.5 V to 51 V the output will be 11.875 V to 12.75 V in a 4:1 implementation or 9.5 V to 10.2 V with a 5:1 implementation. In these cases, the HSTC components will experience the following conditions:

- The current seen by the input MOSFETs will be 2/4 or 2/5 of the output one, circulating for 50% of the time.
- The voltage seen by the output MOSFETs will be 1/4 or 1/5 of the input one.

The most basic implementation of the HSTC topology would be the single-cell configuration shown in Fig. 2. More cells can be paralleled (if an even number of cells are used, the input ripple disappears) to achieve a higher power conversion with benefits in scalability, modularity, and energy efficiency that a multiphase-like solution typically offers.

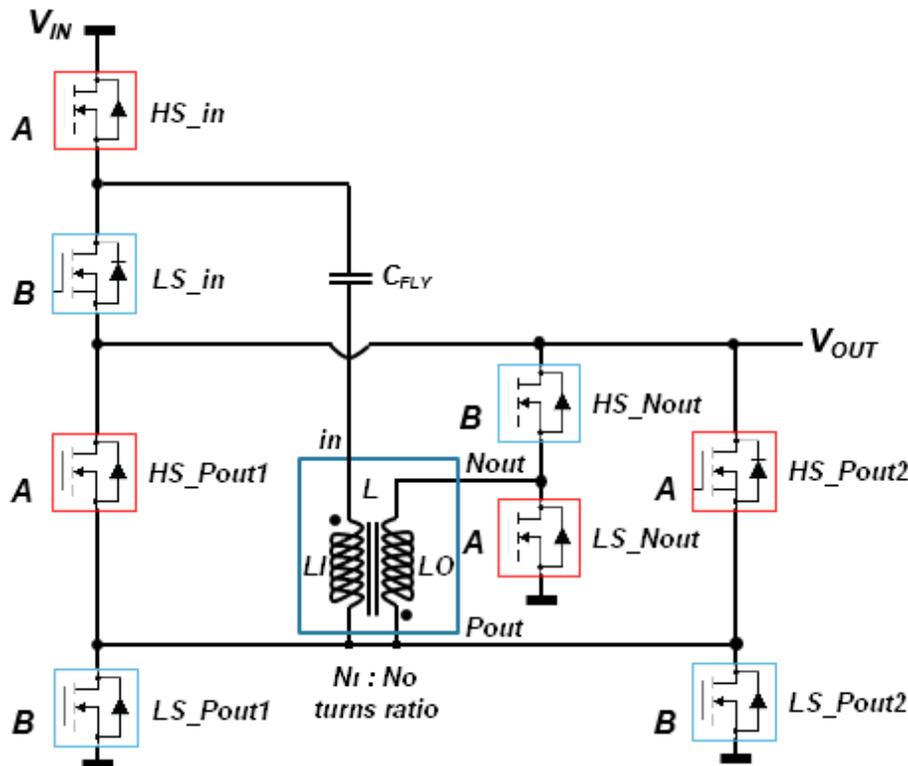


Fig. 2. HSTC topology. The basis for the HSTC topology is a series of low-side and high-side switches in combination with a transformer that reduces the output voltage seen by the output power switches, when compared with the conventional switched tank converter.

### The Concept Behind The Topology

The HSTC topology basic cell appears in Fig. 2 where:

- Input components are the HS\_in and LS\_in (high-voltage MOSFETs), and the  $C_{FLY}$  capacitance.
- Output components are the other six low-voltage MOSFETs.
- The transformer L, with turns ratio  $N = N_i:N_o$ , is shared between input and output, and multiplies the input current and divides the input voltage.
- The current flowing in the input MOSFETs goes directly to the output, not to ground.
- $C_{FLY}$  has two purposes: it eliminates dc current on the input side of the transformer, allowing full use of the magnetic cycle of the core material and stores the energy that drives the negative part of the input cycle, when LS\_in is on.  $C_{FLY}$  is charged at  $V_{in}/2$ , regardless of the dividing ratio of the cell.

The six MOSFETs are divided into two groups of A and B, which are alternately driven in phases—akin to how the output stages are driven in a multiphase converter. For this reason, we'll refer to the two groups of MOSFETs as phases A and B. The control scheme drives the A and B phases of the MOSFETs with a 50% fixed duty cycle. Phase A is on when phase B is off, and vice versa.

The system needs a soft start from the input voltage, usually implemented by an eFuse connected in series with the stage.

### Operating Principles

For analysis of system behavior, two operating conditions can be considered (Figs. 3 and 4), where in phase A and phase B the designated MOSFETs are respectively on or off.

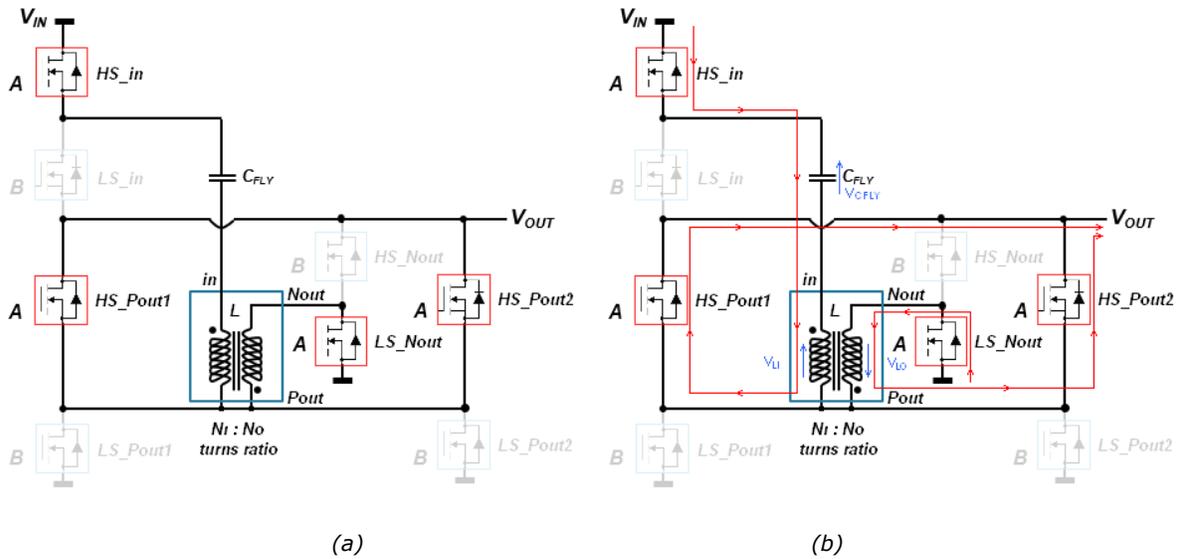


Fig. 3. Phase A on and phase B off.

In this first operating condition (phase A on and phase B off), with  $I_D$  the drain current of the MOSFETs considered, we have:

$$I_{OUT} = I_D(HS\_Pout1) + I_D(HS\_Pout2) = I_{IN} + I_D(LS\_Nout)$$

$$V_{LI} = V_{IN} - V_{CFLY} - V_{OUT}$$

$$V_{LO} = V_{LI} * N_o/N_1 = V_{LI} * N = V_{OUT}$$

where  $V_{LI}$  is the voltage across the transformer input and  $V_{LO}$  is the voltage across the transformer output.

During this period of time  $C_{FLY}$  is charging, and if its value is high enough, the voltage across it can be considered constant.

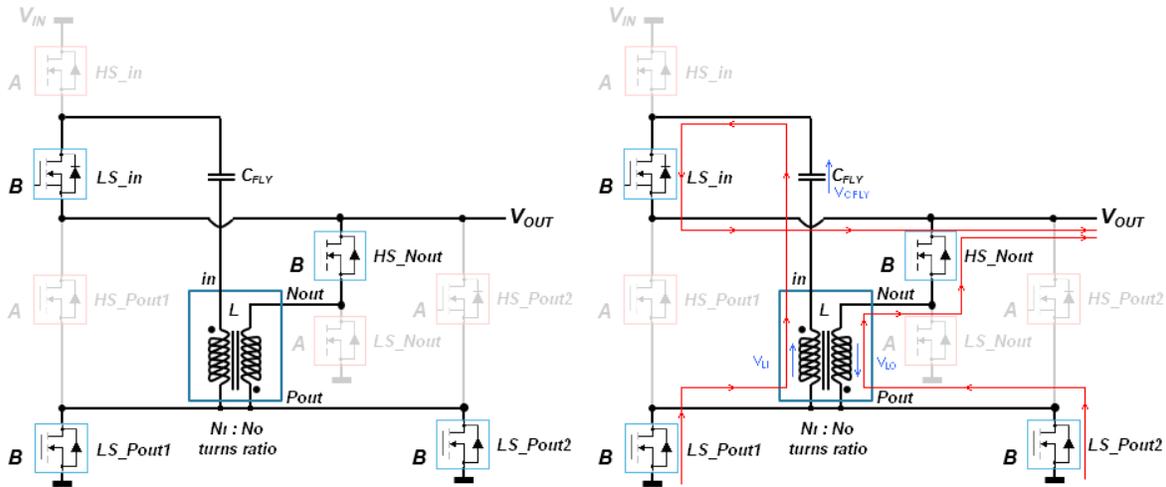


Fig. 4. Phase A off and phase B on.

In this second operating condition (phase A off and phase B on), we have:

$$I_{OUT} = I_D(LS\_in) + I_D(HS\_Nout) = I_D(LS\_Pout1) + I_D(LS\_Pout2)$$

$$V_{LI} = -V_{CFLY} + V_{OUT}$$

$$V_{LO} = V_{LI} * N_o/N_i = V_{LI} * N = V_{OUT}$$

During this period of time  $C_{FLY}$  is discharging and no current is drawn from  $V_{IN}$ .

Due to the series capacitor  $C_{FLY}$  the average voltage on the left side of  $L$  is zero, so:

$$V_{LI} * T(\text{phase A} = \text{On}) + V_{LI} * T(\text{phase A} = \text{Off}) = 0$$

$$(V_{IN} - V_{CFLY} - V_{OUT}) * T(\text{phase A} = \text{On}) + (-V_{CFLY} + V_{OUT}) * T(\text{phase A} = \text{Off}) = 0$$

The duty cycle is 50%, so  $T(\text{phase A} = \text{On}) = T(\text{phase A} = \text{Off})$ , hence

$$V_{IN} - V_{CFLY} - V_{OUT} + (-V_{CFLY} + V_{OUT}) = 0$$

$$V_{IN} - V_{CFLY} - V_{OUT} - V_{CFLY} + V_{OUT} = 0$$

$$V_{IN} - 2 V_{CFLY} = 0$$

$$V_{CFLY} = V_{IN}/2$$

The turns ratio of  $L$  is related to the desired output voltage, or better to the desired  $V_{IN}/V_{OUT}$  ratio. Inserting  $V_{CFLY}$  found above we have:

$$V_{LI} = V_{IN} - V_{CFLY} - V_{OUT} = V_{IN} - V_{IN}/2 - V_{OUT} = V_{IN}/2 - V_{OUT}$$

Now notice that in both operating conditions  $V_{OUT}$  is equal to  $V_{LO}$ :

$$V_{LO} = V_{LI} * N = V_{OUT}$$

Then:

$$V_{LI} = V_{IN}/2 - V_{OUT} = V_{IN}/2 - V_{LO}$$

$$V_{LI}/V_{LO} = N = 1/2V_{IN}/V_{OUT} - 1$$

$$V_{IN}/V_{OUT} = 2N + 2$$

Hence, for a  $V_{IN}/V_{OUT}$  ratio of 4 the  $N_I/N_O$  ratio must be 1, and for a  $V_{IN}/V_{OUT}$  ratio of 5 the  $N_I/N_O$  ratio must be 1.5.

Table 1. Transformer turns ratio for the two stepdown ratios.

$V_{IN}/V_{OUT}$	$N = N_I/N_O$
4	1
5	1.5

### Current And Voltage Seen By The MOSFETs

Tables 2 to 4 below show the voltages and currents for each component during the two working conditions. These values provide an interesting indication for the design and selection of the different parts of the circuit.

Table 2. General expressions for MOSFET voltages and currents.

MOSFET	A On, B Off				A Off, B On			
	V <sub>drain</sub>	V <sub>source</sub>	V <sub>D</sub> -V <sub>S</sub>	I <sub>D</sub>	V <sub>drain</sub>	V <sub>source</sub>	V <sub>D</sub> -V <sub>S</sub>	I <sub>D</sub>
HS_in	V <sub>IN</sub>	V <sub>IN</sub>	0	$\frac{I_{OUT}}{N+1}$	V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>IN</sub> - V <sub>OUT</sub>	0
LS_in	V <sub>IN</sub>	V <sub>OUT</sub>	V <sub>IN</sub> - V <sub>OUT</sub>	0	V <sub>OUT</sub>	V <sub>OUT</sub>	0	$\frac{I_{OUT}}{N+1}$
HS_Pout1	V <sub>OUT</sub>	V <sub>OUT</sub>	0	$\frac{I_{OUT}}{2}$	V <sub>OUT</sub>	GND	V <sub>OUT</sub>	0
LS_Pout1	V <sub>OUT</sub>	GND	V <sub>OUT</sub>	0	GND	GND	0	$\frac{I_{OUT}}{2}$
HS_Pout2	V <sub>OUT</sub>	V <sub>OUT</sub>	0	$\frac{I_{OUT}}{2}$	V <sub>OUT</sub>	GND	V <sub>OUT</sub>	0
LS_Pout2	V <sub>OUT</sub>	GND	V <sub>OUT</sub>	0	GND	GND	0	$\frac{I_{OUT}}{2}$
HS_Nout	V <sub>OUT</sub>	GND	V <sub>OUT</sub>	0	V <sub>OUT</sub>	V <sub>OUT</sub>	0	$I_{OUT} \frac{N}{N+1}$
LS_Nout	GND	GND	0	$I_{OUT} \frac{N}{N+1}$	V <sub>OUT</sub>	GND	V <sub>OUT</sub>	0

Note: The MOSFET currents are calculated considering that the average current consumption from V<sub>IN</sub> is, excluding the losses,  $I_{IN} = P_{OUT}/V_{IN} = V_{OUT} \cdot I_{OUT}/V_{IN} = I_{OUT}/(2N+2)$ . Due to the 50% duty cycle, the I<sub>IN</sub> in the A

on and B off condition is exactly twice the average, i.e.,  $I_{OUT}/(N+1)$ . The MOSFETs' HS\_Pout1 and HS\_Pout2 are in parallel and, if they are the same type, then their current will be the same, i.e.,  $I_{OUT}/2$ . Similarly for LS\_Pout1 and LS\_Pout2. The current in LS\_Nout is the difference between  $I_{OUT}$  and  $I_{IN}$ , and the current flowing in HS\_Nout is the same as in  $C_{FLY}$ , which must be equal to  $I_{IN}$ .

For example, if  $V_{IN} = 54\text{ V}$ ,  $V_{OUT} = V_{IN}/4$  ( $N = 1$ ) and  $I_{OUT} = 50\text{ A}$ , we obtain the voltages and currents in Table 3.

Table 3. MOSFET voltage and current values for a  $V_{IN}/V_{OUT}$  ratio of 4.

MOSFET	A On, B Off				A Off, B On			
	Vdrain	Vsource	$V_D-V_S$	$I_D$	Vdrain	Vsource	$V_D-V_S$	$I_D$
HS_in	$V_{IN}$	$V_{IN}$	0	25 A	$V_{IN}$	$V_{OUT}$	40.5 V	0
LS_in	$V_{IN}$	$V_{OUT}$	40.5 V	0	$V_{OUT}$	$V_{OUT}$	0	25 A
HS_Pout1	$V_{OUT}$	$V_{OUT}$	0	25 A	$V_{OUT}$	GND	13.5 V	0
LS_Pout1	$V_{OUT}$	GND	13.5 V	0	GND	GND	0	25 A
HS_Pout2	$V_{OUT}$	$V_{OUT}$	0	25 A	$V_{OUT}$	GND	13.5 V	0
LS_Pout2	$V_{OUT}$	GND	13.5 V	0	GND	GND	0	25 A
HS_Nout	$V_{OUT}$	GND	13.5 V	0	$V_{OUT}$	$V_{OUT}$	0	25 A
LS_Nout	GND	GND	0	25 A	$V_{OUT}$	GND	13.5 V	0

Another example with  $V_{IN} = 54\text{ V}$ ,  $V_{OUT} = V_{IN}/5$  ( $N = 1.5$ ) and  $I_{OUT} = 50\text{ A}$  produces the results in Table 4.

Table 4. MOSFET voltage and current values for a  $V_{IN}/V_{OUT}$  ratio of 4.

MOSFET	A On, B Off				A Off, B On			
	Vdrain	Vsource	$V_D-V_S$	$I_D$	Vdrain	Vsource	$V_D-V_S$	$I_D$
HS_in	$V_{IN}$	$V_{IN}$	0	20 A	$V_{IN}$	$V_{OUT}$	43.2 V	0
LS_in	$V_{IN}$	$V_{OUT}$	43.2 V	0	$V_{OUT}$	$V_{OUT}$	0	20 A
HS_Pout1	$V_{OUT}$	$V_{OUT}$	0	25 A	$V_{OUT}$	GND	10.8 V	0
LS_Pout1	$V_{OUT}$	GND	10.8 V	0	GND	GND	0	25 A
HS_Pout2	$V_{OUT}$	$V_{OUT}$	0	25 A	$V_{OUT}$	GND	10.8 V	0
LS_Pout2	$V_{OUT}$	GND	10.8 V	0	GND	GND	0	25 A
HS_Nout	$V_{OUT}$	GND	10.8 V	0	$V_{OUT}$	$V_{OUT}$	0	30 A
LS_Nout	GND	GND	0	30 A	$V_{OUT}$	GND	10.8 V	0

### Considerations For Capacitor Design ( $C_{FLY}$ And $C_{IN}$ )

The proper design of the  $C_{FLY}$  capacitor is fundamental to ensure the best efficiency and performance that this topology can offer. A key consideration drives the design of  $C_{FLY}$ .

#### $C_{FLY}$ Equivalent Impedance And Bias Effect

Considering the voltage drop created across  $C_{FLY}$  during the time phase A is on and B is off, the resulting equivalent voltage on  $L_I$  is not a perfect square wave. It exhibits a trapezoidal shape due to the  $C_{FLY}$  discharge.

Based on this, the equivalent square-wave of  $V_{L_I}$  is a square-wave whose voltage, instead of being  $V_M$ , is in practice

$$V_{C_{FLY}} - \frac{\Delta V_{C_{FLY}}}{2} = V_{C_{FLY}} - \frac{T_{ON}}{2 \cdot C_{FLY}} \cdot I_{L_I}$$

An equivalent series resistance

$$R_{eq} = T_{ON} / 2 \cdot C_{FLY}$$

can be considered in series with the  $HS_{in}$ . This affects the equivalent phase-node excursion and, in turn, also affects efficiency.

As a result, a bigger  $C_{FLY}$  causes a lower  $R_{eq}$  and positively affects system efficiency.

Based on these considerations, you need to take additional care to consider the "bias effect" of the MLCC in the equations above: we recommend using the real value of  $C_{FLY}$  at the biasing voltage ( $V_{C_{FLY}} = V_{IN}/2$ ) for proper estimations.

#### $C_{IN}$ Series Impedance

The RMS current ripple at the input is  $I_{INpk}/2 = I_{OUT}/(2N+2)$ , the same value of the average input current. This ripple current flows in the two parallel input impedances, which are:

- the supply source impedance
- the input capacitor  $C_{IN}$  impedance.

This ripple current is on the order of 10 A, so its thermal contribution can be as high as 100 mW for each milliohm of impedance which it flows through. Worst case, this ripple flows entirely in the input capacitor  $C_{IN}$ .

For example, if a 100- $\mu$ F  $C_{IN}$  is implemented by some MLCCs in parallel, then its resistance may be lower than 1 m $\Omega$ . On the other hand, an electrolytic capacitor can have an ESR of 50 m $\Omega$ , and can dissipate 5 W. This value is too big for high efficiency performance and even worse for the life of the capacitor itself.

### Reference Design And Experimental Results

An example of a 700-W HSTC reference design appears in Fig. 5. Its simplified schematic is shown in Fig. 6.

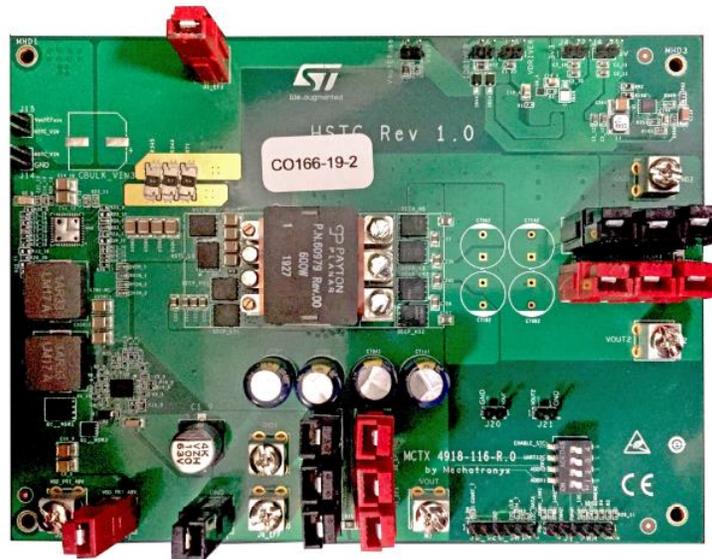


Fig. 5. The 700-W HSTC reference design board.

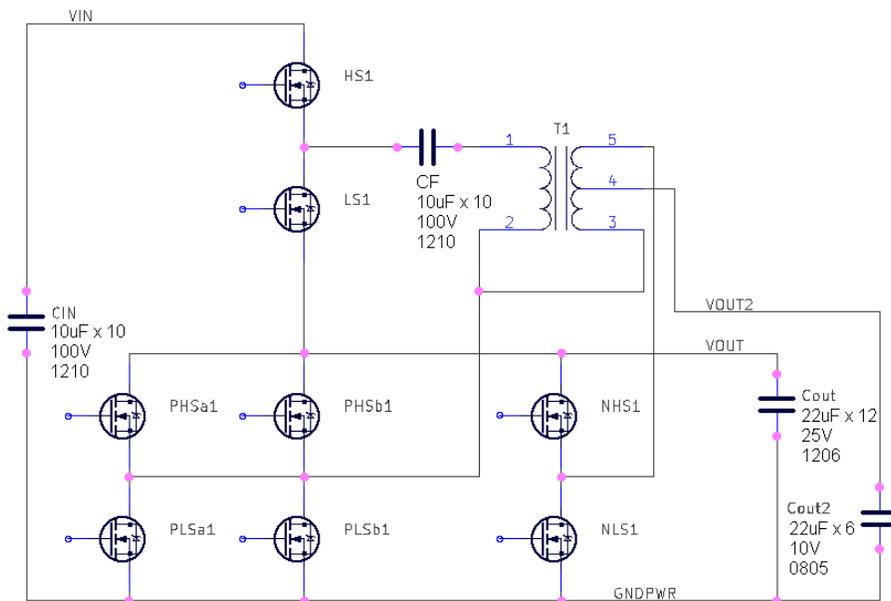


Fig. 6. A simplified schematic for the 700-W HSTC reference design.

The design goal is to maximize conversion efficiency across the entire load range and provide the highest power density. The HSTC PCB size for this reference design is 25 mm x 60 mm, which corresponds to a power density of 300 W/inch<sup>2</sup>. This HSTC example uses an SMD planar transformer. Other reference designs have been implemented with integrated planar magnetics for different power levels.

The 700-W reference board delivers a very flat efficiency curve (Fig. 7), with a peak of 98.5% at 280 W and an efficiency always above 98% from 140 W up to 500 W with a very flat profile.

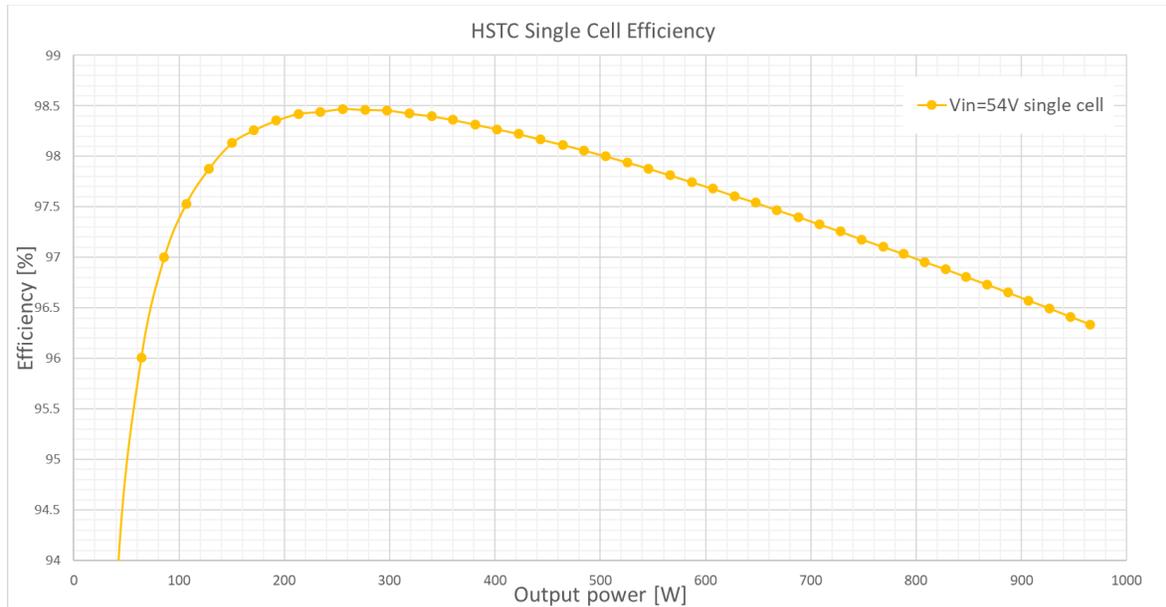


Fig. 7. Efficiency results for the HSTC reference design.

### Conclusion

The hybrid switched tank capacitor topology is a new fixed-ratio, unregulated topology that maximizes efficiency while delivering high power density and minimizing BOM component count (and therefore cost) for any conversion ratio, while using a transformer instead of inductors as in the conventional STC.

The topology is particularly suited to support the new OCP Open Rack V3 specification with a narrow  $V_{in}$  ranging from 47.5 V to 51 V. It allows a higher efficiency and lower voltage stress on the second stage digital multiphase VR that delivers power to the high current digital chipsets (CPU, GPU, etc.). The efficiency advantage versus an STC becomes greater as the conversion ratio increases.

Finally, the HSTC topology enables flexible designs that can deliver higher conversion ratios of, for example, 6:1, 8:1, or 10:1, with the same minimal number of BOM components. It is suitable to efficiently support the next-generation VR trend toward lower input voltage.

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## About The Author



*Paolo Sandri is responsible for specialized Power Management Products at STMicroelectronics. Paolo joined ST as an analog IC design engineer in the Castelletto design center in Italy, where he developed several power conversion ICs. Later, he took on responsibility for U.S.A. market development for power ICs and is currently focused on power management for data centers and cloud computing, where he contributes to improving data center efficiency and power delivery through innovative solutions. Paolo holds a BSEE and MSEE from University of Padua (Italy) with specialization in power conversion.*

*For more information on dc-dc converter design, see the How2Power [Design Guide](#), locate the Power Supply Function category and select "DC-DC Converter". Also locate the Popular Topics category and select "Buck Converters".*