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Designing An Open-Source Power Inverter (Part 11): Minimizing Switch Loss In Low-Input-Resistance Converters

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Low-voltage, high-current input, or low-R_g, power converters are becoming more common as supply voltages are reduced and currents increased. Examples are the point-of-load converters for computer microprocessors and battery chargers for cell phones, power tools, and electric vehicles. However, off-grid inverters also have low-R_g battery-input power ports exemplified by the design of the off-grid 24-V battery converter of the Volksinverter.

In this latest part in the Volksinverter design article series,[1-10] we address a key aspect of optimizing the battery converter stage whose circuitry is realized in the BVC402 module (Fig. 1). As with other low-R_g converter designs, the design of this battery converter begins with a decision about which power-transfer circuit is optimum for this stage. Here in part 11, we consider this issue in terms of which topology minimizes switching loss. Specifically, we'll be comparing the boost push-pull circuit versus single-ended PWM-switch circuits.

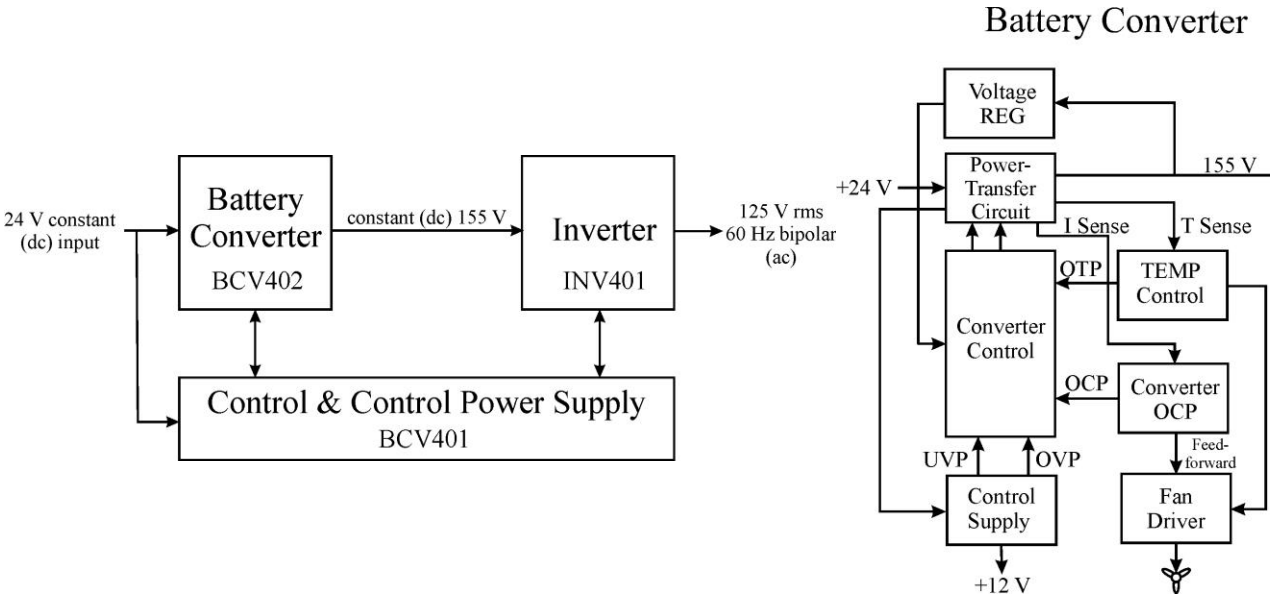

Fig. 1. The Volksinverter's system block diagram (left) and the BCV402 battery converter stage block diagram (right). The battery converter requires optimization of its power transfer circuit for efficiency, including minimization of its switching losses.

Power-Transfer Circuit

Converter design demonstrates how power circuits and magnetics optimization interact significantly, and reveals what the magnetics designer needs to know about the circuit to optimally design the magnetics parts. At the functional center of the converter, the power-transfer circuit has relatively few parts though it is more complicated than it might appear.

Low-R_g power transfer presents complications of large wire size, large circuit-board traces supported by an additional bus bar soldered to them, and large power MOSFETs. These circuits are optimally push-pull because parallel paths for primary currents are advantageous to reduce the current in each path. This will be demonstrated in the next article in this series.

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The Volksinverter battery converter BCV402 power-transfer circuit is a *boost push-pull* (BPP), although this will undergo some refinement later. While retaining the advantage of push-pull parallelism, the boost or *common-active* (CA) PWM-switch configuration places the converter inductor in series with the input port. The other inductor terminal connects to the center-tap of the transformer primary winding, as shown in the simplified power-transfer circuit diagram of Fig. 2.

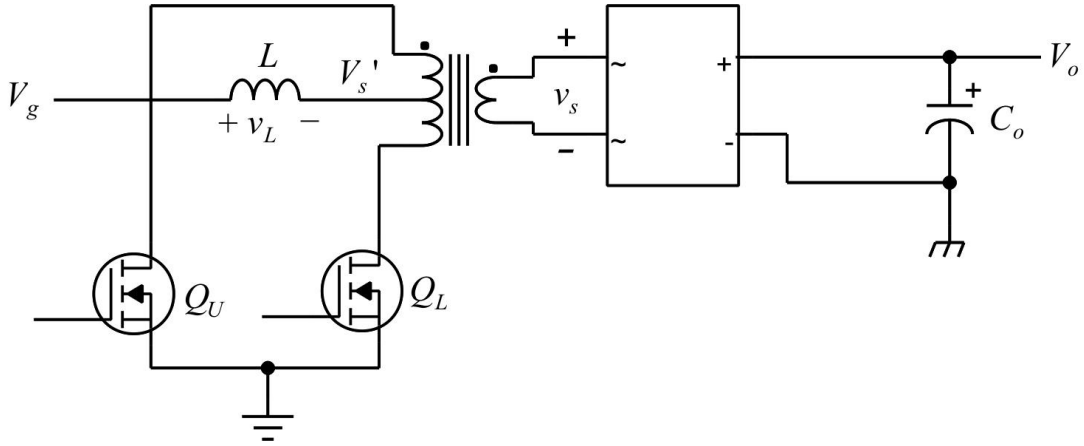

Fig. 2. Boost push-pull (BPP) power-transfer circuit. The center-tapped primary winding is regarded as two coupled primary windings of opposite polarity. V_s' is the secondary winding voltage referred to the center-tap node across one of the conducting primary windings.

The voltage V_s' at the primary winding center-tap is the secondary transformer voltage during off-time referred to the primary circuit. V_s is the secondary voltage amplitude and ' indicates winding-to-winding referral. For steady-state operation and flux balance, $V_s' > V_g$ = VBAT, the input-port (battery) voltage. Although the input current is determined by the input power P_g requirement, there are now three levels of switch current, as shown in the Fig. 3 waveforms diagram of MOSFET switch current i_Q for one of the two primary windings.

In Fig. 3, the upper graph is of the two gate-drive voltages $v_{G\pm}$; when V_G is high, the MOSFET is on. The second graph down is that of $V_s' = n \cdot V_s$, where n is the transformer turns ratio: $n = N_p / N_s$ where N_x is the number of turns. Each of the two primary windings has N_p turns and n applies to each primary winding. Transfer circuit $V_g < V_s$ and $n < 1$. For the BCV402, n = 1/5; V_s' = 170 V/5 = 34 V for a sine-wave output and for a 3HSW, V_s' = 160 V/5 = 32 V.

The third graph shows that the voltage across the off-time switch is $2 \cdot V_s'$. While one switch conducts, across the other primary winding is V_s'. The dots on windings indicate polarity, and the other winding has the same voltage induced into it as the conducting winding, that of V_s'. Then the voltage across the switch of the off winding is twice V_s', as shown in the plot. A major consequence is that neither MOSFET conducts the full RMS input current though they both must sustain twice the peak secondary-referred voltage. They can be lower-current, higher-voltage devices.

The fourth graph is that of input and inductor current. During on-time, both switches Q_U and Q_L are on, shorting the primary and referring that short to the secondary. Each conducting winding induces into the other an opposing voltage, canceling the field and bypassing the magnetizing inductance. The result is 0 V across all the windings. With no voltage across them, i_g increases at a rate determined by input inductor L voltage across it, $v_L = V_g$. Then during off-time, one of the switches is off, V_s' appears across the primary windings, and voltage across the inductor reverses in polarity to

$$V_g - V_s' < 0 \text{ V} \Rightarrow V_s' > V_g$$

The secondary winding and switch current during off-time is shown in the fifth graph as i_s. The sixth and last graph is that of MOSFET switch current i_Q. It has three levels: I_g, $I_g/2$, and 0 A. Slopes are attributed to

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magnetizing current. Transfer current on average is $I_g/2$ during on-time $D{\cdot}T_s$ because the two switches share input current equally from the inductor. In alternate switching cycles, the switches alternate in being on during off-time $D'{\cdot}T_s$. During the time that a switch is off, the other switch conducts the full inductor current of I_g.

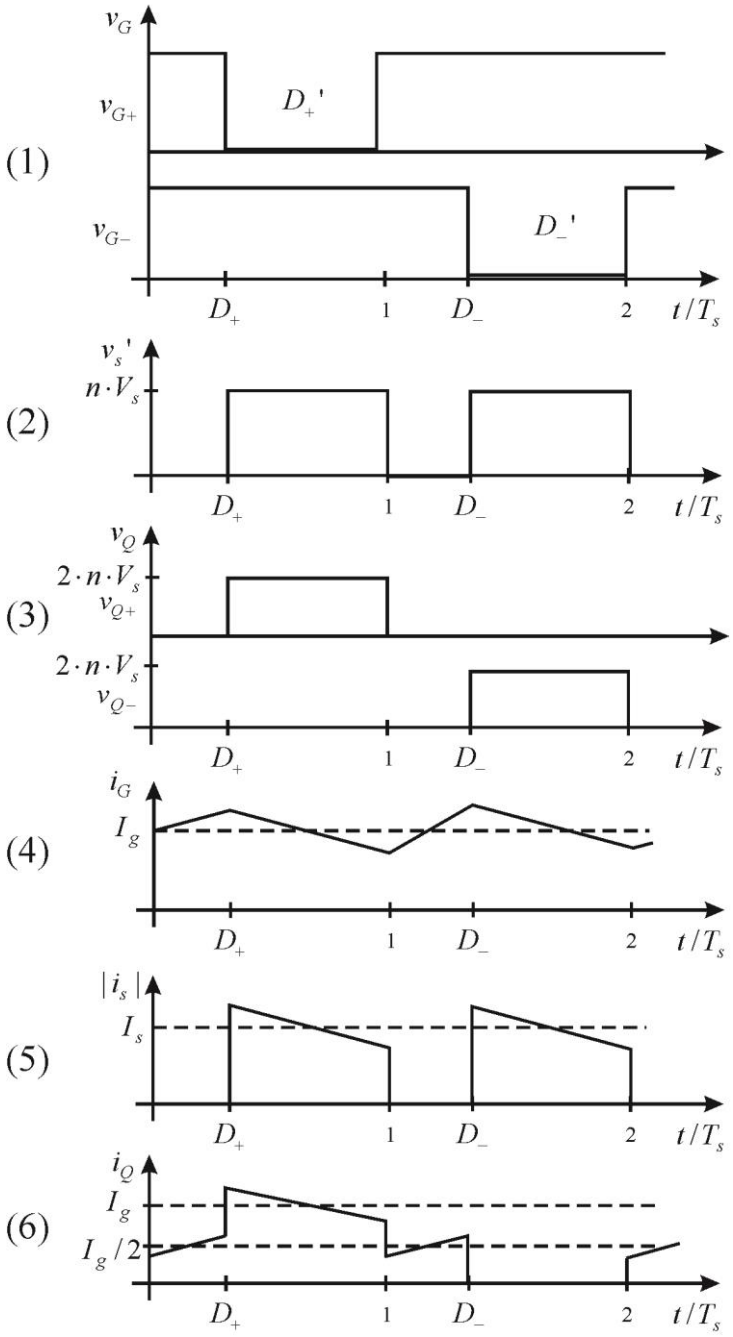

Fig. 3. BPP waveforms. For each magnetic half-cycle, the secondary current i_s has two current levels and is not of the same waveshape as the primary i_Q waveforms, having three non-zero current levels.

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For average inductor current to remain constant in steady-state operation, its per-cycle flux must be zero for flux balance:

$$\Delta\lambda_{on} = -\Delta\lambda_{off} \;\Rightarrow\; V_g \cdot t_{on} + (V_g - V_s') \cdot t_{off} = 0\,\mathrm{V \cdot s} \;\Rightarrow\; V_g \cdot (D \cdot T_s) = (V_s' - V_g) \cdot (D' \cdot T_s)$$

This reduces to the voltage transfer function and duty-ratios, referred to the primary circuit as

$$\frac{V_s'}{V_g} = \frac{n \cdot V_s}{V_g} = \frac{1}{D'} \;\Rightarrow\; \frac{V_s}{V_g} = \frac{1}{n} \cdot \frac{1}{D'} \;\Rightarrow\; D' = \frac{V_g}{V_s'} \;\Rightarrow\; D = 1 - \frac{V_g}{V_s'}$$

The transfer function is for a boost converter with a transformer of turns ratio *n*. The primary turns of *n* are the turns of either of the primary windings because only one of them conducts when transfer to the secondary occurs, though the primary windings are magnetically coupled.

The three-terminal primary-referred equivalent circuit of a transformer is shown in Fig. 4. L_{mp} is the primary-side or primary-referred magnetizing inductance, the mutual inductance of the windings referred to either primary winding. L_{lp} and L_{ls} are the leakage inductances of each primary winding that do not couple to the other windings. The basic voltage and current transfer functions are

$$V_p = V_s' = n \cdot V_s \;;\; I_s = I_p' = n \cdot I_p$$

where I_p and I_s are the primary and secondary winding currents, respectively.

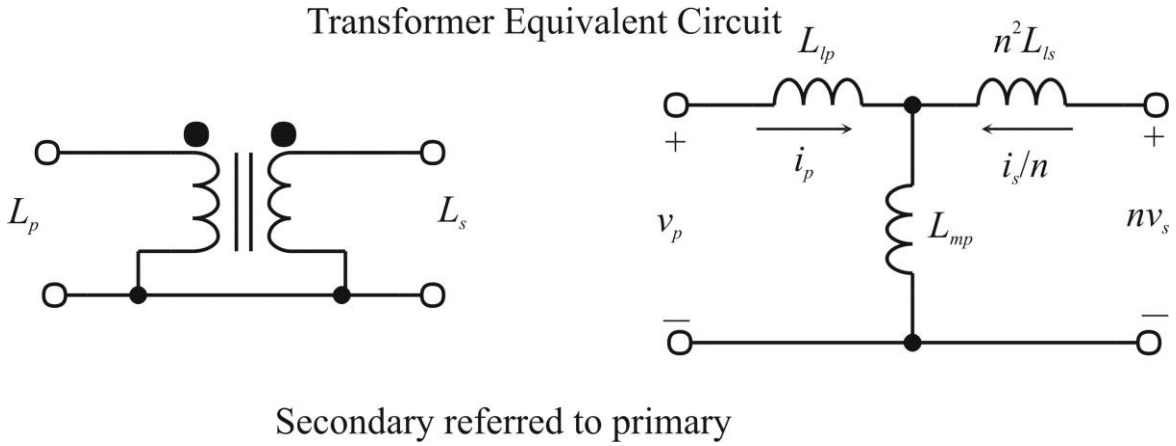

Fig. 4. Equivalent three-node circuit of a transformer with the secondary winding (right side of symbol and model) referred to (or "as viewed from") the primary (left side) winding. In this model, leakage inductances balance: $L_{lp} = L_{ls}' = n^2 \cdot L_{ls}$.

Switch-Loss Minimization

For the BPP transformer, $I_p = I_Q$ and $I_s = n \cdot I_p$. If the input inductor current ripple is small relative to its average value, or $\Delta i_L << \bar{i}_L$, then average input current,

$$\bar{i}_g = I_g \approx \tilde{i}_g$$

where $\tilde{i}_g$ is the RMS i_g. The *form factor* of i_g is

$$\kappa_g = \frac{\tilde{i}_g}{\bar{i}_g} \approx 1$$

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The form factor is a design performance parameter because the RMS value is related to power dissipation while the average value is what is rated in the specifications. $\kappa \geq 1$ and κ ideally is minimum at one but only for a constant waveform. However, constant waveforms do not transfer power through transformers or inductors. The design goal is to minimize κ.

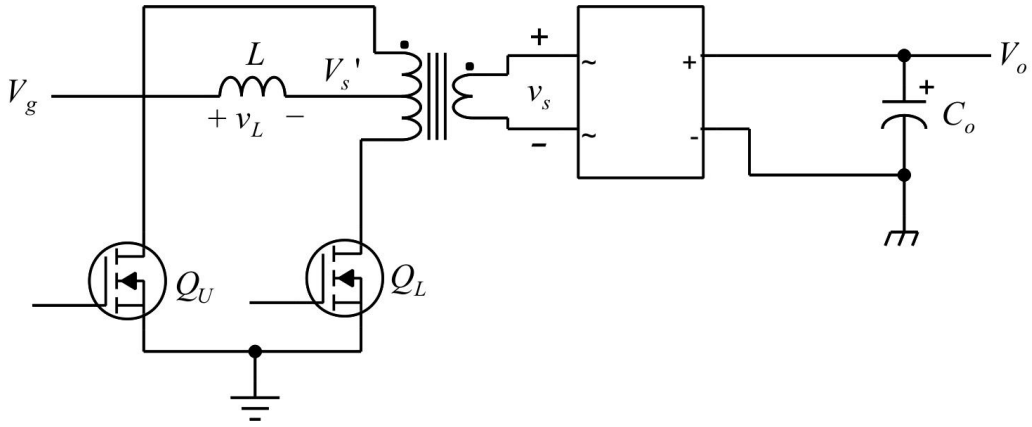
The secondary winding, rectifier diodes, and output are all in series (as suggested by the power transfer circuit in Fig. 2, repeated below for convenience), with current

$$\bar{i}_s = \bar{i}_o = \bar{i}_D = D' \cdot I_s = D' \cdot n \cdot I_p$$

where I_s and I_p are the *on-time average amplitudes* of i_s and i_p, and i_D is the diode current. With small ripple, the secondary current waveforms are approximately square-waves for which the RMS value is

$$\tilde{i}_s = \tilde{i}_D = \tilde{i}_o = \sqrt{D'} \cdot I_s = \sqrt{D'} \cdot n \cdot I_p \;\Rightarrow\; \kappa_s = \kappa_D = \kappa_o = \frac{\tilde{i}_s}{\bar{i}_s} = \frac{\sqrt{D'} \cdot I_s}{D' \cdot I_s} = \frac{1}{\sqrt{D'}}$$

This value of κ_D assumes current through the diode(s) each cycle or else thermally-connected (isothermal) diodes, as in a full-wave (FW) rectifier module or with integrated diodes.



Copy of Fig. 2. Boost push-pull (BPP) power-transfer circuit. The same current flows through the secondary winding, rectifier diodes, and output, such that $\kappa_S = \kappa_D = \kappa_O$ where the goal is to minimize these terms.

On the primary side, because the windings are in series with the switches,

$$\bar{i}_p = \bar{i}_Q = D \cdot \frac{I_g}{2} + \frac{D'}{2} \cdot I_g = \frac{I_g}{2}$$

The first term of $\bar{i}_Q$ is when both switches are on, and the second term is the average current for one switch on each alternating cycle. During off-time, the switch that remains on conducts an average of $D' \cdot I_g$, but this occurs only every other cycle—hence the $D'/2$ in the second term. Therefore, the average switch current is $I_g/2$.

The RMS current is

$$\tilde{i}_p = \tilde{i}_Q = \sqrt{D \cdot \left(\frac{I_g}{2}\right)^2 + \frac{D'}{2} \cdot I_g^2} = \frac{I_g}{2} \cdot \sqrt{D - 2 \cdot D'} = \frac{I_g}{2} \cdot \sqrt{1 + D'} \;\Rightarrow\; \kappa_p = \kappa_Q = \sqrt{1 + D'}$$

Thus, κ_Q is minimized whenever D is maximized and D' minimized.

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The current-waveform power-loss minimization of the primary and secondary windings, as expressed by the form factor of each, is optimum when they are equal, or

$$\kappa_p = \kappa_s \;\Rightarrow\; \sqrt{1+D'} = \frac{1}{\sqrt{D'}} \;\Rightarrow\; D'^2 + D' + 1 = 0$$

Solving the quadratic equation, and given that $0 \le D' \le 1$, the positive root is

$$D'_{opt} = \frac{\sqrt{5}-1}{2} \approx 0.618 \;\Rightarrow\; D_{opt} \approx 0.382$$

D'_{opt} = 1/ D'_{opt} – 1 (where 1/ D'_{opt} is incidentally the Golden Ratio ≈ 1.618). Then $\kappa_p = \kappa_s \approx 1.272$.

A performance parameter for PWM-switch efficiency is the *form-factor product* $\kappa_{QD} = \kappa_Q \cdot \kappa_D$. A minimum κ_{QD} maximizes active and passive switch efficiency in that both κ_Q and κ_D are minimized together. At D_{opt} the BPP

$$\kappa_{QD}(\text{BPP}) = \sqrt{1+D'} \cdot \frac{1}{\sqrt{D'}} = \sqrt{\frac{1+D'}{D'}} \;\Rightarrow \kappa_{QDopt}(\text{BPP}) = \sqrt{\frac{\sqrt{5}+1}{\sqrt{5}-1}} \approx 1.618,\; D_{opt} \approx 0.382$$

This compares somewhat unfavorably with push-pull (PP) choppers, which are the choice in many power inverter designs because of their low cost;

$$\kappa_{QD}(\text{PP}) = \frac{\sqrt{2}}{D} \;\Rightarrow \kappa_{QDopt}(\text{PP}) \approx 1.414,\; D_{opt} = 1$$

The minimum κ_{QD}(BPP) is at D = 0, but this extreme value is hardly feasible as an operating-point because it leaves no lower range below D = 0. The criterion of equal active (Q) and passive (P) switch losses therefore is the choice for the design. Regulated converters operate over a range of D, and as D decreases, κ_{QD}(PP) rises quickly, as shown in Fig. 5. Then κ_{QD}(BPP) < κ_{QD}(PP) for D < 0.69, where the κ_{QD} plots for PP and BPP intersect.

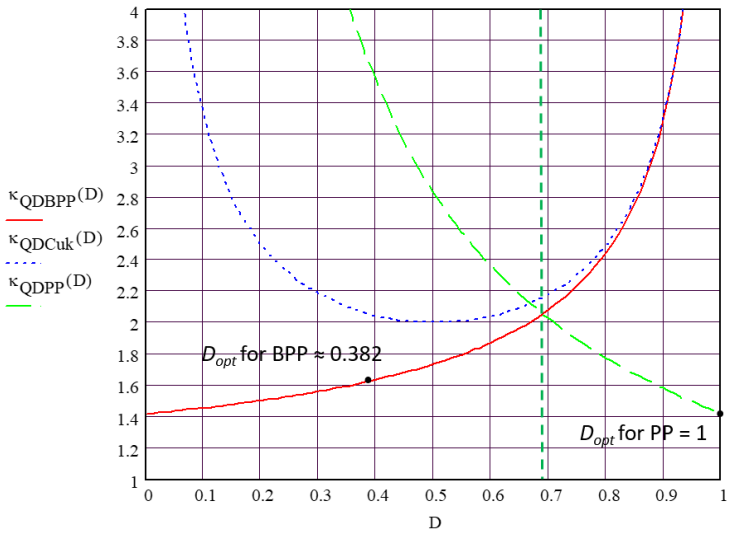

Fig. 5. Switch-loss performance plots of form-factor products κ_{QD}—a performance indicator of switch loss for push-pull chopper (PP), boost push-pull (BPP) and the three PWM-switch circuits including Ćuk-switch circuits (Cuk). Combined switch loss is minimized at lower values of κ_{QD}.

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The BPP minimum κ_{QD} is the same as for the PP, but the BPP operates at lower κ_{QD} over a wider range of D than the PP. The three basic configurations of unipolar PWM-switch power-transfer circuits, including current-steered variations such as the Ćuk-derived circuits, have a minimum $\kappa_{QD} = 2$ at $D = 0.5$. Both of the push-pull circuits have lower switching loss.

In the secondary circuit, the FW rectifier diodes conduct alternating switching cycles that are transformer magnetic half-cycles. If the two diode branches of each conduction half-cycle are discrete and thermally isolated, then

$$\bar{i}_D = \frac{\bar{i}_s}{2} = \frac{D'}{2} \cdot I_s \; ; \; \tilde{i}_D = \sqrt{\frac{D'}{2}} \cdot I_s \Rightarrow \; \kappa_D = \frac{\tilde{i}_D}{\bar{i}_D} = \frac{\sqrt{\frac{D'}{2}} \cdot I_s}{\frac{D'}{2} \cdot I_s} = \sqrt{\frac{2}{D'}}$$

The diode RMS current rating is thus

$$\tilde{i}_D = \sqrt{\frac{D'}{2}} \cdot I_s = \sqrt{\frac{D'}{2}} \cdot \frac{\bar{i}_s}{D'/2} = \frac{1}{\sqrt{2}} \cdot \frac{\bar{i}_s}{\sqrt{D'}} \approx (0.7071) \cdot \frac{\bar{i}_s}{\sqrt{D'}}$$

The switching loss, as expressed by the form factor of each, is minimized whenever

$$\kappa_Q = \kappa_D \Rightarrow \sqrt{1+D'} = \sqrt{\frac{2}{D'}} \Rightarrow D'_{opt} = 1$$

Thus the form-factor product for thermally isolated diodes is

$$\kappa_{QD} = \sqrt{1+D'} \cdot \sqrt{\frac{2}{D'}} = \sqrt{2} \cdot \sqrt{\frac{1+D'}{D'}} \Rightarrow \min \; \kappa_{QD} = 2, \; D'_{opt} = 1$$

Consequently, thermally-shorted (isothermal) FW rectifiers and not thermally-isolated diode rectifiers have less switch-loss than unipolar PWM-switch converters.

Switch power-loss minimization is only one optimization for the BPP power-transfer circuit. Another is the choice of V_s' that minimizes the size of the magnetic components, a task also to be addressed later in this series.

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About The Author



Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.

For further reading on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC power inverters."

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