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New JEDEC Guidelines Help Designers To Realistically Predict Stability Of SiC MOSFETs In Applications

by Thomas Aichinger, Infineon Technologies, Villach, Austria

With the recent publication of JEDEC guidelines for SiC MOSFETs in January and February, the promised benefits of silicon carbide (SiC) MOSFETs can now be fully realized and consistently demonstrated through recognized industry guidelines.[1,2] Concurrently, newly introduced high-voltage (1200-V) SiC MOSFETs have improved threshold voltage stability that can be validated by the new testing procedure. Systems engineers that have previously evaluated SiC MOSFETs and observed somewhat different threshold voltage (V_{TH}) variations compared to silicon (Si) MOSFETs now have an answer on how to measure V_{TH} reproducibly in pristine devices and what is the worst-case drift of critical electrical parameters that can be expected in different SiC MOSFET applications.

Those who have yet to evaluate SiC as a replacement for silicon MOSFETs can confidently compare the alternative and take advantage of the high thermal conductivity, energy efficiency and operating frequency, and low thermal expansion of these wide-bandgap devices. This article will provide background on the SiC market, discuss the JEDEC guidelines and testing performed by Infineon and conclude with details on newly implemented test procedures.

The Growing Demand For SiC MOSFETs

These SiC advantages are causing fast migration as customers adopt the technology quickly. The market growth rate was 22.8% from 2021 to 2022,[3] and the SiC market is expected to reach $2.1 billion U.S. by 2026 from $1.1 billion U.S. in 2022.

Compared to silicon MOSFETs, SiC devices offer several advantages such as wide bandgap, high drift velocity, high breakdown voltage, large critical electrical field and high thermal conductivity. They are also capable of working at higher current densities and temperatures.

Growing implementation of SiC devices is occurring in automotive applications due to the increasing demand for hybrid and electric vehicles. Also, the increasing need for efficient industrial operations is creating a strong demand for SiC in factories.

New JEDEC Guidelines And SiC

Based on engineers' observations that fully reversible and more permanent threshold-voltage variations occur with SiC MOSFETs, JEDEC developed "Guidelines for measuring the threshold voltage (V_T) of SiC MOSFETs," JEP183A, and "Guideline for Evaluating Gate Switching Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion," JEP195. These guidelines combined with extensive investigations at Infineon provide deep insight into characterization and long-term parameter stability of SiC MOSFETs that has resulted in a greater understanding and new test methods.

A stable and reproducible measurement of V_{TH} is needed to define the datasheet values of "pristine" devices—these are parts that may have been tested but have not yet been used extensively or stressed. Also, it is mandatory for assessing V_{TH} evolution in a stress experiment. Silicon MOSFETs do not require any particular precautions. Pristine silicon power transistors always show the same V_{TH}.

In contrast, SiC MOSFETs have a V_{TH} that is not constant. Measurements of V_{TH} show different values when the transistor turns on, coming from a negative gate voltage and when it turns off, coming from a positive gate voltage (see Fig. 1). This V_{TH} hysteresis is the difference between the V_{TH} during turn-on, the upsweep V_{TH} (V_{TH-UP}), and V_{TH} during turnoff, the downsweep V_{TH} ($V_{TH-DOWN}$).

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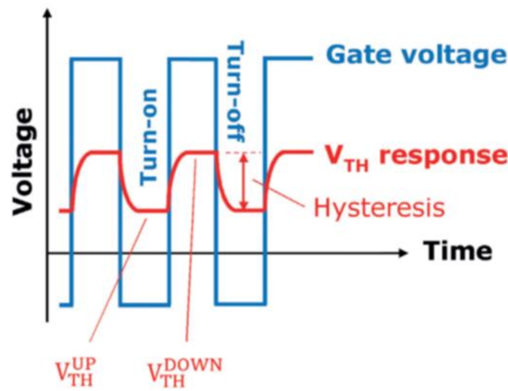

Fig. 1. The threshold voltage dynamics of a SiC MOSFET when switching the gate of a pristine device in bipolar mode.

Hysteresis is the largest when sweeping the gate between deep accumulation and deep inversion, for example, between -10 V and +15 V. Fig. 2 shows typical transfer characteristics of SiC MOSFETs for fast upsweeps and downsweeps of the gate voltage. Hysteresis reduces when the upsweep starts at voltages closer to 0 V and when sweeping is slower. Investigations suggest that these effects are due to short-term charging and discharging of preexisting traps located near or directly at the SiC/gate-oxide interface.

The upsweep V_{TH} is always lower because the interface is charged positively in the negative half period of the gate pulse due to holes captured from the valence band. Meanwhile, the downsweep V_{TH} is always larger because the interface is charged neutrally or even negatively in the positive half period of the gate pulse due to electrons captured from the conduction band. Within the hysteresis envelope, there is a continuum of possible V_{TH} values due to the large variety of capture and emission time constants for trapped charges in the virtually continuous defect band.

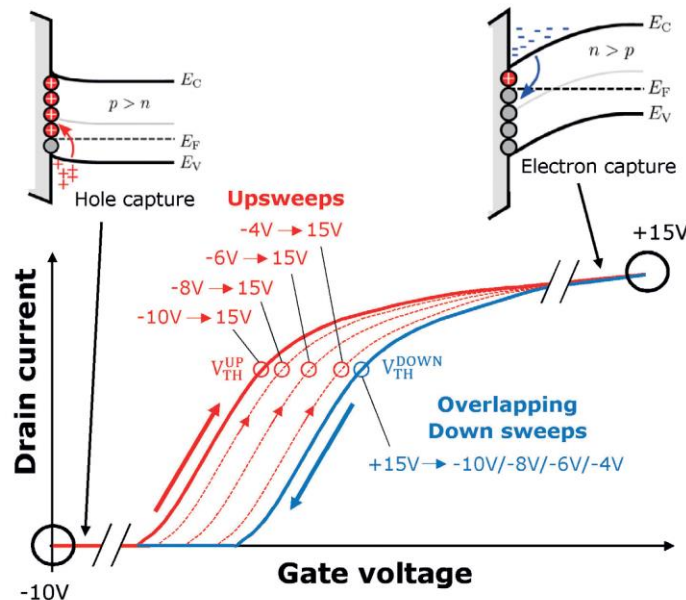

Fig. 2. Transfer characteristics vary during turn-on and turn-off. V_{TH} is lower during turn-on due to holes captured at negative gate bias. During turn-off, V_{TH} is higher due to electrons captured at positive gate bias.

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Improving Gate-Switching Stability

One consequence of these findings is that the gate biasing history of the SiC MOSFET can impact V_{TH} measurements for a very long time. For instance, when the device is either floating or biased at V_{GS} = 0 V after the application of a positive or negative gate pulse, charges that are trapped near the mid-gap may be stored at the interface for hours, days or even longer.

This stored charge keeps the device in a state of non-equilibrium. It results from the large thermal emission barriers associated with the wide bandgap of SiC. A comparable effect in silicon MOSFETs does not exist because they have a lower density of interface traps and a narrower bandgap.

Based on these observations, obtaining reproducible V_{TH} measurements with a SiC MOSFET begins by defining a gate-biasing history. One option is to apply a short positive gate pulse to the device using gate voltages between the recommended use voltage and the maximum allowed voltage in the datasheet (see Fig. 3). This technique is called gate conditioning. Once undertaken, V_{TH} must be measured with a constant time delay.

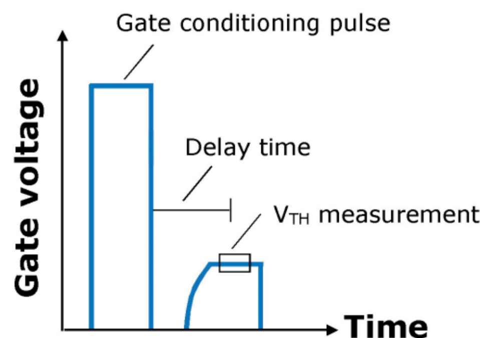

Fig. 3. An example of gate conditioning. Before measuring the V_{TH}, a positive gate pulse is applied for several milliseconds to bring the MOS interface to a defined charged state.

An easy way to accomplish fast, well-timed V_{TH} spot measurements is to use a gated-diode measurement scheme. Here, the gate and drain terminals of the device are shorted, the source terminal grounded and a forced threshold current, for example 1 mA, is applied. Eventually, this gate-conditioning procedure creates a defined, reproducible charge state at the SiC/gate-oxide interface and enables a defined, reproducible V_{TH} measurement.

Infineon research that is consistent with recent guidelines published by JEDEC showed that more-complex conditioning procedures, involving negative and positive gate-conditioning pulses, also allow for reproducible measurements of hysteresis.[4]

With the process for measuring V_{TH} in an accurate and reproducible manner defined, the next challenge was controlling and assessing V_{TH} instabilities in SiC MOSFET operations. This was accomplished by developing a stress procedure for determining worst-case V_{TH} drifts for different application profiles.

Two more potentially application-relevant stressors were tested: the drain voltage and the load current. These studies revealed that neither led to altered V_{TH} instabilities. The negative results allow a drastic simplification of the stress procedure without neglecting any important V_{TH} stressors present in real applications.

Another critical finding was the noticeable impact of the V_{TH} increase on the $R_{DS(ON)}$ that differs among the voltage classes of the devices. The higher the voltage class, the more pronounced is the contribution of the thicker epitaxial layer's resistance. However, with M1H technology developed through the increased understanding of charge trapping phenomena and engineering of the SiC/gate-oxide interface, recently introduced 1,200-V CoolSiC MOSFETs excel in overall V_{TH} stability.

The end results of this extensive testing were that M1H technology was found to improve gate switching instability and enlarge the recommended gate-driving window. Applying the new test and stress guideline, CoolSiC MOSFET M1H devices demonstrate significant improvements in overall V_{TH} stability. In particular, the application relevant drift caused by dynamic bipolar gate switching has been reduced significantly.

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As a consequence, the M1H technology offers the full window of gate voltages, even down to -10 V at the highest switching frequencies. The larger gate operation window provides maximum flexibility to customers and a high level of robustness against driver- and layout-related voltage peaks at the gate, with no restrictions towards higher switching frequencies.

Finally, Infineon provides parameter drift evolution curves in app notes accompanying datasheets. These curves allow customers to directly extract the maximum drift that they can expect worst-case for a given technology during a specific application. Now, system designers can benefit from new test and stress procedures for SiC MOSFETs as well as predictability that can realistically determine their worst-case threshold voltage variations.

Conclusion

With an increased understanding of trapping dynamics at SiC's gate-oxide interface, new characterization and stress procedures have been developed specifically for SiC MOSFETs. These new methods provide standardized, reproducible measurements, as well as realistic assessments of time-dependent parameter variations in real applications.

Now, engineers can predict how device characteristics will evolve during an application—even those applications that require 1,200-V SiC MOSFETs and very demanding requirements such as automotive. This paves the way for SiC MOSFETs to reach their next level of quality excellence and achieve projected market growth targets.

Reference

1. Guidelines for Measuring the Threshold Voltage (VT) of SiC MOSFETs | JEDEC, Jan 2023.
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3. "Silicon Carbide Market by Device (SiC Discrete, SC Bare Die, and SiC Module), Wafer Size, Application, Vertical (Power Electronics, Automotive, Telecommunications, and Energy & Power), and Geography, 2026," report by Markets and Markets.
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About The Author

Since 2012 Thomas Aichinger has been part of the SiC MOSFET technology development team at Infineon Technologies, where he currently serves as lead principal engineer for SiC development. Thomas has been serving on the technical committee of IRPS and WiPDA and is currently serving as task group co-chair within the JEDEC sub-committee JC.70.2 focusing on SiC Power Electronic Conversion Semiconductor (PECS) standards. In addition, he has contributed to more than 80 scientific publications including journal articles, conference papers and book chapters. Prior to joining Infineon, Thomas was a postdoctoral researcher at Penn State University. He received his Ph.D. in electrical engineering from the Technical University of Vienna.

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