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Meeting The Challenges Of USB-PD Extended Power Range With An Asymmetrical Half-Bridge Flyback Topology

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The new USB-PD Extended Power Range (EPR) standard is designed to enable a universal power supply capable of charging a wide range of devices, from handheld smartphones and laptops to power tools and e-bikes. However, supporting a variable output voltage from 5 V to 48 V at up to 5 A while maintaining high conversion efficiency raises new challenges for engineers. Further complications arise from the need to also maintain a small footprint, accept a wide input voltage, provide power factor correction (PFC), support standby power modes, and dissipate heat only through passive cooling.

This article describes how a hybrid flyback topology meets the requirements of the USB-PD EPR standard while achieving a full load efficiency of up to 96.84% across an input voltage range of 90 to 265 Vac and a power density of 44 W/inch^3. The discussion begins with a look at the existing power supply architectures that were initially considered by Infineon to meet USB-PD EPR power supply requirements, and the limitations those topologies imposed. Then a new architecture based on the hybrid flyback topology is introduced and its key characteristics are described.

One of the drawbacks of the hybrid flyback is its longer demagnetization times at lower output voltages, leading to difficulties in making it resonant. A technique for addressing this issue using the flyback effect to transfer magnetizing energy to the secondary side is described. Finally, efficiency results are presented for a 240-W power supply prototype that provides a USB-PD EPR output from 5 V to 48 V. Design choices to optimize efficiency and the controller choice are noted.

Possible Architectures

There are several architectures that can be considered for a USB-PD EPR power supply. Implementing a PFC-stage followed by a flyback-based converter (see Fig. 1) provides a highly flexible architecture in terms of input and output voltage range. However, the large size of the transformer leads to a bulky form factor. In addition, a high reflected voltage appears across the primary switch.

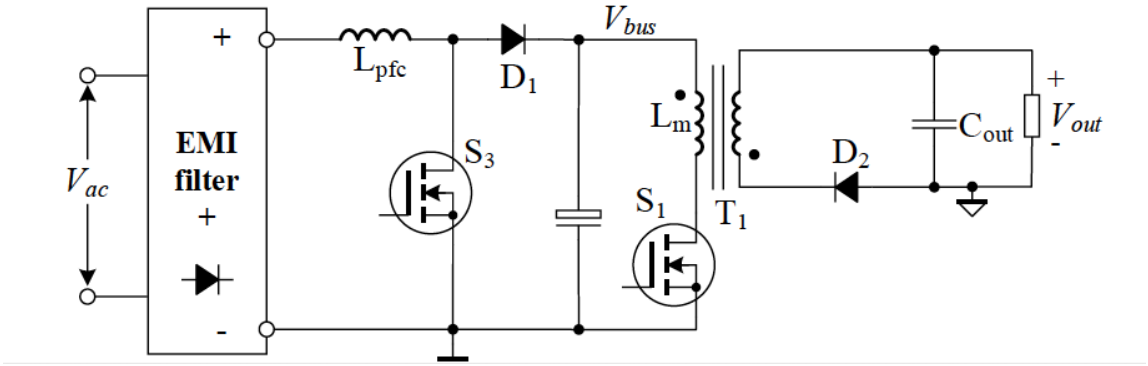

Fig. 1. PFC + flyback topology.

Alternatively, the PFC-stage can be followed by an LLC-based converter (see Fig. 2). This architecture is compact and efficient but is limited in terms of output voltage. A third power stage, such as a buck converter, is needed to achieve the required output voltage range. This leads to a bulky and expensive system. In addition, three power stages make it challenging to meet USB-PD EPR standby power requirements.

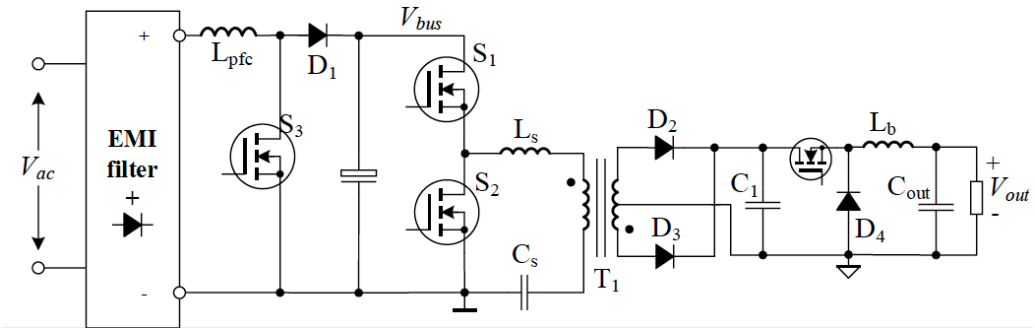

Fig. 2. PFC + LLC + buck topology.

To address all USB-PD EPR requirements in an optimum way, a new architecture, combining the advantages of the flyback and LLC converters is proposed (Fig. 3). In such an architecture, the PFC-stage is followed by an asymmetrical half-bridge flyback converter, also known as a hybrid flyback. With proper control methods, including the modulation of V_{bus} and the use of GaN switches, the proposed architecture can serve as a universal power supply providing excellent efficiency across the range of output voltages.

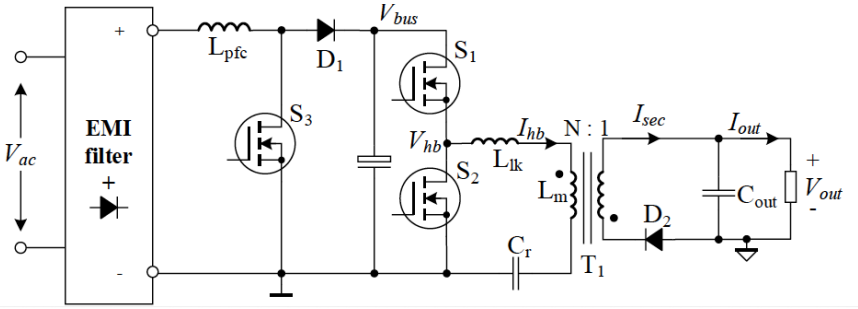

Fig. 3. PFC + asymmetric half-bridge flyback (hybrid flyback) topology for USB-PD EPR power supplies.

Proposed Architecture For USB-PD EPR

The proposed architecture consists of two stages: an ac-dc PFC boost stage using active bridge rectification and a dc-dc hybrid flyback (Fig. 4). Synchronous rectification is applied at the output. The XDPS222x combo controller from Infineon controls both the PFC and hybrid flyback.

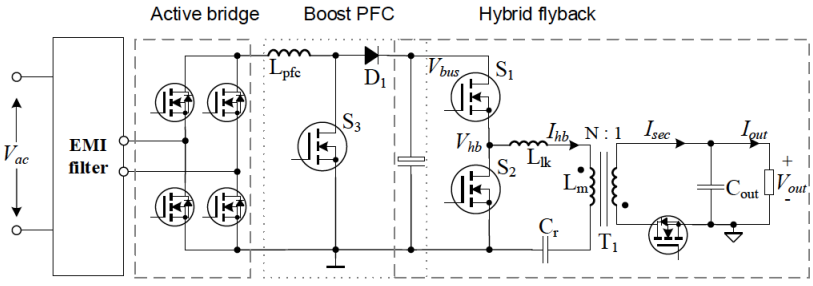

Fig. 4. In the proposed architecture, an active bridge rectifier is followed by a boost PFC. The dc-dc stage is a hybrid flyback. The XDPS222x combo controller from Infineon controls both the PFC and hybrid flyback.

A key feature of this approach is that since the first stage can provide the optimal voltage (V_{bus}) for the second stage, it maximizes the forward energy transfer of the asymmetrical half-bridge flyback. In addition, the synchronous active bridge helps to achieve high efficiency to lower the heat dissipation.

The amount of energy transfer in forward mode across the dc-dc stage depends on the average voltage of the resonant capacitor (V_{cr}). For example, for 48-V output and 400-V input, a V_{cr} of ~200 V results in a ratio of 50% forward energy transfer which helps to reduce the transformer size and increase the efficiency. At low

output voltage, because V_{cr} is much lower than V_{bus}, the PFC can be turned off to maximize efficiency. V_{bus} can also be modulated as a function of the output voltage for optimum performance.

Because of the nature of a flyback converter, the discharge time of the main transformer magnetizing current is inversely proportional to the output voltage. This means that when the supply is optimized for 48 V, the resonant tank may not be optimal for low output voltages because of longer demagnetization time. This leads to multiple oscillations of the resonant tank where part of the energy flows back and forth between the magnetizing inductance and resonant capacitor.

Such oscillations result in a pulsating secondary current and circulating energy, resulting in extra losses and suboptimal efficiency. Even if ceramic capacitors are used, the capacitance increase due to the lower dc voltage cannot fully compensate for the longer demagnetization time. In addition, if an SR controller is used, it may turn off after the first current pulse if the current reaches zero. Furthermore, the secondary ZCS may be lost if the LS (low-side switch) turns off while there is still secondary current flow.

The Flyback Effect

To eliminate extra circulating energy on the primary side at low output voltage, the magnetizing energy must be transferred to the secondary side. A straightforward way to do this is to open the primary-side current loop to ensure magnetizing current can only flow to the secondary side. However, the energy stored in the resonant capacitor needs to be transferred to the secondary side as well. To achieve this, the primary-side circuit can only be opened after the resonant capacitor has transferred all possible energy but before it charges again.

The optimal time to open the primary-side circuit is when the primary-side current is increasing and reaches zero (L_{lk} current equals zero). This avoids possible ringing from remaining current in the leakage inductance. Fig. 5 shows how the magnetizing current decreases linearly and flows to the secondary stage as it does in a flyback converter. This is why this is called the flyback effect.

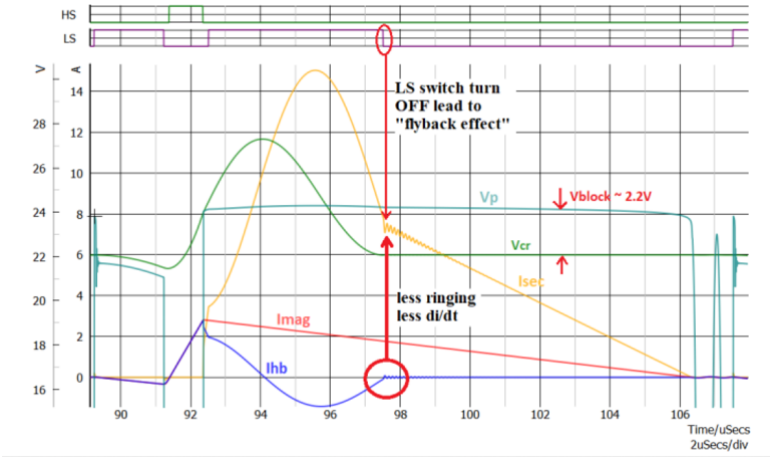

Fig. 5. Simulation of flyback effect waveforms showing the optimal time to open the primary current path (when I_{hb} reaches zero).

Bidirectional switches can be used to open the primary current loop to ensure that current flows to the output capacitor. However, in addition to increasing cost, this approach can lead to other effects arising from the missing clamping structure such as the "body diode" commonly found in non-bidirectional switches.

Alternatively, the flyback effect can be achieved by providing a minimum blocking voltage on the primary side. When the primary loop is open, the reverse voltage that appears across the low-side switch is the difference between the transformer primary voltage and the resonant capacitor (V_{block} in Fig. 5).

Using GaN HEMTs allows for modulation of the gate voltage to increase and guarantee the required blocking voltage during the off phase. Fig. 6 shows the resulting equivalent circuit when the LS switch goes off. The resonant tank formed by L_{lk} and C_r can ensure small variations of V_{cr} by maximizing C_r and minimizing L_{lk} within the same resonant period. This, in turn, minimizes the required V_{block}.

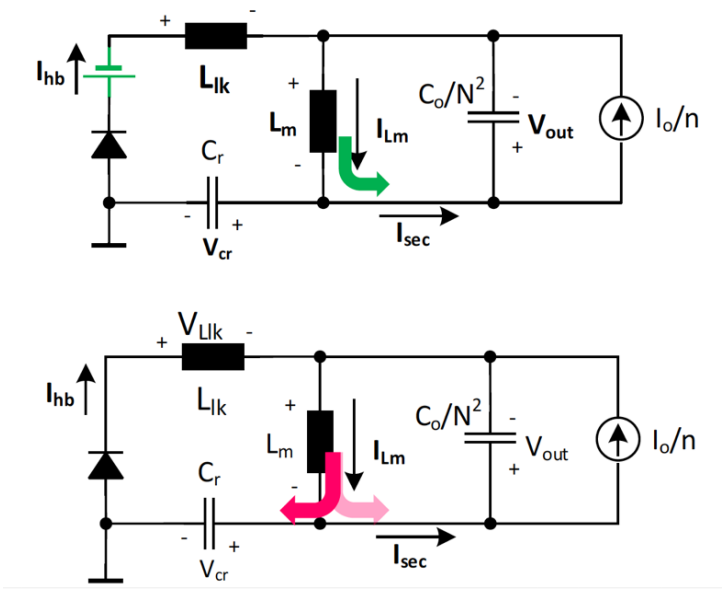

Fig. 6. Equivalent circuit when the LS switch goes off. Top: GaN switch case. Bottom: silicon switch case.

For example, the circuit shown in Fig. 6 can ensure the primary-side loop will not conduct any current if the LS switch provides a blocking voltage higher than 2.2 V. Note that care needs to be taken on the RC network to drive the LS GaN HEMT to ensure sufficient negative gate voltage during demagnetization of the transformer.

A silicon MOSFET can be used for the LS switch, as the body diode structure may allow the primary current to flow in the positive direction after it switches off, eventually charging the resonant capacitor. The secondary side will clamp the transformer voltage once V_{cr} is high enough, taking the rest of the magnetizing energy to achieve a partial flyback effect.

Efficiency

Fig. 7 shows the full load efficiency of the proposed architecture, including the hybrid flyback as dc-dc converter, across input voltage. Efficiency is 96.8% at 230 Vac and over 95% for Vac higher than 100 Vac. Fig. 8 shows the efficiency at 5-A loading across output voltage. Notice how the flyback effect is particularly pronounced at low output voltages, providing an efficiency gain from 1% to 2%.

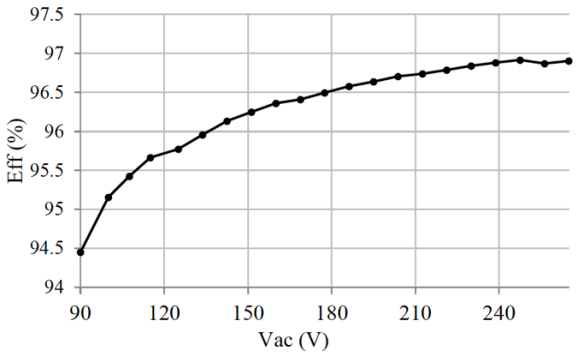

Fig. 7. Full load efficiency of the hybrid flyback topology across input voltage.

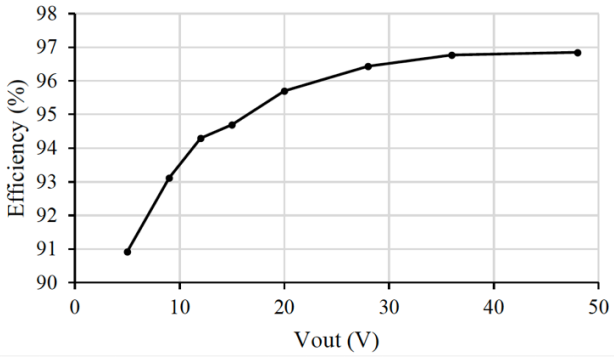

Fig. 8. Efficiency of the hybrid flyback topology at 5 A across output voltage.

These figures were measured from an ac-dc 240-W power supply prototype using GaN switches for the dc-dc stage and providing a USB-PD EPR output voltage from 5 V to 48 V (Fig. 9). To maximize efficiency over the entire ac input voltage range, the input bridge rectifier was replaced by an active bridge. Synchronous rectification was used at the output of the dc-dc stage. The design is built around the XDPS2222 PFC and hybrid flyback controller from Infineon. The dimensions of the prototype are 110 x 40 x 20 mm, resulting in a power density of 44 W/inch^3.

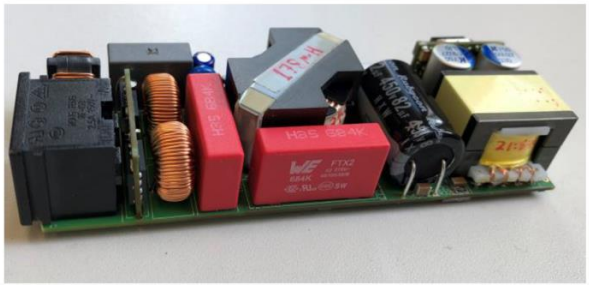

Fig. 9. A 240-W ac-dc GaN USB-PD EPR power supply prototype built around the XDPS2222 PFC and hybrid flyback combo controller and CoolGaN power switches from Infineon.

The hybrid flyback topology helps engineers meet USB-PD EPR requirements while maintaining high efficiency with high energy density across both a wide V_{in} and V_{out} range. Combining the PFC boost with an asymmetrical half-bridge converter maximizes forward energy transfer in a compact and efficient design with small magnetic size. Use of the flyback effect through GaN devices manages the hybrid flyback nature of the dc-dc converter in an optimal manner to improve efficiency at low output voltages as well.

About The Authors

Alfredo Medina-Garcia currently serves as a lead principal engineer in the innovation department for power conversion at Infineon Technologies in Munich, Germany, and has been with the company since 2004. His research focus is on highly efficient power converters with high power density, and control algorithms in the area of ac-dc power adapters. Medina-Garcia has contributed to several patents and scientific publications. He received a B.Sc. degree in industrial engineering from the University of Cordoba, an M.Sc. degree in telecommunication engineering from the University of Sevilla, and an M.Sc. degree and a PhD in electronic engineering from the University of Granada.

Martin Krueger joined Infineon in 1999 and since 2006 has been working on digital control of power for TV supplies, PC silver boxes, chargers, and adapters. He has contributed to many patents and publications. Krueger received a master's degree and a PhD degree, both in electrical engineering from Bochum University, Germany.

Markus Schmid currently serves as a lead principal engineer and heads the Technical Marketing Team for SMPS at Infineon Technologies. He joined Infineon in 2014 as an application engineer for switch-mode power supply design. Previously, he worked in power supply design for NMB Minebea. Schmid has contributed to several patents and scientific publications. He received Dipl.-Ing. and Ph.D degrees in electrical engineering from the University of Erlangen-Nuremberg, Germany.

Josef Daimer is currently the director for system engineering at Infineon Technologies where he is leading a team in Munich working on innovative SMPS solutions. Over the last 12 years he has served as a manager for system engineering for SMPS application teams in Singapore and Munich. Daimer has more than 30 years' experience in power semiconductors. He graduated as a diplom engineer (FH) for electrotechnics from Landshut University.

Manfred Schlenk provides consulting services at Dr. Schlenk Consulting in Ausburg, Germany. He has over 42 years of experience in the field of power conversion and motor control, with a focus on resonant converters and magnetics. Schlenk has co-authored over 30 patents in the field of power conversion and its control methods, and has contributed over 40 publications scientific in the field of power conversion and motor control. He is a senior member of IEEE and a vice chair of EPSMA. Schlenk received an M.Sc. degree in electrotechnics engineering from the Technical University of Munich and a Ph.D. degree from the Technical University of Berlin.