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Designing An Open-Source Power Inverter (Part 14): Boost Push-Pull Or Buck Bridge?

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In the last installment in this series,[1-13] we considered an alternative to the boost push-pull (BPP) topology that was previously selected for the power transfer circuit in the Volksinverter's battery converter stage (Fig. 1). The new circuit under consideration was the differential boost push-pull (DBPP), and our analysis led us to conclude that BPP and DBPP are very comparable in performance with each having slight advantages, depending on the priorities of the application. These two topologies can be referred to collectively as the common-active push-pull or CA-PP.

Nevertheless, the BPP and the DBPP are not our only options. In the ongoing search for the optimal power-transfer circuit for the Volksinverter, this article compares the differential boost push-pull (DBPP) power-transfer circuit of part 13 to a bridge-switched common-passive or buck (CP-BRG) transfer circuit to determine whether the DBPP and BPP (i.e. the CA-PP) or the CP-BRG has lower loss as a low-R_g power-transfer circuit. This comparison of the CA-PP with the CP-BRG is motivated in part by the popularity of the full-bridge buck circuit, which will be familiar to designers because of its common use in inverters.

Note that the DBPP is used as the initial point of reference here because it was most recently discussed in the last part. However, it is similar enough to the BPP that the comparisons here with the CP-BRG apply to both circuits. And we'll present performance data for all three topologies, which illustrates this point.

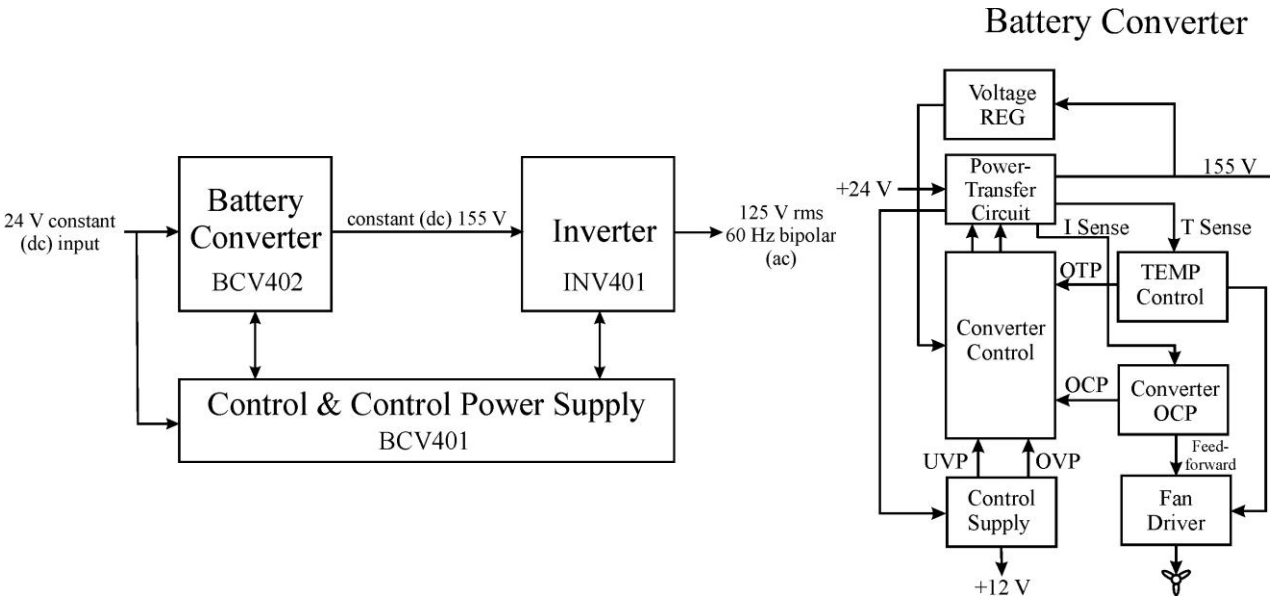


Fig. 1. The Volksinverter's system block diagram (left) and the BCV402 battery converter stage block diagram (right). Continuing the search for the optimum power transfer circuit, in this part we seek to determine whether a bridge-switched common-passive or buck (CP-BRG) transfer circuit might offer advantages over the boost push-pull (BPP) and differential boost push-pull (DBPP) circuits previously discussed.

Buck-Bridge And Boost-Push-Pull Performance Comparisons

As a starting point, let's recall the transfer circuit of the DBPP from part 13, Fig. 2, which is repeated here in Fig. 2.

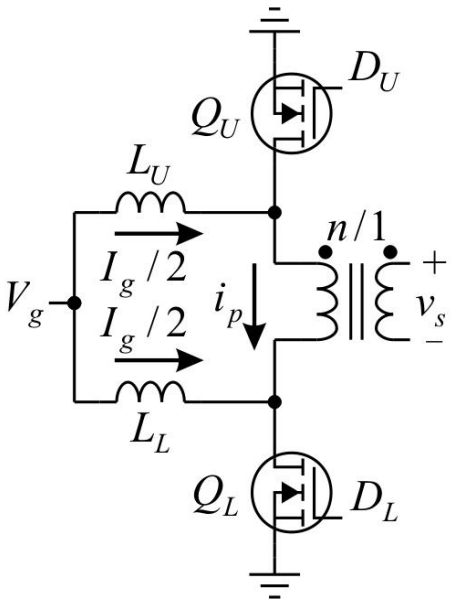


Fig. 2. The interleaved or differential boost push-pull (DBPP) primary circuit. A BPP primary winding is traded for an extra inductor. The switch formulas are the same but the primary winding current waveforms are different.

Another popular transfer-circuit alternative to the CA-PP (either BPP or DBPP) is the transformer-coupled PWM-switch CP or buck full-bridge circuit, shown in Fig. 3. The full-bridge avoids the half-bridge complication of the capacitive branch but adds two additional switches. Two switches conduct in series for a circuit switch resistance of $2 \cdot r_{on}$.

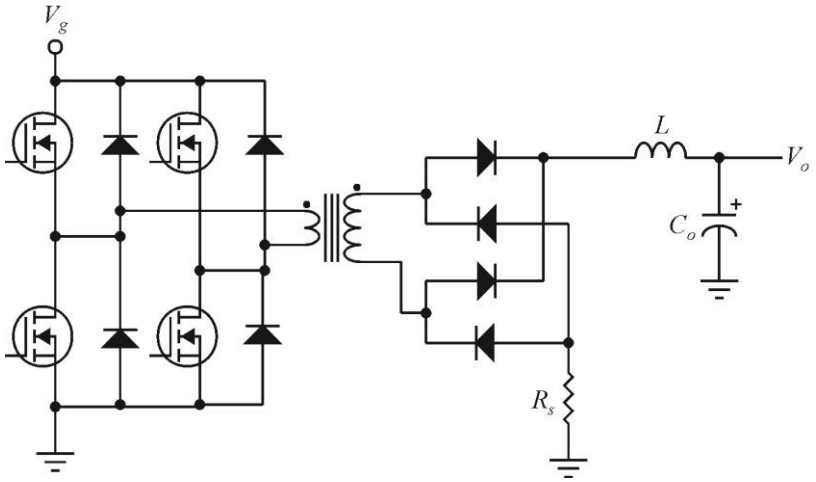


Fig. 3. CP (buck) full-bridge (CP-BRG) power-transfer circuit. The transformer windings are fully utilized. Output inductor current forces the secondary winding to be shorted during off-time as both branches of the FW rectifier conduct. On-time primary winding voltage is V_g and switch current from V_g is the transformer primary current.

A full-bridge is chosen over a half-bridge because in a half-bridge, switches conduct $2 \cdot I_g$ when input current I_g is already high, and the series resistance of the capacitive branch is not as low as r_{on} of high-current MOSFETs. The half-bridge drives the primary winding with half the voltage and twice the current of the full-bridge—the opposite of what is needed for a high-I_g, low-R_g circuit if the goal is to minimize losses. However, full-bridge switches conduct the full input current of I_g.

The rationale for preferring the *boost push-pull* (CA-PP)— whether DBPP or BPP—over a *buck-bridge* (CP-BRG) transfer-circuit topology is the reduction of currents in power components, notably switch and transformer primary-circuit currents, to reduce winding and switch conduction loss and power-component count and cost. High input current in a CP-BRG requires careful attention to circuit-board trace ampacity, input-port lead inductance, and input capacitor C_i heating. In the DBPP, only the input connectors and fuses conduct the full-scale current; the inductors, switches, and primary winding(s) have higher voltage, lower current ratings. In the BPP, fuse and inductor conduct the full I_g.

Transfer-circuit design equations for both CA-PP and CP-BRG assume transformer magnetizing current $i_{mp} << i_p$ and that $i_m \approx 0$ A (small-ripple approximation). The CP-BRG transfer-circuit design formulas are thus

$$M(\text{CP}) = \frac{V_s}{V_g} = \frac{1}{n}\cdot D\ ,\ V_s' = n\cdot V_s \Rightarrow \frac{V_s'}{V_g} = D\ ;\ \text{avg on-time } v_s = V_s$$

$$\bar{i}_g = \left|\bar{i}_p\right| = I_g\cdot D\ ;\ \tilde{i}_p = I_g\cdot\sqrt{D}\ ,\ I_g = \text{avg on-time } i_g$$

$$\bar{i}_Q = I_g\cdot\frac{D}{2}\ ;\ \tilde{i}_Q = \sqrt{I_g^2\cdot\left(\frac{D}{2}\right)} = I_g\cdot\sqrt{\frac{D}{2}}$$

$$\left|\bar{i}_s\right| = \bar{i}_L = \bar{i}_O = D\cdot I_s = n\cdot I_p\cdot D\ ;\ \tilde{i}_s = n\cdot\tilde{i}_p = n\cdot I_g\cdot\sqrt{D}\ ;\ \tilde{i}_O = \tilde{i}_L \approx \bar{i}_s$$

$$\left|\bar{i}_D(\text{FW})\right| = \begin{cases} I_s\cdot\dfrac{D}{2}, \text{diodes thermally isolated} \\ I_s\cdot D, \text{diodes themally shorted} \end{cases}\ ;\ \tilde{i}_D(\text{FW}) == \begin{cases} I_s\cdot\sqrt{\dfrac{D}{2}}, \text{diodes thermally isolated} \\ I_s\cdot\sqrt{D}, \text{diodes themally shorted} \end{cases}$$

$$\Rightarrow \kappa_p = \kappa_s = \frac{1}{\sqrt{D}}\ ;\ \kappa_Q = \kappa_D = \frac{1}{\sqrt{D}}, \text{ diodes thermally shorted}^{[14]}$$

$$\kappa_{ps} = \frac{1}{D}\ ;\ \kappa_{QD} = \frac{1}{D}\ ;\ \kappa_{CP} = \kappa_{QD}\cdot\kappa_{ps} = 1/D^2.$$

where κ_p = form factor of transformer primary, κ_s = form factor of transformer secondary, κ_Q = form factor of active switches (transistors) and κ_D = form factor of passive switches (diodes).

The CA-PP circuits bypass the design complication of full I_g by effectively transforming resistance in the primary circuit to a higher voltage at lower current. To put numbers to the comparison of DBPP with CP-BRG, the specified transfer circuit in both cases has an input transfer-ratio range (with ranges ordered to correspond to the V_g range) of

$$V_g \in [20\text{ V}, 25\text{ V}, 30\text{ V}],\ V_s = 160\text{ V} \Rightarrow \frac{V_s}{V_g} \in [8.00, 6.40, 5.33]$$

Volksinverter V_s = 160 V. The worst-case value of V_s = 155 V includes voltage loss across windings and switches.

The current-waveform power-loss minimization of the primary and secondary windings, as expressed by the form factor of each, is optimum when they are equal, or

$$\kappa_p = \kappa_s \Rightarrow \sqrt{1+D'} = \frac{1}{\sqrt{D'}} \Rightarrow D'^2 + D' + 1 = 0$$

Solving the quadratic equation, and given that $0 \le D' \le 1$, the positive root is

$$D'_{opt} = \frac{\sqrt{5}-1}{2} \approx 0.618 \Rightarrow D_{opt} \approx 0.382$$

$D'_{opt} = 1/D'_{opt} - 1$ (where $1/D'_{opt}$ is incidentally the Golden Ratio ≈ 1.618). Then $\kappa_p = \kappa_s \approx 1.272$.

A performance parameter for PWM-switch efficiency is the *form-factor product* $\kappa_{QD} = \kappa_Q \cdot \kappa_D$. A minimum κ_{QD} maximizes active and passive switch efficiency in that both κ_Q and κ_D are minimized together. At D_{opt} for the BPP

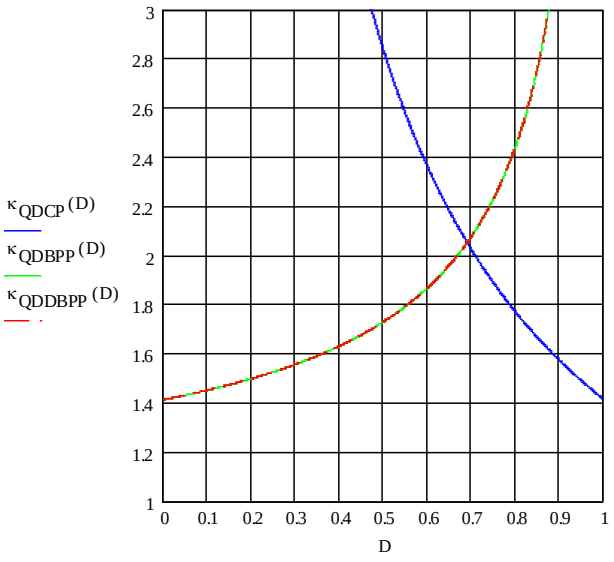
$$\kappa_{QD}(\text{BPP}) = \sqrt{1+D'} \cdot \frac{1}{\sqrt{D'}} = \sqrt{\frac{1+D'}{D'}} \Rightarrow \kappa_{QDopt}(\text{BPP}) = \sqrt{\frac{\sqrt{5}+1}{\sqrt{5}-1}} \approx 1.618,\ D_{opt} \approx 0.382$$

The form factor of the CP-BRG is

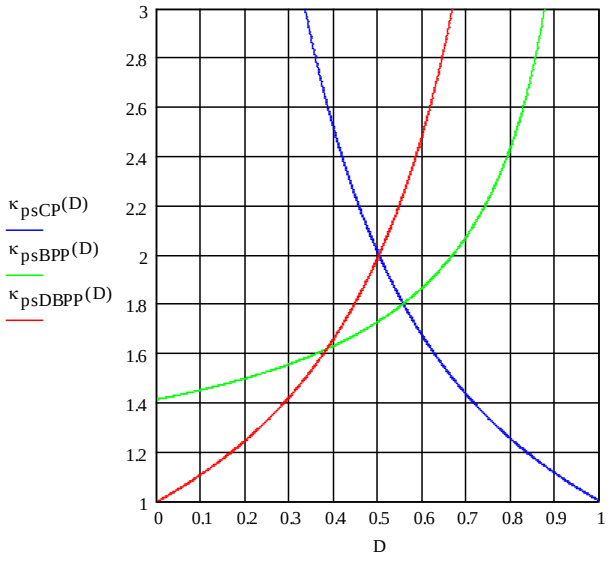
$$\kappa_{QD}(\text{CP}) = \frac{\sqrt{2}}{D} \Rightarrow \kappa_{QDopt}(\text{CP}) \approx 1.414,\ D_{opt} = 1$$

The BPP κ_{QD} is minimized when $D = 0$, but that is hardly a feasible operating-point for a circuit because it has no lower range; $D \geq 0$. The criterion for setting κ_Q and κ_D is to share equally the fractional loss between switches by setting $\kappa_Q = \kappa_D$. Regulated converters operate over a range of D, and as D decreases, κ_{QD}(CP) rises quickly, as shown in Fig. 4.

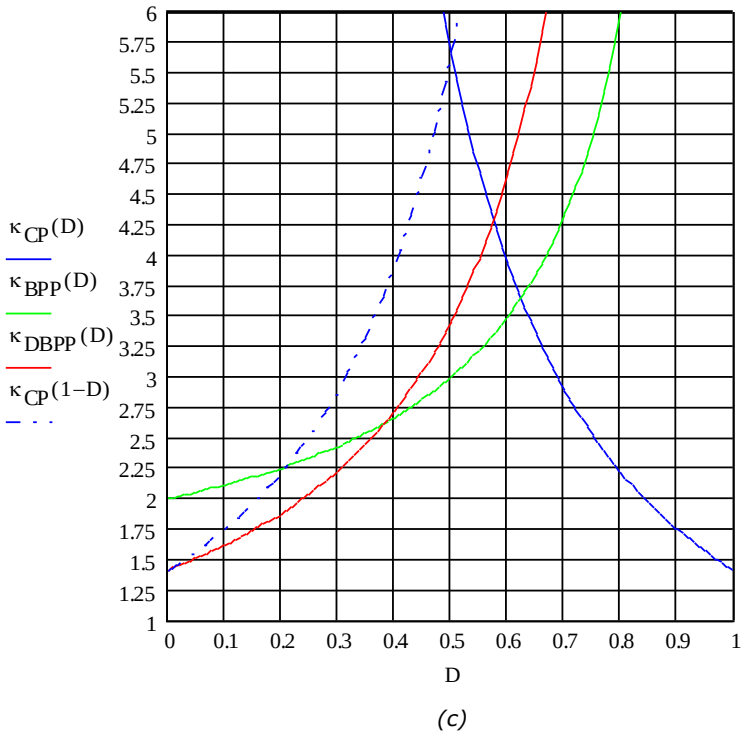
The optimal D minimizes switch form-factor product κ_{QD} of active and passive switches (by making them equal) and then achieves an overall minimum for switch form-factor and transformer form-factor κ_{ps} by equating $\kappa_{QD} = \kappa_{ps}$. Fig. 4 graphs these functions.



(a)



(b)



(c)

Fig. 4. Graphs of the form-factor products of CP-BRG, BPP, and DBPP switches (a) and windings (b), and their products (c). In parts (b) and (c), κ for DPBB and BPP cross at D_{opt}. $\kappa_{DBPP} < \kappa_{BPP}$ for $D < D_{opt}$ and $\kappa_{DBPP} > \kappa_{BPP}$ for $D > D_{opt}$. Around the D_{opt} operating-point, the rate of increase of $\kappa_{BPP} < \kappa_{DBPP}$. The complementary function of $\kappa_{CP}(D)$ is reflected around D = ½ as the dash-dot plot for a more direct comparison with the CA-PP plots. In (a), note that κ_{QDBPP} and κ_{QDDBPP} overlap and are the same plot.

Applying the above equations, the table shows the comparisons. The CP operating-point (design center) cannot be set to the optimal *D* because it is at the maximum of the *D* control range. The BPP and DBPP have an advantage in that their minimum κ_{QD} is at a value of D_{opt} (at 0.382) that is within and not at the end of their *D* range of [0, 1].

The CP-BRG has two-level current waveforms with κ minima at $D = 1$. Having both $\kappa_Q = \kappa_p$ and $\kappa_D = \kappa_s$ track is in itself advantageous, but with $D_{opt} = 1$ at one extreme of the *D* range, it cannot be approached too closely because the controller needs a range of *D* around the operating-point. Allowing for finite switching time at the extremes of *D*, a practical value might be $D_{max} \leq 0.95$.

If *n* is chosen for the DBPP at the center of its range it also sets $V_s' = n \cdot V_s$ which sets the voltage rating (with safety margin included) of the switches. Allowing D_{opt} to be placed at the center of the V_g range, then for the DBPP, $1/n = (6.4/2) \cdot (0.618) = 1.98 \rightarrow 2$ and $V_s' = 160$ V/2 = 80 V. By setting $1/n$ to an integer of $1/n = 2$, the switches can have a 100-V rating, and with $V_s' = 80$ V at 1-kW transfer power, $I_g/2 = 1$ kW/80 V = 12.5 A and $I_g = 25$ A. At the operating-point of D_{opt}', DBPP $\tilde{i}_Q \approx (1.272) \cdot (12.5\text{ A}) = 15.9$ A per each of the two switches.

Table. Performance comparison based on given parameters and their formulas.

CP-BRG	DBPP	Design formulas and notes
$V_s/V_g = (1/n)\cdot D$	$V_s/V_g = (2/n)\cdot(1/D')$	V_s/V_g = 160 V/$V_g \in$ [8.00, 6.40, 5.33]
Set D_{max} = 0.95	Set D_{opt}' = 0.618	Constrained by D_{max} ; D_{opt}'(min $\kappa_{QD}\cdot\kappa_{ps}$) = 0.618
$D \in$ [0.95, 0.760, 0.633]	$D' \in$ [0.500, 0.625, 0.75]	$D = V_s'/V_g$; $D' = 2/(V_s'/V_g)$
$1/n \geq 8.42 \rightarrow$ **8.5** V_s' = 19 V ≤ V_{gmin}	$1/n$ = 1.98 → **2** V_s' = 80 V ≥ V_{gmax}	$\frac{1}{n} \geq \frac{V_s/V_{g\min}}{D_{\min}}$; $\frac{1}{n} \leq \frac{2}{D'_{opt}\cdot(V_s/V_{gopt})}$, $V_{gopt} \approx V_{gmid}$ = 25 V
$\kappa_Q \in$ [1.451, 1.622, 1.777]	$\kappa_Q \in$ [1.225, 1.275, 1.323]	CP-BRG $\kappa_Q = \sqrt{\frac{2}{D}}$; DBPP $\kappa_Q = \sqrt{1+D'}$
κ_p, κ_D, $\kappa_s \in$ [1.026, 1.147, 1.257]	κ_p, κ_D, $\kappa_s \in$ [1.414, 1.265, 1.155]	$\kappa_p = \kappa_D(\text{FW}) = \kappa_s = \frac{1}{\sqrt{D}}$; $\kappa_p = \kappa_D(\text{FW}) = \kappa_s = \frac{1}{\sqrt{D'}}$
$\kappa_{QD} \in$ [1.489, 1.861, 2.233]	$\kappa_{QD} \in$ [1.732, 1.612, 1.528]	$\kappa_{QD} = \frac{\sqrt{2}}{D}$; $\kappa_{QD} = \sqrt{\frac{1+D'}{D'}}$
mid κ_{QD} = 1.861, D_{mid} = 0.76	mid κ_{QD} = 1.612, D'_{mid} = 0.625	1.861/1.612 = 1.154 ⇒ CP-BRG has 15.4% more loss, mid-scale
$\kappa_{ps} \in$ [1.053, 1.316, 1.579]	$\kappa_{ps} \in$ [2.00, 1.60, 1.33]	$\kappa_{ps} = \frac{1}{D}$; $\kappa_{ps} = \frac{1}{D'}$
$\frac{\overline{P}_{Ld}}{\overline{P}_g}$ = 0.367	$\frac{\overline{P}_{Ld}}{\overline{P}_g} = \frac{4}{4} = 1.000$	$\frac{\overline{P}_{Ld}}{\overline{P}_g} = 1 - \frac{V_s'}{V_{g\max}}$; $\frac{\overline{P}_{Ld}}{\overline{P}_g} = \frac{1}{4}\cdot\frac{V_s'}{V_{g\min}}$, both L
$\frac{\overline{P}_{pd}}{\overline{P}_g} = \sqrt{\frac{V_{g\max}}{V_{g\min}}}$ = 1.225		Transformer design power rating for CP-BRG and CA-PP

The CP-BRG minimum $1/n$ is determined by V_{gmin}; $1/n$ must be large enough so that $V_s > V_o$. The lowest $1/n$ minimizes the inductor design-power rating $\overline{P}_{Ld}$, but $1/n$ is limited by D_{max} = 0.95 and V_{gmin} = 20 V to $1/n \geq (8.00)/(0.95) = 8.42$. The nearest CP-BRG half-turn $1/n$ = 8.5. With these turns for each circuit, total switch loss (from κ_{QD}) of the CP-BRG at midrange is 15.4% greater than the DBPP, and at V_{gmax} it is a maximum at 2.233/1.528 ≈ 1.461 or is greater by 46.1%. Diode switch-loss and winding losses are comparable.

From the performance graphs of Fig. 4 the conclusion from the upper-right graph is that the transformers of CA-PP and CP-BRG, though operating with complementary duty-ratios (D for the CP-BRG, D' for the DBPP) have symmetrical winding-loss curves. The secondary circuit loss is the same for both.

For the CA-PP circuits, the DBPP primary current (unlike the BPP) is a two-level square-wave, the same waveshape as for the CP-BRG. The DBPP advantage over the CP-BRG is in switch loss, shown in the upper-left graph. Switch form-factor products κ_{QD} include both primary-circuit active MOSFET and secondary rectifier

passive diode switches. The curves show that the DBPP form-factor product remains lower than the CP-BRG value over a given Δ*D* range of *D*, which represents the operating range of the circuit.

Averaging κ_{QD} over the *D* range

$$r = D_{max}/D_{min} = 1.50$$

$$\text{CP-BRG } \bar{\kappa}_{QDCP} = \frac{1}{D_{max} - D_{min}} \cdot \int_{D_{min}}^{D_{max}} \frac{\sqrt{2}}{D} \cdot dD = \sqrt{2} \cdot \frac{\ln\left|D_{max}/D_{min}\right|}{D_{max} - D_{min}} = \frac{\sqrt{2}}{D_{min}} \cdot \frac{\ln r}{r-1} \approx \frac{1.147}{D_{min}}$$

For the DBPP, κ_{QD} is integrated over the range of *D* (from D_{min} to D_{max}) and averaged over that interval of *D*. To integrate $\kappa_{QD}(D')$ the variable of integration is changed from *D* to *D'* so that $dD' = d(1-D) = -dD \Rightarrow dD = -dD'$. The integration limits change from *D* to *D'* = 1 – *D*, or from D_{min} to 1 – D_{min} = D'_{max} and from D_{max} to 1 – D_{max} = D'_{min}. Then these limits are exchanged in the integration by the negative sign of –*dD'* to result in

$$\text{DBPP } \bar{\kappa}_{QDCA} = \frac{1}{D_{max} - D_{min}} \cdot \int_{D_{min}}^{D_{max}} \sqrt{\frac{1+D'}{D'}} \cdot dD = \frac{1}{D'_{max} - D'_{min}} \cdot \int_{D'_{min}}^{D'_{max}} \sqrt{\frac{1+D'}{D'}} \cdot dD'$$

where $D_{max} - D_{min} = (1 - D_{min}) - (1 - D_{max}) = D'_{max} - D'_{min}$.

Set $D' = \tan^2\theta$. Then $\tan\theta = \sqrt{D'}$, $\theta = \tan^{-1}\sqrt{D'}$, and $dD' = 2 \cdot \frac{\tan\theta}{\cos^2\theta} \cdot d\theta \Rightarrow d\theta = \frac{1}{2} \cdot \frac{\cos^2\theta}{\tan\theta} \cdot dD' \Rightarrow$

$$\int \sqrt{\frac{1+D'}{D'}} \cdot dD' = \int \sqrt{\frac{1+\tan^2\theta}{\tan^2\theta}} \cdot \left(2 \cdot \frac{\tan\theta}{\cos^2\theta} \cdot d\theta\right) = 2 \cdot \int \frac{d\theta}{\cos^3\theta} = 2 \cdot \left[\frac{1}{2} \cdot \frac{\tan\theta}{\cos\theta} + \frac{1}{2} \cdot \int \frac{d\theta}{\cos\theta}\right] = \frac{\tan\theta}{\cos\theta} - \ln\left|\frac{1}{\sin\theta} + \frac{1}{\tan\theta}\right|$$

$$\Rightarrow \frac{1}{\sin\theta} = \frac{\sqrt{1+\tan^2\theta}}{\tan\theta} = \frac{\sqrt{1+D'}}{\sqrt{D'}} = \sqrt{\frac{1+D'}{D'}} \;;\; \cos\theta = \frac{1}{\sqrt{1+\tan^2\theta}} = \frac{1}{\sqrt{1+D'}}$$

$$\frac{\tan\theta}{\cos\theta} - \ln\left|\frac{1}{\sin\theta} + \frac{1}{\tan\theta}\right| = \sqrt{D'\cdot(1+D')} - \ln\left|\sqrt{\frac{1+D'}{D'}} + \frac{1}{\sqrt{D'}}\right| \Rightarrow$$

$$\text{DBPP } \bar{\kappa}_{QDCA} = \frac{1}{D'_{max} - D'_{min}} \cdot \left[\sqrt{D'\cdot(1+D')} - \ln\left|\sqrt{\frac{1+D'}{D'}} + \frac{1}{\sqrt{D'}}\right|\right]\Bigg|_{D'_{max}}^{D'_{min}}$$

With expressions for $\bar{\kappa}_{QD}$ of both DBPP and CA-BRG circuits, substitute D and D' limits first for the CP-BRG;

$$\text{CP-BRG: } D \in [0.95, 0.63]$$

$$\text{CP-BRG } \bar{\kappa}_{QDCP} \approx \frac{1.147}{D_{min}} = \frac{1.147}{0.633} \approx 1.811$$

For the DBPP,

$$\text{DBPP: } D' \in [0.50, 0.75] \Rightarrow D \in [0.50, 0.25]$$

$$\frac{1}{D'_{max}-D'_{min}}=4\ ;\ \sqrt{D'\cdot(1+D')}\ =[0.866,\ 1.146]\ ;\ \sqrt{\frac{1+D'}{D'}}+\frac{1}{\sqrt{D'}}\ =[3.146,\ 2.682]$$

$$\text{DBPP}\ \ \bar{\kappa}_{QDCA}\approx(4)\cdot\left((1.146-0.866)+\ln\left|\frac{3.146}{2.682}\right|\right)=(4)\cdot[0.280+0.1596]=1.758$$

Comparing the DBPP and CP-BRG $\bar{\kappa}_{QD}$, the CP-BRG has higher switch loss by 1.811/1.758 = 1.030 or about 3%. The average over the full range for the DBPP is only slightly better than for the CP-BRG. It is more advantageous at the operating-point at mid-scale, an advantage having about 15% less loss. Because battery-input converters operate near the chosen mid-scale value much of the time, the benefit of CA-PP circuits is greater than the average κ indicates.

Average $\kappa(D)$ over the D range is found for more comprehensive loss minimization as the product of both switch and winding form-factor products:

$$\bar{\kappa}_{Cx}=\frac{1}{D_{max}-D_{min}}\cdot\int_{D_{min}}^{D_{max}}\kappa_{QD}(D)\cdot\kappa_{ps}(D)\cdot dD\ ,\ \kappa_{Cx}(D)=\kappa_{QD}(D)\cdot\kappa_{ps}(D)$$

Direct comparisons of κ_{CP} with κ_{BPP} and κ_{DBPP} are numerically computed and plotted on the graphs in Fig. 5. The dot-dash plot of the left graph of Fig. 5 replaces D by D' in κ of the CP-BRG for direct comparison to the CA-PP plots over D from 0 to ½.

Below $D \approx 0.618$ the CP-BRG has greater loss than the BPP, and less loss above $D \approx 0.618$. The DBPP increases with less slope than the CP-BRG over the entire range of D (or D') and thus has less loss than the CP-BRG. The DBPP has less loss than the CP-BRG and the BPP for $D < D_{opt} \approx 0.382$ where their plots cross over.

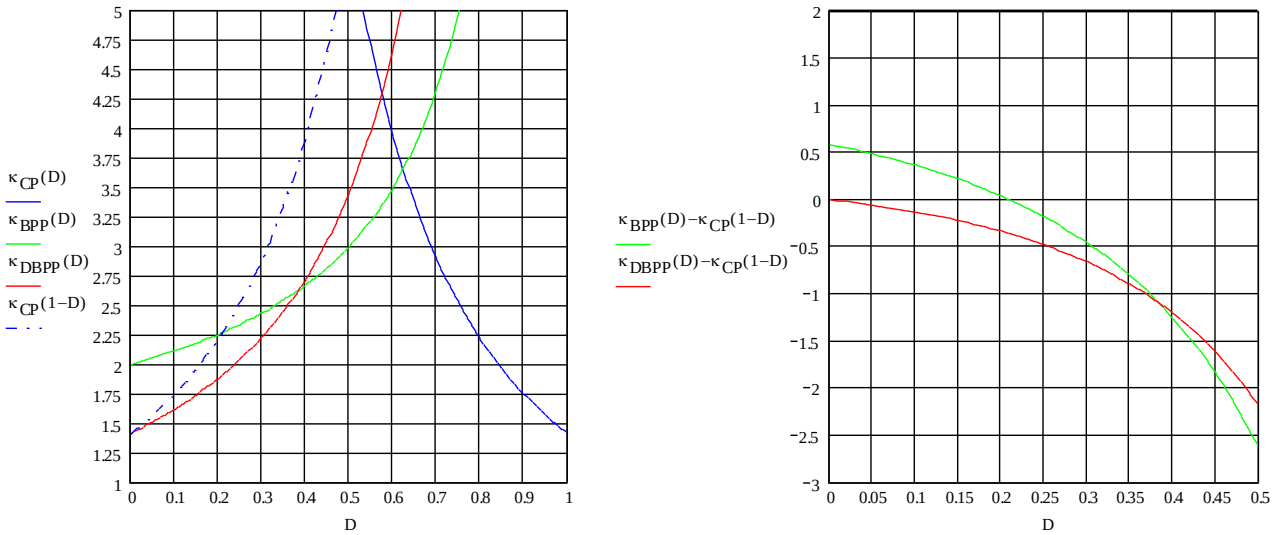


Fig. 5. CP-BRG, BPP, and DBPP plots of κ (left) and their comparison to $\kappa_{CP}(D')$ (right) where the lower the plot, the lower the CA-PP loss relative to the CP-BRG; below 0, BPP and DBPP have lower loss than the CP-BRG. The DBPP has less loss than the BPP below $D_{opt} \approx 0.382$, but above D_{opt}, the BPP advantage over the CP-BRG is higher than is the DBPP. For D < 0.2, the CP-BRG is better than the BPP.

Another consideration in comparing the CP-BRG and CA-PP circuits is the magnetic design of the components. One glaring disadvantage of the DBPP over both the BPP and CP-BRG is the inductor sizing. The design-power

rating for the combined inductors must equal the input power. The BPP for 1/*n* = 4 has $\overline{P}_{Ld} / \overline{P}_g$ = 0.5, or half the DBPP power requirement. At $\overline{P}_{Ld} / \overline{P}_g$ = 0.367, the CP-BRG is better than both CA-PP circuits and is its major advantage. Consequently, for switch and winding power loss, the CA-PP circuits are better though they require somewhat larger (BPP) to twice (DBPP) inductor design-power than the CP-BRG. Thus, the CP-BRG inductor is smaller and costs less but switch and transformer winding losses are greater.

Switch Voltage And On-Resistance

For the CA-PP circuits, the off-time voltage of V_s' applied to the inductor(s) must always exceed the maximum V_g. If $V_s' < V_g$, the off-time voltage across the inductor does not oppose its current but aids it, and the inductor current ratchets upward in *low-V_o fault* mode.

The Volksinverter V_g range is $V_g \in$ [20 V, 30 V] and fixed secondary voltage is set at a nominal V_s = 160 V. It is referred to the BPP primary winding through n = 1/4 as V_s' = (160 V)/4 = 40 V. Both BPP and DBPP switches must have twice this voltage when off, or $2 \cdot V_s'$ = 80 V. Switch off-voltage of the CP-BRG is $V_{DS} = V_g$. The CP-BRG has two series bridge switches and $2 \cdot r_{on}$ switch resistance. Both CA-PP have a single MOSFET switch with higher voltage and hence higher r_{on}. Which has less conduction loss?

The higher V_{DS} rating of CA-PP circuits raise MOSFET r_{on} by V_{DS}^e. The theoretical limit for MOSFETs is e = 2.5 but has been decreasing for decades as MOSFET construction is refined. A 1990s IR HEXFET III in an SMD220 package with a die capable of handling 150 W has r_{on} (50 V) = 24 mΩ (IRFZ46S) and r_{on} (100 V) = 77 mΩ (IRF540S). Solving for e,

$$\left(\frac{r_{on2}}{r_{on1}}\right) = \left(\frac{V_{DS2}}{V_{DS1}}\right)^e \Rightarrow e = \frac{\log(r_{on2}/r_{on1})}{\log(V_{DS2}/V_{DS1})} = \frac{\log(77\,\text{m}\Omega/24\,\text{m}\Omega)}{\log(100\,\text{V}/50\,\text{V})} = \frac{\log(3.208)}{\log 2} = 1.68$$

At present, e is less than this 1990s value and for DMOSFETs is approaching e = 1. In other words, MOSFETs are becoming increasingly better suited for higher V_g.

Secondary circuit winding, switch waveforms, and power loss are the same among CA-PP and CP-BRG because the secondary circuits are similar. The primary circuit is where they differ. To make a valid comparison of the r_{on} difference between same-area MOSFETs, the two CA-PP switches are given twice the area of the CP-BRG switches because the CP-BRG has twice the number of MOSFETs. The CA-PP switch higher-voltage tradeoff is that the circuit current of each MOSFET is reduced, as is switch conduction loss, by $\tilde{i}_{sw}^2$. The ratio of CA-PP to CP-BRG switch currents at D_{opt} of each is

$$\frac{\tilde{i}_{QCA}}{\tilde{i}_{QCP}} = \frac{\frac{I_g}{2} \cdot \sqrt{1+D'}}{I_g \cdot \sqrt{\frac{D}{2}}} = \frac{0.636}{0.707} \approx 0.90 \Rightarrow \left(\frac{\tilde{i}_{QCA}}{\tilde{i}_{QCP}}\right)^2 \approx 0.81$$

For equal switch loss, the 1 – 0.81 = 19% less conduction loss of the CA-PP switches allows them to have 1/0.81 = 1.236 times more r_{on}. The MOSFET voltage exponent at equal switch loss is calculated from loss ratio

$$\frac{\overline{P}_{QCA}}{\overline{P}_{QCP}} = \frac{\tilde{i}_{QCA}^{\,2} \cdot r_{onCA}}{\tilde{i}_{QCP}^{\,2} \cdot r_{onCP}} = \frac{\tilde{i}_{QCA}^{\,2}}{\tilde{i}_{QCP}^{\,2}} \cdot \frac{r_{onCA}}{r_{onCP}} = (0.81) \cdot \frac{1}{2} \cdot \left(\frac{V_{DSCA}}{V_{DSCP}}\right)^e = (0.81) \cdot \frac{1}{2} \cdot \left(\frac{80\,\text{V}}{40\,\text{V}}\right)^e = (0.81) \cdot (\tfrac{1}{2} \cdot 2^e) = 1 \Rightarrow e = 1.30$$

Thus e must exceed 1.3 for the CP-BRG to have a switch-loss advantage over the CA-PP at their optimal operating-points. A more comprehensive comparison considers this ratio over the operating range.

Which Topology Is Best?

The conclusion drawn from these comparative analyses is that the BPP has only a slight advantage as the Volksinverter converter power-transfer circuit. With switch trends to lower *e*, it has lower switch conduction loss than the CP-BRG and lower inductor design-power than the DBPP. The tradeoff in CA-PP and CP-BRG switch ratings is higher voltage at lower current. The CA-PP also have fewer switch-driver parts and lower on-board currents.

Comparing DBPP and BPP, the two inductors of the DBPP are of equal size ($\overline{P}_{Ld} / \overline{P}_g$ = 0.5) to the single inductor of the BPP. However, the BPP has lower primary winding utilization in that at D_{opt}, each winding conducts more than half the magnetic switching period (two switching cycles) or U_p = (1 + 0.382)/2 = 0.691 whereas the DBPP and CP-BRG primary winding utilization is U_p = 1, which is about 31% higher.

The transformer power-loss ratio for the DBPP and CP-BRG are equal at 1.225 whereas for the BPP, $\overline{P}_{pd} / \overline{P}_g$ = 1.5, resulting in a 22.4% larger transformer. Overall, the CP-BRG magnetics are smallest in size, followed by the BPP, then the DBPP. The CA-PP primary circuits are also protected from overcurrent by their inductors and can be designed to be inherently more reliable.

In weighing magnetics and switch design alternatives, none of the three power-transfer circuits for the Volksinverter design stand out as clearly the best overall. Yet a decision must be made. Weighing the importance of reduced current in the primary circuit, switch reliability, and parts count, the decision is made for the BPP.

The simplicity of a single BPP inductor versus the DBPP outweighs the somewhat larger transformer. Moreover, as a practical consideration, BPP magnetics prototypes have already been designed and wound at Innovatia and will be tested in the first Volksinverter prototypes. R&D sometimes takes a tortuous, suboptimal path. Happily for anyone who has already built the BPP circuit, not much prototype circuit-board reconfiguration is required to transition between the BPP and DBPP transfer-circuit topologies and the DBPP can be tried without much additional circuit-board mutilation.

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About The Author

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For further reading on inverter design, see the How2Power Design Guide, locate the Power Supply Function category and select "DC-AC power inverters."