GaN HEMT Package Improves Paralleling Of Devices In Space Power Applications

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As more processing power and more complex loads are placed on-orbit or into deep space missions, it is necessary in some situations to parallel two or more power switches to increase power handling or to preserve or improve conversion efficiency in power conversion circuitry. However, conventional power device packages, such as the FSMD-A/B/C/D and their I/O pad provisioning make it difficult to accomplish paralleling of these devices in a performance-conscious manner.

The reason for this difficulty is that when paralleled, the gate and source-sense pads on these packages either serve to block the most efficient/shortest interconnect from package-to-package for the drain and source connections if the gate-to-source-sense drive loop is optimized. Or they do the same for the gate and source-sense pads if the drain-to-source high-current loop is optimized. With these packages it is always a compromise in parallel configurations between optimized drain-source load-circuit performance and gate-source-sense drive-loop performance.

Some new thinking is required in order to enhance the application performance of hermetic power packaging in space designs where paralleled devices are required.

Enter the FSMD-G package. This new packaging option rethinks the way that the I/O pads on the discrete HEMT packages are provisioned, and places them with relation to one-another in a manner that electromechanically partitions the high-frequency, voltage-sensitive gate-source-sense drive loop from the high-frequency, high-current gate-source loop. This mechanical partitioning places the source pad (the potential reference node for the HEMT device) between the drain and the gate and source-sense pads.

This clever rearrangement of the package I/O pads now allows the designer more degrees of freedom when connecting multiple HEMT packages in parallel. The result is that the gate-drive loop may be optimized by reducing the induction loop area to its minimum value, thus reducing the loop inductance to as small a value as possible. And along with this optimization of the gate-drive loop, the drain-source loop may also be optimized as the drain-to-drain and source-to-source connections from paralleled packages may be made as short, and thus as least resistive, as physically possible.

Conventional Packaging Limitations For Paralleling Devices

The best way to observe the paralleling problems and issues with legacy, conventional hermetic HEMT packaging is with an example. Consider a conventional HEMT package, the FSMD-B, as shown in Fig. 1.

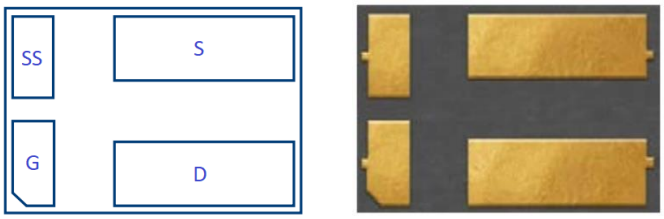


Fig. 1. EPC FSMD-B power HEMT packaging (bottom/pad view).

The FSMD-B package's pad arrangement is excellent for standalone applications of a particular device. However, when paralleling of HEMTs is desired or required, the positions of the four pad terminals make it difficult to efficiently parallel devices. That's because the drain and source terminals of the paralleled devices must be connected together, but the gate and source-sense pads interfere with a clean, effective PCB layout, as demonstrated in the example in Fig. 2.

In Fig. 2 the gate and source-sense pads on HEMT Q2 are "landlocked" by common copper etch areas of the drains and sources of HEMTs Q1 and Q2. This necessitates connecting the gate of Q2 to the gate of Q1 with vias

and an etch trace on an inner layer (running beneath the drain and source of Q1). The addition of the vias in each connection between the two metal layers creates additional parasitic inductance to the gate of Q2. This parasitic inductance is beyond that of the induction loop area from the gate-driver output to the gate and source-sense of Q2.

The same situation exists for the source-sense connections. Also notice how the D1-to-D2 connection must go "up and over" the G2 pad in order to accomplish the connection. This diversion of etch around the G2 pad adds resistance between the D1 and D2 pads, and thus adds etch resistance that would not be present if the G2 pad was not directly adjacent to the D1 and D2 pads. This same situation exists for the S1 and S2 pads due to the adjacency of the SS2 pad.

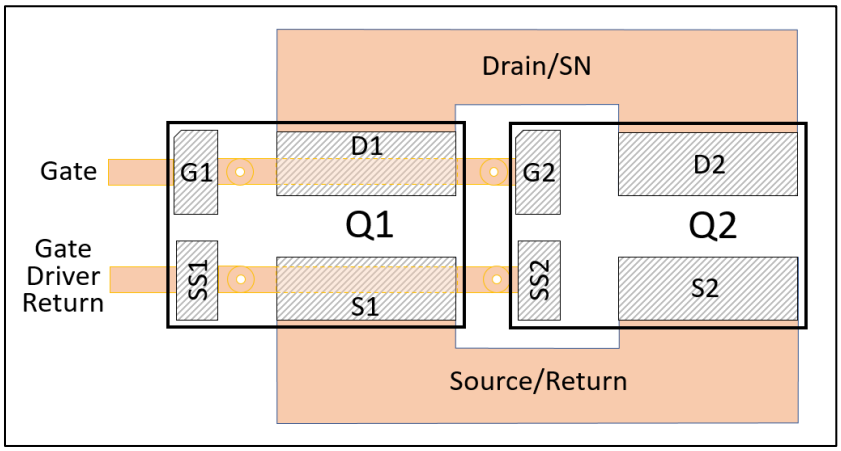


Fig. 2. Example PCB layout of two FSMD-B packages in parallel (top X-ray/lid view).

The net outcome is that in order to accommodate the legacy packaging in a PCB layout, performance compromises must be made in order to parallel these packages.

A New Package

The FSMD-G package designed by EPC Space helps to eliminate the PCB implementation roadblocks, such as shown in Fig. 2, that are encountered when using the other HEMT packaged devices in the EPC Space discrete product portfolio. This new, easily paralleled package is shown in Fig. 3.

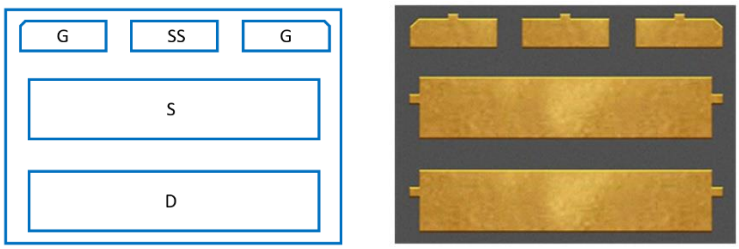


Fig. 3. EPC FSMD-G power HEMT packaging (bottom/pad view).

An examination of Fig. 3 shows that there are two key differences between the "G" package and any other package in the EPC Space discrete product lineup. The first is that the drain and source pads are parallel to one another the entire length of the package, and the second is that there are two gate connections on the package.

Implementing the drain and source in this way allows the paralleled drain and source connections to be uninterrupted from package to package, creating the optimum parallel device situation. And the two gates on each package, internally-connected within the G package's base, allow the gates in a parallel implementation to be daisy-chain connected from package-to-package on the top PCB etch layer.

A typical parallel arrangement of the FSMD-G package is shown in Fig. 4, and it illustrates how clean and tidy the layout becomes (in comparison with the FSMD-B example) because of the improved I/O pad layout of the FSMD-G package. All the required connections are as short as possible and they all reside on the top etch layer of the PCB—no vias required!

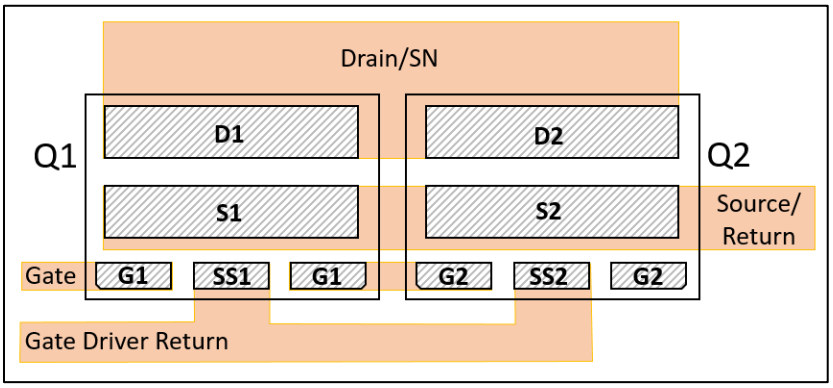
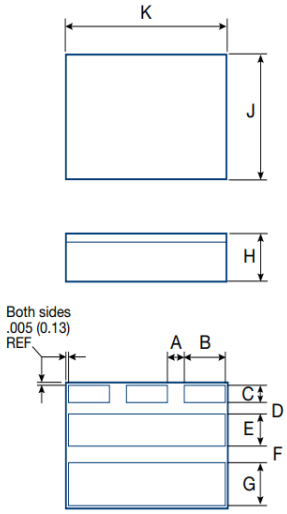


Fig. 4. Example PCB layout of two FSMD-G packages in parallel (top X-ray/lid view).

Discussion And Summary

Some other noteworthy features of the FSMD-G package are the fact that it has been purposely designed to be slightly larger than other packages in the EPC Space discrete product portfolio. This is so this package can accommodate the large die in the new EPC7000 series.

The physical dimensions for the FSMD-G package are shown in Fig. 5.



Symbol	Inches		Millimeters		Note
	MIN	MAX	MIN	MAX	
A (2x)	0.028	0.038	0.711	0.965	
B (3x)	0.075	0.085	1.905	2.159	
C (3x)	0.025	0.035	0.635	0.889	
D	0.015	0.025	0.381	0.635	
E	0.051	0.061	1.295	1.549	
F	0.024	0.034	0.61	0.864	
G	0.07	0.08	1.778	2.032	
H	0.078	0.088	1.981	2.235	
J	0.215	0.225	5.461	5.715	
K	0.311	0.321	7.899	8.153	

Standard Terminal Pad finish is a solder alloy of 63%Pb 37%Sn

Fig. 5. Physical/mechanical dimensions of the EPC Space FSMD-G package.

These new devices in the EPC7000 series have lower $R_{DS(ON)}$, better dynamic on-resistance performance and improved thermal performance than their predecessors. And as with the other discrete devices offered by EPC Space, they are rock-solid rad-hard. This makes the devices housed in the FSMD-G package ideal for paralleling in demanding high-current applications in space such as low-side synchronous rectification in a conventional POL converter or as the synchronous switches in the isolated secondary of a synchronously rectified forward converter. The designer can be assured that they are obtaining the best possible electrical performance from the paralleled devices because of the unique, improved pad arrangement on the FSMD-G package.

Now, to achieve the optimized paralleling, a compromise had to be made with regard to the PCB layout of two of the FSMD-G packages connected in a half-bridge configuration. When two FSMD-G packages are utilized in a half-bridge, their low-side drain (D1) to high-side source (S2) connection (which forms the switching node) appears as follows in Fig. 6.

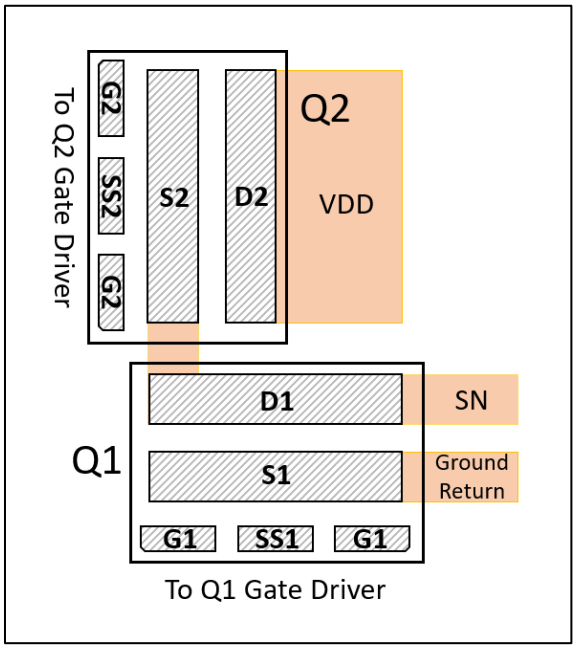


Fig. 6. Example PCB layout of two FSMD-G packaged HEMTs in a half-bridge configuration.

It's clear that the arrangement of the drain and source terminals on the packages creates a choke point between the required etch connection from D1 to S2. This connection is necessarily small to comply with the spacing requirements of D2-to-S2 and D1-to-D2. The switching node (SN) connection is of higher resistance, thus creating higher ohmic losses, than packaging alternatives. Such an alternative is shown in Fig. 7 for a legacy FSMD-B or FSMD-D style package.

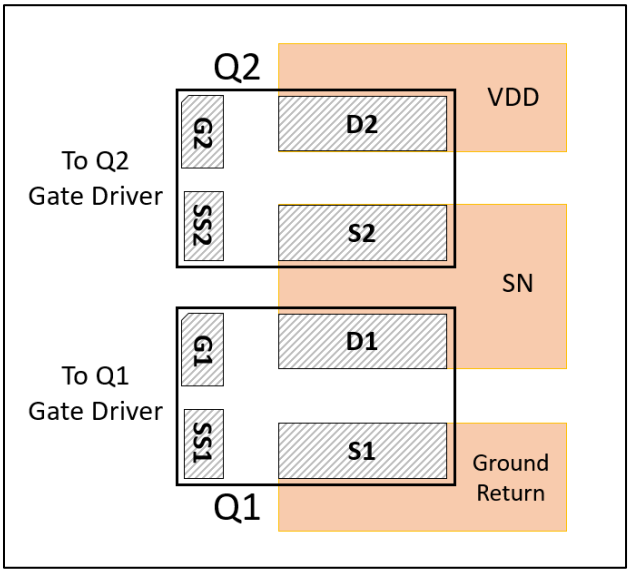


Fig. 7. Example PCB layout of two FSMD-B or FSMD-D packaged HEMTs in a half-bridge configuration.

The packaging shown in Fig. 7 allows for a wide etch trace to connect D1-to-S2, a situation that allows for a much smaller interconnection (etch) resistance between D1 and S2.

There is a solution to achieving the optimum interconnect resistance between D1 and S2 as well as allowing superior paralleling of devices with Q1. This is possible using the packaging shown in Fig. 8.

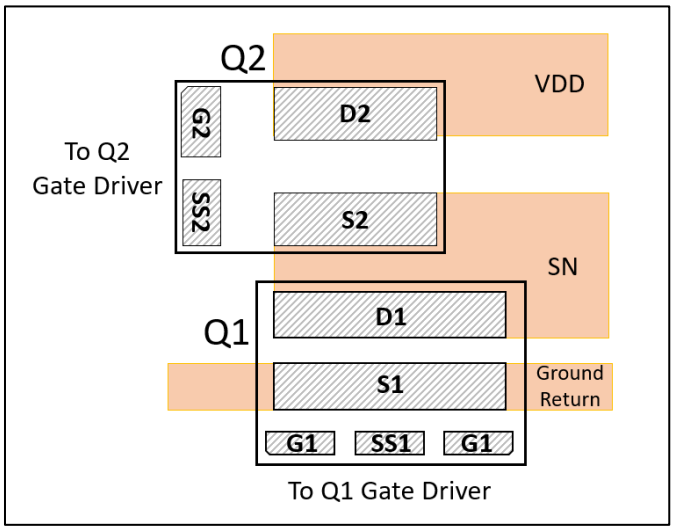


Fig. 8. Example PCB layout of an FSMD-B/D (Q2) and FSMD-G (Q1) packaged HEMTs in a half-bridge configuration.

The packaging implementation in Fig. 8 shows that by utilizing packages with different pad configurations designers can obtain the required optimized switching-node connection resistance while allowing for optimized paralleling of the low-side transistor (Q1) if necessary or desired. Each package type can serve a useful purpose to achieve optimum performance, so the packaging compromise for the FSMD-G package does not result in a performance (efficiency) dead end.

Reference

EPC Space website.

About The Author

Tony Marini is the president of dtm Associates, an engineering consultancy in Massachusetts and works with EPC Space in a consulting role. Tony has over 40 years of experience in the areas of electronics, semiconductors and microelectronics. He also has expertise in the areas of power electronics, system reliability prediction and failure modes, and EMC/EMI design and problem remediation.

Tony has published numerous technical papers and has been a presenter at technical conferences and symposia. He earned his BSEE and MSEE from Worcester Polytechnic Institute (Worcester, Mass.), with a concentration in semiconductor physics and power electronics.

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