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Tradeoffs In Raising The Maximum Duty Ratio In Forward And Flyback Converters

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In single-cycle isolated power converters, such as forward and flyback, the allowable duty ratio does not usually exceed 50%. This conventional boundary combined with a stiff voltage clamping technique[1,2] usually allows limiting the primary switch voltage magnitudes at the supply voltage level (V_{IN}) for dual-ended- and at double supply voltage level (2 x V_{IN}) for single-ended converter topologies. This voltage clamping technique significantly increases converter efficiency by recovering the energy stored in the transformer leakage inductance, returning it back to the primary source.

Expanding the operational duty ratio beyond the 50% mark and providing a balance of the volt-second areas of the positive and negative portions of the transformer windings' voltage waveforms would require the primary switches to operate at higher voltage levels. Recent developments in high-voltage-rated MOSFET technologies such as SiC MOSFETs and high-voltage GaN transistors have created new opportunities for single-cycle converter designs in such modes. If usage of the stiff voltage clamping feature can be extended to higher voltage levels, it might be of interest to examine the benefits of extending the operational duty ratio beyond the 50% point.

This article studies the impact of such an operating mode on power loss in the converter's active components in the most widely used forward and flyback single-ended topologies. It provides a framework for making tradeoffs between achieving higher efficiency at lower cost and using more-expensive switching transistors (whether wide-bandgap or silicon devices) with a lower on-resistance.

We begin by examining the primary- and secondary-side component power losses under the conditions that can provide efficiency improvements over baseline cases representing operation at duty ratios not exceeding 50%. We then analyze what tradeoffs need to be considered to achieve such improvements. Examples of stiff clamp techniques for single-ended and dual-ended single-cycle power converters operating at duty ratios above 50% are then provided.

Pros And Cons Of Increasing The Maximum Duty Ratio

Let's examine the impact of operating duty ratios on some major dc-dc converter parameters, such as the output inductor value in a forward converter, transformer magnetizing inductance in a flyback converter, switch RMS and peak currents, and power losses.

A standard rule of thumb for designing the output inductor in forward topologies (or a transformer in flyback topologies) is to set the magnetic component ripple current ΔI at a certain percentage of the rated output current I_O. The equation for output inductance L_{OUT} of a forward converter operating at switching frequency f_{sw}:

$$L_{OUT} = \frac{V_O(1-D)}{(\Delta I/I_O)\cdot f_{SW}}$$

yields that when duty ratio D gets increased from D_1 to D_2 the required inductance value drops by: $(1-D_1)/(1-D_2)$ times.

For example, if D_1 = 0.5 and D_2 = 0.667 the required inductance drops by a factor of 1.5; if D_2 = 0.75, the required inductance value would be twice lower than in the baseline case. That is, a significantly smaller magnetic component is needed for the same output ripple current. This phenomenon is illustrated in Fig. 1a for a duty ratio range of 0.5 to 0.9. A similar result would be reached in the case of the flyback transformer magnetizing inductance.

The dc-dc converter parameters, such as primary transformer winding and switching transistor currents, as well as synchronous rectifier (SR) voltage magnitude, directly depend on the power transformer turns ratio. For

example, for a conventional forward converter, the transformer turns ratio *n*, primary switch RMS current I_{1RMS} and current magnitude (neglecting ripple) I_{1max} can be determined by the following equations:

$$n = \frac{w_1}{w_2} = \frac{V_{IN.min} D_{max}}{V_O} \quad (1)$$

$$I_{1max} = \frac{I_O}{n} \quad (2)$$

$$I_{1RMS} = \frac{I_O \sqrt{D_{max}}}{n} \quad (3)$$

The voltage across the freewheeling SR $V_{FW.max}$ also depends on the turns ratio:

$$V_{FW.max} = \frac{V_{IN.max}}{n}$$

where w_1 and w_2 are numbers of turns in the primary and secondary transformer windings, respectively, and $V_{IN.min}$ and $V_{IN.max}$ are minimum and maximum input supply voltages.

As follows from equations (1) through (3), increasing the operating duty ratio allows designers to increase the turns ratio *n* which in turn results in significant reduction in the peak and RMS values of the primary switch current. Graphs illustrating these reductions are also shown on the chart in Fig. 1a.

The last equation also shows that raising the duty ratio can also lead to reduction in the magnitude of the output sync rectifier voltage. However, there are also drawbacks to duty ratio expansion.

For example, in single-cycle topologies, causing a power transformer to reset properly, i.e., providing a balance of volt-second areas in the primary winding voltage waveform at shorter off-time intervals, requires an increase in the switch-voltage magnitude. Assuming a square-wave waveform shape produced in stiff voltage clamping topologies at a minimum supply voltage level, the maximum voltage across the switch derived from the volt-second area balance across the primary transformer winding can be defined as follows:

$$V_{1m} = \frac{V_{IN}}{1 - D_{max}} \quad (4)$$

Expression (4) demonstrates that the use of a larger duty ratio leads to an increase in the peak switch voltage which may reach extreme levels when D_{max} approaches one and require usage of switches with higher voltage ratings. Such switches will typically have higher on-resistance[3] and the higher conduction loss associated with it. Graphs illustrating the increase in peak voltage magnitude for single-ended and dual-ended converter topologies providing stiff voltage clamping are shown in Fig. 1b.

As follows from the graphs in Fig. 1b, the benefits of the required inductance value reduction along with reductions of peak and RMS switch currents (Fig. 1a) could be negated by the increase in the switch-voltage magnitude, which leads to the selection of switches with larger on-resistance. Also, the higher the switch-voltage magnitude, the greater the parts count required in the stiff clamping circuit,[1] which can be a significant factor in tradeoff decisions.

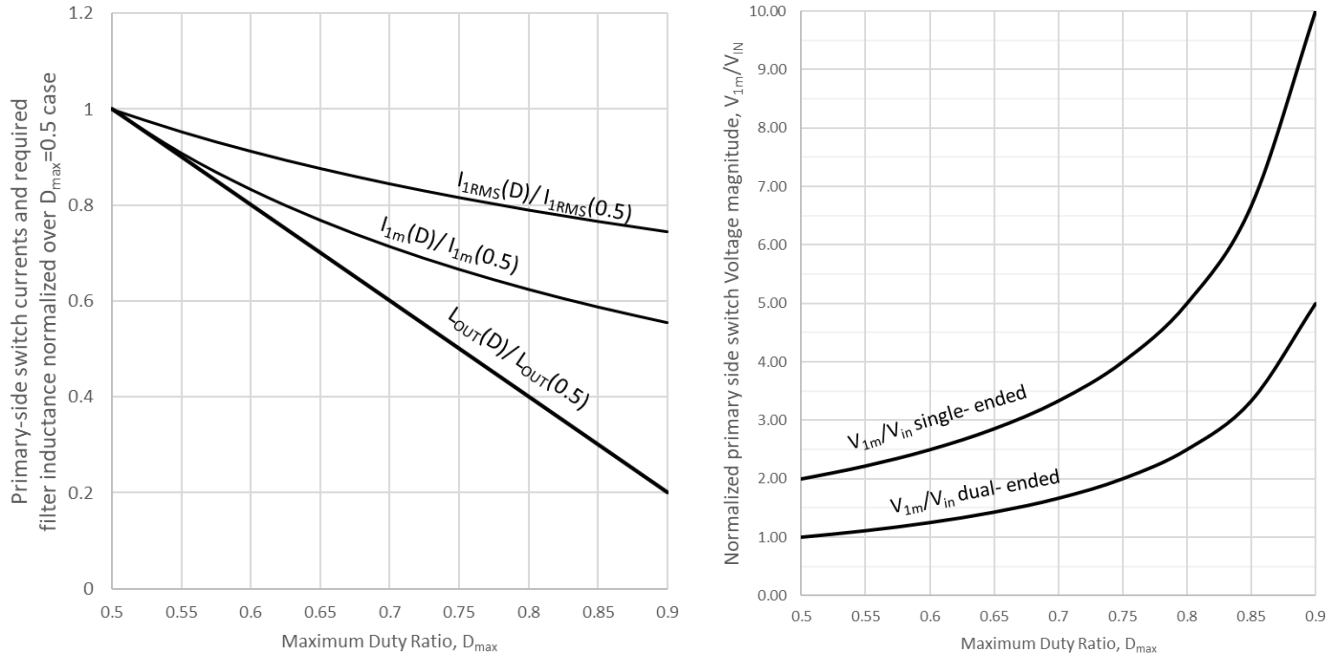

Fig. 1. Operational duty cycle expansion impacts on single-cycle converters. Increasing the operational duty ratio opens an opportunity for reduction of the filter inductance- and primary switch peak- and RMS currents (a). However, at higher duty ratios the primary-side switch-voltage magnitude increases at a growing rate, and at D_{max} approaching one can reach extreme levels (b).

The aforementioned pros and cons associated with duty ratio increase make it relevant to quantify the benefits, i.e., to determine power losses in active converter components as functions of duty ratio and converter topologies realizing higher duty ratio operation. Then, comparing losses at a baseline duty ratio (D_{max} = 0.5) and in a higher duty ratio case will allow us to determine the tradeoffs of expanding the duty ratio range and making a decision on adopting necessary converter topology mods.

Impact Of Duty Ratio On Power Losses

Power losses directly impact the efficiency and thermal design of the dc-dc converter which makes them a key parameter in comparing different operating modes. Let's determine power losses in converter active components as functions of the duty ratio.

Switch voltage and current magnitudes are the two variables that define switching losses. According to equations (2) and (4) they change in opposite directions with increasing duty ratio. This means that conduction loss variations will be the dominating factor in power dissipation change and with sufficient accuracy for practice, we can focus on the conduction loss component which can be accurately computed based on known active component current and voltage waveshapes.

Power losses in the primary-side and secondary-side (synchronous rectifier) switches of the single-ended flyback converter can be determined by their on-resistances and the RMS values of the rectangular current waveforms:

$$P_{LOSS1} = I_{1.RMS}^2 \cdot R_{DSON1} = \frac{P_O^2 R_{DSON1}}{D_{\max} V_{IN.min}^2} \qquad (5)$$

$$P_{LOSS2} = I_{2.RMS}^2 \cdot R_{DSON2} = \frac{I_O^2 R_{DSON2}}{1-D_{\max}} \quad (6)$$

where R_{DSON1} and R_{DSON2} are on-resistances on the primary and secondary switches, respectively.

The equation for the power loss in the primary-side switch of the single-ended forward converter is identical to equation (5). Secondary-side conduction losses in the forward converter are split between two SR switches conducting during different portions of a switching cycle. Similar to the flyback converter case, the equations for the power loss in the output SR switches of a forward converter can be determined based on their RMS currents:

$$P_{LOSS2.R} = I_{R.RMS}^2 \cdot R_{DSON.R} = I_O^2 D_{\max} R_{DSON.R} \quad (7)$$

$$P_{LOSS2.FW} = I_{FW.RMS}^2 \cdot R_{DSON.FW} = I_O^2 (1 - D_{\max}) R_{DSON.FW} \quad (8)$$

where $R_{DSON.R}$ and $R_{DSON.FW}$ are on-resistances of the MOSFETs representing rectifying and freewheeling SRs, respectively.

Peak voltage across the primary switch in both forward and flyback topologies having stiff voltage clamping is defined by equation (4) at $V_{IN} = V_{IN.max}$. Peak voltages across the secondary switches in the forward converter are defined by the following equations:

$$V_{FWD.R.max} = \frac{aV_O}{(1-D_{max})} \quad (9)$$

$$V_{FWD.FW.max} = \frac{aV_O}{D_{max}} \quad (10)$$

where *a* represents an input voltage swing factor equal to a ratio of maximum and minimum primary supply voltage levels: $a = \frac{V_{INmax}}{V_{INmin}}$. Peak voltage across the secondary switch of a flyback converter is defined by the equation:

$$V_{FLBK.max} = V_O \left[a \left(\frac{1}{D_{max}} - 1 \right) + 1 \right] \quad (11)$$

Assuming that voltage magnitudes within a given transistor technology directly affect its on-resistance, and by using equations (5) through (11), we can compare power losses in different maximum duty ratio operating modes.

Comparing Power Losses

For a detailed comparison of power losses at different duty ratios let's establish baseline cases—conventional single-ended forward and flyback converters operating at $D_{max} = 0.5$. We will assume that for cost-optimized designs, change (increase or decrease) in voltage magnitude across a power MOSFET and rated breakdown voltage of a selected part is accompanied by a corresponding change in its on-resistance.

This on-resistance of a MOSFET is proportional to the blocking voltage raised to the 2.6 power[3] and its variation is caused by the need to change a thickness of a layer of higher resistivity epitaxial material used to sustain the rated voltage level. The on-resistance increase will be reflected in the ratio of losses in the expanded duty case to the baseline case. These data are shown in Table 1 for the forward converter case and in Table 2 for the flyback converter case.

As follows from equations (9) through (11), a relative change in voltage magnitudes across output sync rectifiers in a forward converter does not depend on the input voltage swing factor. In the flyback converter,

this change has some dependency on *a*, which is why for this converter we will be assuming a 20% voltage swing, and using *a* = 1.2 which is typical for many practical cases.

Table 1. Conduction power losses and voltage magnitudes of active components in a forward dc-dc converter at different duty ratios.

Component	Parameter	Baseline (D_{max} = 0.5)	Expanded (D_{max} = 0.667)	Expanded/Baseline
Primary-side switching MOSFET	P_{LOSS1}	$\frac{2P_O^2R_{DSON1}}{V_{IN.min}^2}$	$\frac{1.5P_O^2R_{DSON1E}}{V_{IN.min}^2}$	$0.75 \cdot 1.5^{2.6} = 2.15$
	V_{1m}	$2V_{IN.max}$	$3V_{IN.max}$	1.5
Sync rectifier SR1, P_{LOSS1}	P_{LOSS2R}	$0.5I_O^2R_{DSON.R}$	$0.67I_O^2R_{DSON.RE}$	$1.33 \cdot 1.5^{2.6} = 3.8$
	$V_{FWD.R.max}$	$2aV_O$	$3aV_O$	1.5
Sync rectifier (freewheeling) SR2	$P_{LOSS2F.W.}$	$0.5I_O^2R_{DSON.FW}$	$0.33I_O^2R_{DSON.FWE}$	$0.67 \cdot 0.75^{2.6} = 0.32$
	$V_{FWD.FW.max}$	$2aV_O$	$1.5aV_O$	0.75

Table 2. Conduction power losses and voltage magnitudes of active components in a flyback dc-dc converter at different duty ratios.

Component	Parameter	Baseline (D_{max} = 0.5)	Expanded (D_{max} = 0.667)	Expanded/Baseline
Primary-side switching MOSFET	P_{LOSS1}	$\frac{2P_O^2R_{DSON1}}{V_{IN.min}^2}$	$\frac{1.5P_O^2R_{DSON1E}}{V_{IN.min}^2}$	$0.75 \cdot 1.5^{2.6} = 2.15$
	V_{1m}	$2V_{IN.max}$	$3V_{IN.max}$	1.5
Sync rectifier SR1, P_{LOSS1}	P_{LOSS2R}	$2I_O^2R_{DSON.R}$	$3I_O^2R_{DSON.RE}$	$1.5 \cdot 0.727^{2.6} = 0.654$
	$V_{FLBK.R.max}$	$V_O(a+1)$	$V_O(a/2+1)$	0.727 (a=1.2)

Tradeoffs

For a fair comparison of different operating modes, the same criteria needs to be applied. In our case, we will be considering the usage of the same MOSFET technology on the primary and secondary sides and a theoretical cost-optimized design for which the MOSFET maximum rated voltage exactly matches the projected level.

As follows from Table 1, despite a 3x power loss reduction in the freewheeling sync rectifier MOSFET, a 3.8x increase in losses in the sync rectifier SR1 makes it unreasonable to use the expanded duty operation mode in forward converter designs utilizing identical MOSFET technologies in the primary and secondary switches. The reason for this statement is that the efficiency gain in this case comes at a high cost, requiring use of several transistors in parallel for the SR1 implementation.

Exceptions may include size-optimized cases in which, for example, the SR power loss increase doesn't affect SR heatsink size while the reduction in output inductor value provides space savings, or where the SR in the baseline design already has more than 50% margin in its maximum voltage rating. It can also be used in

efficiency-focused applications in which employing more-expensive power switches (either SiC MOSFETs, GaN HEMTs or multiple Si MOSFETs in parallel) on the secondary side is not an obstacle.

For the flyback converter case, represented in Table 2, there is an opportunity for almost a 30% loss reduction in the sync rectifier. As follows from Table 2, this reduction can outbalance the primary-side MOSFET power loss increase if the baseline secondary-side component losses are greater than the primary by a factor of (see Table 2): 2.15/0.654= 3.29.

Let's determine the application area for which this statement is valid. The ratio of secondary-to-primary side component losses for the baseline case (D_{max} = 0.5) can be determined by using equations (5) and (6), and assuming that for a given MOSFET technology, the on-resistance ratio R_{DSONR}/R_{DSON1} is proportional to the peak voltage ratio raised to the 2.6 power:

$$\frac{P_{LOSS2R}}{P_{LOSS1}} = n^{-0.6}\left(0.5+\frac{1}{2a}\right)^{2.6}$$

Assuming the ratio equals 3.29 at the baseline condition (D_{max} = 0.5) and *a* = 1.2, from this equation we can find that the increased operational duty ratio (D = 0.667) in a flyback converter can provide efficiency improvements in stepup cost-optimized applications having a turns ratio: n < 0.094.

The conducted analysis demonstrates the possibility of getting benefits from operation at an increased duty ratio. Within a given MOSFET technology and cost-optimized designs these benefits can be realized in stepup flyback converters with transformer turns ratios belonging to the just mentioned range.

It is important to note that if converter component selection (or cost optimization) is based not on this theoretical case, for which the maximum rated component voltage exactly matches the projected level, but on some other (practical) criteria, such as part interchangeability, providing enhanced component stress margins, maximum efficiency, etc., power saving benefits can be achieved also in forward and flyback stepdown topologies.

For example, if in the baseline case, the primary switch or sync rectifier is selected to withstand 50% higher voltage than projected, expanding the operating duty ratio in the forward converter will result in just power savings with no penalties in terms of other design criteria such as size or cost. Using specific advanced power component technologies on the primary and secondary side can also significantly extend the valid usage of higher duty ratio operation. For such cases the decision on the duty ratio expansion will be made based on the dominating design criteria: minimal power dissipation, component cost, weight, size, etc.

Practical Topologies

Theoretically, a stiff voltage clamping circuit can be configured for any maximum duty ratio. For example, to provide such clamping in a single-ended converter at level N x V_{IN}, primary and recuperating windings need to be divided into (N-1) sections and have their identical taps connected with "flying" caps. Examples of such circuit implementations for clamping levels exceeding $2V_{IN}$ for single-ended converters and V_{IN} for dual-ended converters will be given below.

As follows from the graphs in Fig. 1, the D_{max} increase above the 50%-point, despite the required reduction in filter inductor value at a fixed rate, provides a diminishing return in terms of other benefits. While switch current reduction becomes smaller at a decreasing rate as duty ratio increases, voltage magnitude V_{1m} across the primary-side switch rises at an increasing rate, and, as it was mentioned above, at D_{max} approaching one can reach extreme levels. Such high voltage levels will make the operation of single-cycle converters at duty ratios coming close to one impractical.

Also, as noted above, increasing the stiff voltage clamping level is associated with an increased number of winding taps in the power transformer, and an increase in the primary-side parts count (clamping diodes and caps). In addition to that, increasing the maximum duty ratio, for example, to 0.75 and having peak voltage

limits at 4 x V_{IN} for a single-ended configuration and 2 x V_{IN} for a dual-ended one will have some shortcomings. These shortcomings are essentially limitations in comparison with interleaved configs, which have an additional transformer, but double the duty at the filter input and clamp the peak voltages at lower levels: 2 x V_{IN} and 1 x V_{IN} for single-ended and dual-ended topologies.

Based on these considerations, practical topologies with extended duty ratio, capable of providing power loss reduction with reasonable impact on complexity would be those whose clamping voltage levels don't exceed 3 x V_{IN} for a single-ended configuration and 1.5 x V_{IN} for a dual-ended configuration while having a maximum duty ratio of 2/3 (0.67).

These topologies are given in Fig. 3a and Fig. 4a, respectively. Their equivalent schematics in the switch-on and voltage clamping states are shown in Fig. 3b and c, and Fig. 4b and c, respectively.

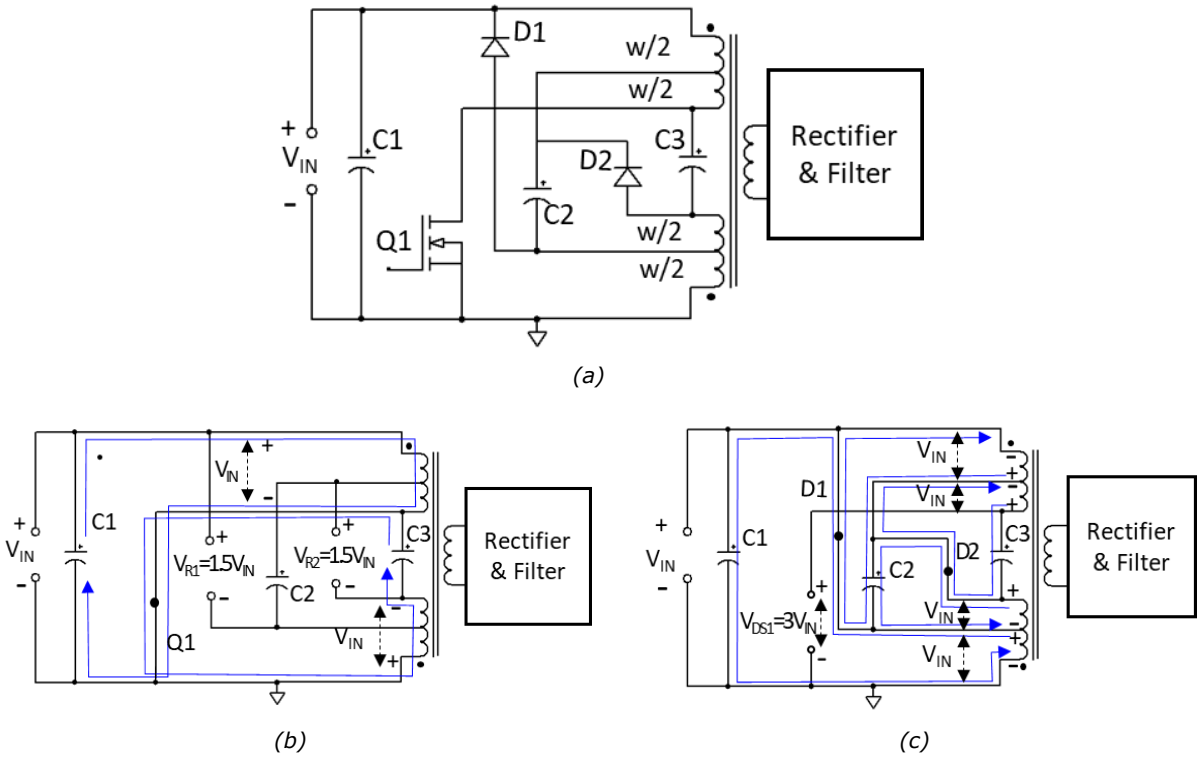

Fig. 3. Single-ended converter with 3 x V_{IN} clamping voltage level (a) and its equivalent schematics in the switch-on (b) and switch-off/voltage clamping (c) states.

Since there is no dc voltage drop across transformer windings, flying caps C2 and C3 in Fig. 3a represent floating dc sources with a voltage level equal to V_{IN}. When Q1 is on, clamping diodes D1 and D2 are reverse biased and are shown in Fig. 3b as open terminals. Voltages applied to them during this time interval are formed by voltage sources represented by C2, and C3, both charged to the V_{IN} level, and voltages generated across the halves of the primary winding (V_{IN}/2). This makes diode reverse voltages V_{R1} and V_{R2} equal to 1.5V_{IN}.

During this time interval, a voltage source formed by C3 is coupled to the grounded (recuperating) winding (Fig. 3b) and provides power to the load alongside the primary source V_{IN} coupled to the primary winding. When switching transistor Q1 turns off, voltages across transformer windings change polarities which makes the voltage across the switch rise above V_{IN}. Once the voltage across Q1 reaches 3 x V_{IN}, D1 and D2 start

conducting (Fig. 3c), clamping Q1 peak voltage at this level and recovering energy stored in the transformer leakage inductance back to the primary source. Primary-side current paths and directions during Q1 on and off time intervals are shown with blue lines in Fig. 3b and 3c, respectively.

In a dual-ended converter with a 1.5 x V_{IN} clamping voltage level (Fig. 4a), flying caps are charged from the primary source in series to $V_{IN}/2$ levels. When Q1 and Q2 are on, clamping diodes D1 and D2 are reverse biased, and voltages applied to them during this time interval are formed by sources represented by C2, and C3, and input supply voltage V_{IN}. These voltages are equal to $1.5V_{IN}$.

During this time interval, voltage sources represented by caps C2 and C3 are coupled to the two halves of recuperating winding (far-left and far-right locations in Fig. 4a and 4b) via conducting switches Q1 and Q2. These sources provide power to the load alongside the primary source V_{IN} coupled to the primary winding during this time interval.

When switching transistors turn off, voltages across transformer windings change polarities. Once the voltage across each of the two switches reaches 1.5 x V_{IN}, D1 and D2 start conducting, stiffly clamping the switches' peak voltages at this level and recovering energy stored in the transformer leakage inductance back to the primary source. Primary-side current paths and directions during Q1/Q2 on and clamping time intervals are shown with blue lines in Fig. 4b and 4c, respectively.

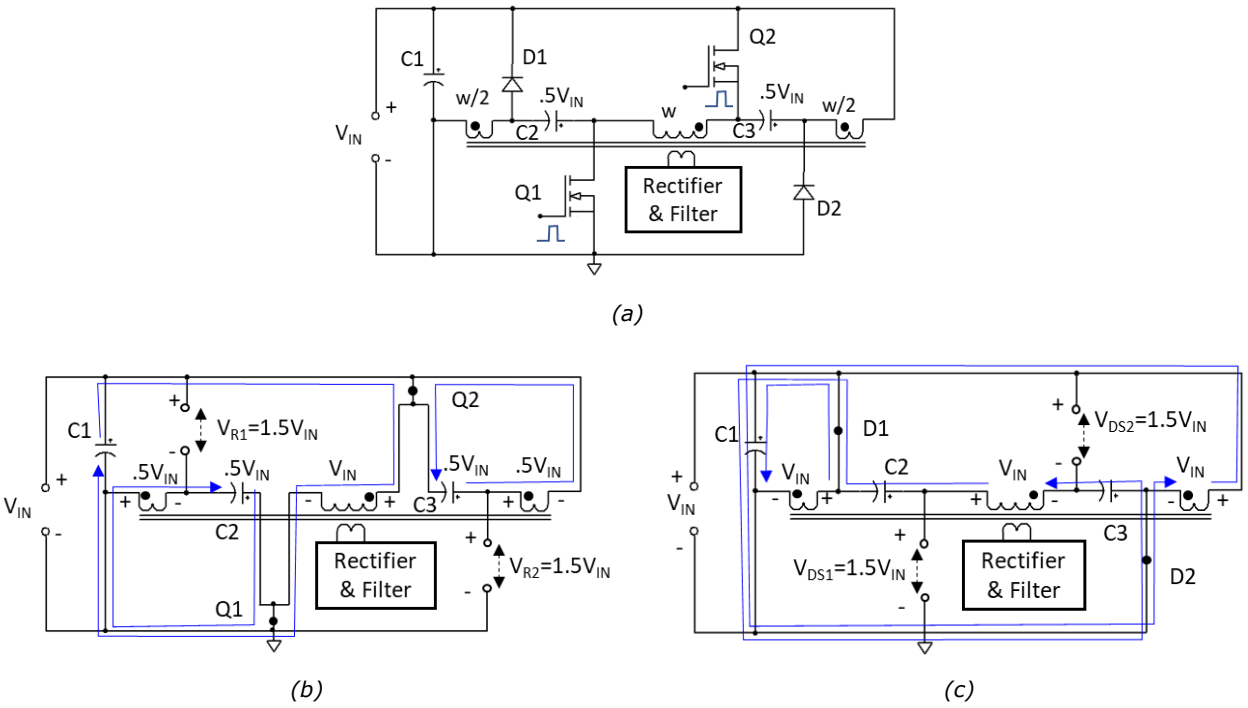

Fig. 4. Dual-ended converter with 1.5 x V_{IN} clamping voltage level (a) and its equivalent schematics in the switch-on (b) and switch-off/voltage clamping (c) states.

Primary switch voltage waveforms for forward and flyback converters in a voltage regulator application at maximum and minimum duty ratios are given in Fig. 5a and Fig. 5b, respectively. In plotting these waveforms, it was assumed that in the most commonly used voltage regulator application, D_{max} is achieved at min supplied voltage. These waveforms are given for single-ended topologies. For a dual-ended case all voltage levels shown in these diagrams should be scaled down by a factor of two.

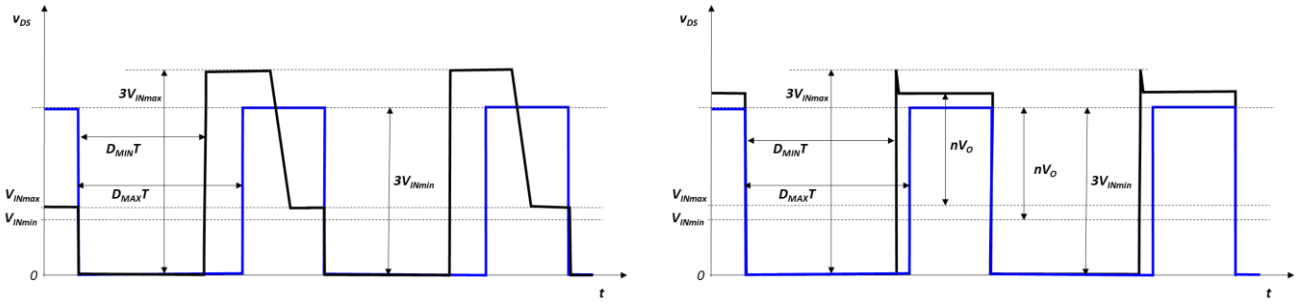

Fig. 5. Primary switch voltage waveforms for a forward (a) and flyback (b) single-ended converter in a voltage regulator application.

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About The Author

Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

For more on the design of forward and flyback converters, see How2Power's Design Guide, locate the "Topology" category and select "Forward" and "Flyback".