

Commentary

ISSUE: October 2023

Designing High-Performance, Robust Power Supplies For 5G And Outdoor Edge Computing

by Alessandro Pevere, Francesco Di Domenico and Alex Rossi, Infineon Technologies, Villach, Austria, and David Meneses, Infineon Technologies, Espoo, Finland

Designing an efficient and robust power supply unit (PSU) requires a deep understanding of application requirements and the environment in which the power supply will need to operate. One of the most challenging applications for which engineers must design a PSU is the 5G and edge computing ecosystem (Fig. 1).

As with most applications, the PSU must be efficient and compact. However, for 5G and edge computing, it must also be suitable for mounting close to telecom equipment on a pole or wall and operate robustly in a diverse range of harsh outdoor environmental conditions.

This article will explore key trends in 5G and edge computing applications and the design challenges these trends introduce. It will then introduce an architecture for a compact and efficient ac-dc power supply for 5G and edge computing in outdoor applications. Finally, the article presents an implementation example illustrating how engineers can successfully address each of the design challenges using the proposed architecture.



Fig. 1. The 5G and edge computing ecosystem must be able to operate efficiently and robustly in a diverse range of harsh outdoor environmental conditions.

Trends And Design Challenges

There are a number of trends that have a substantial impact on switch mode power supply (SMPS) design and power semiconductor selection for PSUs within the 5G and edge computing ecosystem.

The first is the expected proliferation of 5G small cells, edge computing, and private 5G networks over the coming years. According to Rethink RAN Research,^[1] new use cases will bring about rapid growth in private mobile networks, increasing the number of private 5G cells from less than 2000 in 2020 to 1.56 million by 2027. In terms of data, global traffic generated by these private 5G cells is expected to rise from 51,115 EB (exabytes) monthly in 2020 to 77.46 million EB monthly by 2027.

With this increase in traffic, these cells will be expected to deliver more functionality in a smaller form factor. Furthermore, there is already a trend toward fewer new cabinet installations. Instead, equipment is being mounted on towers, poles, or walls. As a result, there is less space and weight to allocate to the PSU.

Another significant trend impacting design is the higher level of integration in these systems. The PSU must be closer to the radio unit (RU) and perhaps even be integrated with it. Finally, the visual appeal of the PSU + RU takes on more importance since equipment is out in the open and no longer hidden in a cabinet.

Such integration has helped made it possible for edge computing to be deployed through highly scalable and compact "micro datacenters" with extremely variable sizes. These micro datacenters range from the "shoebox-like" deployments requiring ≤ 1 -kW power to containerized solutions requiring up to 500 kW. Frequently, the edge system includes an IP65 enclosure similar to the latest generation of 5G outdoor small cell base stations, which can be assembled either at the telecom RAN tower, on buildings, or on lighting infrastructure.



The success of edge computing, then, depends on the availability of systems able to provide the necessary processing speed and power while operating reliably in the less-regulated—and more unpredictable— environments encountered outside the conventional datacenter. The edge computing hardware must then include compact, energy-efficient architectures that can be widely deployed, even in space-constrained and harsh environments, to locate computing as close as possible to sensors and other data sources.

All the above-mentioned factors introduce a number of challenging requirements to PSU design. In short, a PSU designed for outdoor edge servers has to fulfill most of the usual requirements of a telecom rectifier (for example, for outdoor small cells). Thus, to be successful, PSUs must have

- High power density
- Thin form factor, from 22 to 27 mm and down to 18.5 mm in cases where the PSU is integrated with the radio
- Fanless and convection cooling
- Wide input voltage
- High output power
- Reduced EMI to meet stringent requirements
- The ability to operate in harsh outdoor conditions (rain, snow, dry heat) and extreme temperatures (freezing cold, direct sunlight).

A Compact And Efficient AC-DC Power Supply Architecture

To meet the many requirements of a PSU for 5G and edge computing outdoor applications, a design fully based on surface mount devices (SMDs) is needed. Top-side cooling is preferred, utilizing a metal baseplate and chassis cooling. Because of the high-input- and high-output-power requirements, massive surge protection is needed as well. The design will also need to make use of planar magnetics and 3D assembly techniques to meet compact form factor requirements.

Table 1 shows the specifications for a 5G edge computing outdoor PSU. As can be seen, the PSU must have a wide-voltage input range and high-power output, high efficiency, and high power density. It must also have a wide operating temperature range with low EMI and massive surge protection.

Ac input voltage	85-305 Vac
Dc output	12 V and 1000 W
Power factor	>0.98 at full power
THD	<5% at full power
Efficiency	>96% at high line (peak)
	>95% at low line (peak)
Cooling	Natural, fanless
Power density (without heatsink)	50 W/in. ³
Dimensions	27 x 80 x 150 mm
Operating temperature range	-40°C to 85°C
Surge	Common mode: 4 kV
	Differential mode: 4 kV
EMI	Class A
Control	Digital (XMC)

Table 1. The specifications for an edge-computing outdoor power supply unit.

The architecture of the example PSU employs an interleaved, continuous conduction mode (CCM) totem-pole power factor correction (PFC) circuit combined with a half-bridge LLC dc-dc resonant converter (Fig. 2).





Fig. 2. The PSU architecture employs an interleaved continuous conduction mode (CCM) totempole PFC circuit combined with a half-bridge LLC dc-dc resonant converter.

Using CCM totem-pole PFC offers several advantages. First, it enables the final design to achieve a power factor of >0.98 at full power. This reduces reactive power, lowering operating costs and improving overall system efficiency. Meanwhile, an interleaved topology distributes current across multiple power devices while reducing input current ripple. In addition to reducing EMI, this reduces stress on individual components, enabling the use of smaller and more cost-effective components. Interleaving also spreads heat dissipation, allowing for the use of smaller heat sinks or other heat-spreading technologies.

The use of an interleaved CCM totem-pole PFC topology gives engineers greater flexibility in design since the topology can be easily scaled to match different power requirements. Interleaving is also inherently redundant, since if one stage fails, the others can continue to operate, improving robustness and reliability.

Using a half-bridge LLC dc-dc resonant converter provides multiple benefits as well. Soft switching at 0 V or 0 A minimizes switching losses and lowers EMI for better efficiency and reduced power dissipation. This converter also enables the use of lighter and smaller magnetic components, leading to a compact footprint with higher power density.

Another benefit is the ability of a half-bridge LLC dc-dc resonant converter to operate across a wide input voltage range, which results in a more flexible PSU design. And with excellent transient responsiveness, it enables the power supply to maintain a stable output voltage during sudden load variations.

The interleaved CCM totem-pole PFC (see Fig. 3) has two variants where Q1 through Q4 are implemented using silicon carbide (CoolSiC^[2]) with 72-m Ω typical R_{DS(ON)} or gallium nitride (CoolGaN^[3]) with 70-m Ω maximum R_{DS(ON)}. SD1 and SD2 are power MOSFETs (CoolMOS S7^[4]) at 600 V and 22 m Ω . The circuit supports 400-Vdc output.



Fig. 3. The interleaved CCM totem-pole PFC.



The half-bridge LLC dc-dc resonant converter is implemented using a planar transformer to maintain a low profile and high power density with excellent thermal characteristics (Fig. 4). The secondary side of the transformer has center-tapped windings and the sync rectifier utilizes a 40-V/0.7-m Ω power MOSFET (OptiMOS 6^[5]) that supports double-sided cooling.



Fig. 4. The half-bridge LLC dc-dc resonant converter.

The final implementation is shown in Fig. 5. The PFC and LLC efficiency achieved is shown in Fig. 6. As can be seen, PFC efficiency is nearly 99% at 230 Vac and just under 98% at 115 Vac. LLC efficiency reaches over 97%. Overall PSU efficiency is shown in Fig. 7, reaching over 96% at 230 Vac and over 95% at 115 Vac.



Fig. 5. The complete implementation of the PSU.





 $1ph \rightarrow$ only one active phase; $2ph \rightarrow$ two active phases in interleaved mode



Fig. 6. PFC efficiency (top graphs) and LLC efficiency (bottom graph).



Thermal performance and EMI are excellent as well, as shown in Figs. 8 and 9.







Fig. 8. PFC thermal performance.



Designing power supplies for 5G and outdoor edge computing requires an efficient and compact design that can withstand harsh environmental conditions and integrate with radio units without introducing interference. By utilizing an interleaved continuous-conduction-mode totem-pole PFC circuit combined with a half-bridge LLC dc-dc resonant converter, engineers can meet exacting application requirements while providing superior efficiency, thermal performance, and reduced EMI (Table 2). This fanless design also maintains design flexibility to support a wide range of input and output voltages while providing full digital control in both the PFC and LLC stages.

PFC key requirements	Value
Input voltage	100 to 250 Vac. (nom.)
	85 to 305 Vac (max)
Output voltage	12 V
Output current	83 A
Output power	1000 W
Efficiency	>96% peak (efficiency curve TBD)
Height	1U or 0.5U (TBD)
Cooling	Natural convection
Ambient temperature	-40°C to 70°C
Infineon components	600-V CoolSiC, 600-V CoolMOS S7,
	40-V OptiMOS all in SMD packages
	with top-side cooling

Table 2. Final details of PSU architecture.



References

- 1. "<u>1.56 million private 5G cells deployed by 2027</u>" by Annie Turner, Mobile Europe, March 30, 2021.
- 2. "<u>CoolSiC Products</u>," Infineon website.
- 3. "<u>CoolGaN Integrated Power Stage (IPS)</u>," Infineon website.
- 4. "500V-950V CoolMOS N-Channel Power MOSFET," Infineon website.
- 5. "<u>N-Channel Power MOSFET</u>," Infineon website.
- 6. "<u>Building Better Power Supplies For 5G Base Stations</u>" by Alessandro Pevere and Francesco Di Domenico, How2Power Today, June 2022.

About The Author



Alessandro Pevere is a system application engineer in the high voltage demo board team at Infineon Technologies Austria. Previously, he served as head of system eng. at Meta System in Italy, following almost two years as a post-doctoral researcher at KU Leuven/Energyille in Belgium.

Alessandro received B.Sc. and M.Sc. degrees in electronic engineering from the University of Udine, Italy and a Ph.D. in power electronics from the same university. During his Ph.D. studies he also served as a research assistant at the University of Michigan working on wireless power transfer.



Francesco Di Domenico is a senior principal application engineer at Infineon Technologies Austria. He's a system architect for telecom power and specialist in SMPSs for server/datacenter, telecom and general industrial applications. Francesco's main competencies include the application of power semiconductors, both based on Si SJ and modern wide-bandgap materials, in power conversion topologies.

His expertise covers telecom system architectures, but also the design of power converters, magnetic components, control concepts, with special focus on resonant/soft switching topologies. Before joining Infineon Technologies Austria, he held technical leading positions in the professional SMPS industry in Italy.



David Meneses currently works as an application engineer in ac-dc and dc-dc topologies for server and telecom applications. He joined Infineon Technologies in 2014. David received the M.Sc. degree in electrical engineering and the Ph.D. degree in power electronics, both from the Universidad Politecnica de Madrid, Madrid, Spain.