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CMOS Buffers Support Cold Sparing For Space ICs Without The Usual Power Penalty

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Electronic circuits can experience operational failures from a variety of factors, especially when operating in harsh environments like space applications. Such failures can stem from various sources, including radiation effects, exposure to extreme temperatures, electro-static discharge (ESD), aging, or any other causative factor.

In systems required to function in inaccessible environments, such as satellites, it is necessary to provide mechanisms for allowing the system to continue to operate while experiencing either permanent or temporary failures in portions of its circuitry. For this reason, satellites are designed with duplicate systems or components for critical functions. These can include communication equipment, power systems (like batteries and solar panels), onboard computers, sensors, and control mechanisms.

In such systems where redundant components are utilized, the back-up systems are kept in a powered-off state or "cold spared" when not in use. When a problem is detected in a primary component, the satellite can automatically switch to the corresponding cold spare. Alternatively, ground control can manually command the switch after evaluating the situation.

Cold-spare components are electrically isolated from the primary system in operation via separate power supplies. The power supply isolation protects the cold-spared component from being damaged by the same incident that caused the failure of the primary component (like a power surge induced by radiation). While the power supplies are isolated, the inputs and outputs of the corresponding primary and cold spared blocks are tied together as show in Fig. 1.

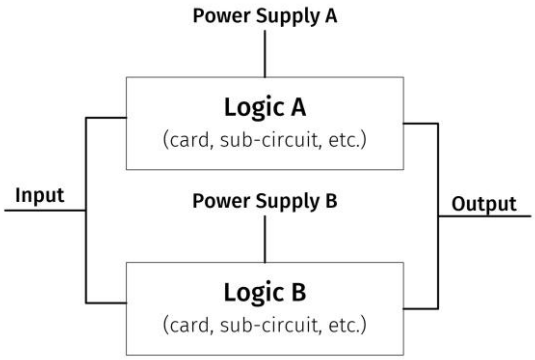

Fig. 1. Cold spare system block diagram. In cold-spared systems, the backup circuits that provide redundancy are kept in a powered-off state (hence the term "cold spare") until needed. Use of separate power supplies permits the systems to be electrically isolated.

The presence of ESD clamping diodes in standard CMOS input and output buffers creates difficulties in cold-sparing of logic circuits. The diodes create unwanted paths of current conduction via the cold-sparing power supply, wasting power when the cold-sparing circuitry is not in use, and also uncertainty as to what the state of the cold-spared power supply will be when it's turned on. Various fault conditions can ensue.

To address these problems, system designers may add isolation circuitry but that also increases system complexity and may impact reliability. The extra components may also affect size, weight and power. With these challenges in mind, Apogee Semiconductor has developed proprietary I/O structures that enable cold-sparing without the power penalty associated with use of COTS-based CMOS ICs, while also avoiding the

drawbacks of isolation circuitry.

In this article, we explain the source of parasitic power consumption and potential fault conditions in cold-sparing circuits, the limitations of existing solutions, and I/O structures that overcome these problems. These CMOS input and output circuit structures are offered in the digital and mixed-signal rad-hard ICs offered by Apogee, and in the company's semi-custom Rad-flex logic chips.

The Difficulty Of Cold Sparing

For digital applications, all integrated circuits (ICs) have electrical input and output pins that utilize buffers to process the incoming and outgoing signals. The circuit structures of a commonly utilized input and output buffer are shown in Fig. 2.

For the input buffer of Fig. 2a, one can identify a conduction path from the input pin (IN) to the power supply (VCC) via either of the anodes of D1 or D3 to their cathodes. These diodes are necessary structures required to protect input transistors M1 and M2 from human body model (HBM) and charge distributed model (CDM) ESD stress.

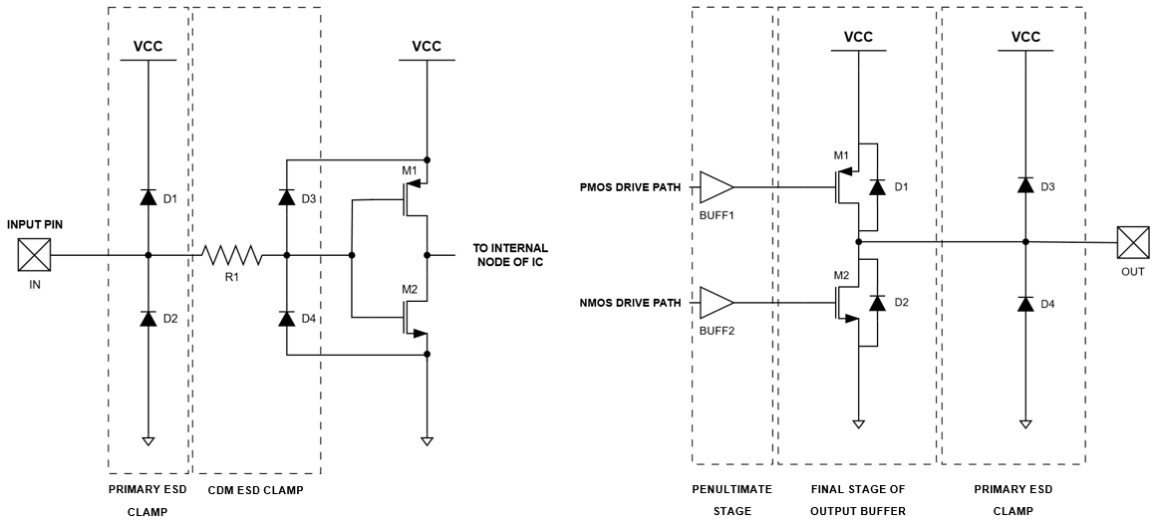

Fig. 2. Standard CMOS input (a) and standard CMOS output (b) in logic ICs. In both the input and output circuits, diodes D1 and D3 represent parasitic bias paths that allow conduction from either the input or output to VCC. These paths are problematic because they can conduct current into the cold-spared power supply.

Similarly, in the case of the output buffer of Fig. 2b, it can be seen by inspection that there is a conduction path from the output pin (OUT) to the power supply (VCC) by way of the anode of the primary ESD clamp diode (D3) to the cathode. In addition, there is also a conduction path from the output pin (OUT) to the power supply (VCC) by way of the parasitic back-gate diode labeled (D1).

This last diode is introduced because of the parasitic back-gate diode of the PMOS labeled M1 that forms from the p-type doped source to the NWELL of M1 that is connected to the supply (VCC). For the remainder of this discussion, all these paths will be collectively referred to as parasitic bias paths.

When parallel inputs and outputs are connected in cold-spared systems as illustrated by the block diagram of Fig. 1, the parasitic bias paths can conduct current into the cold-spared power supply. Fig. 3 illustrates how this situation can develop.

Consider the case when the active output in Fig. 3 labeled OD2 is set to a logic high level that is defined by the level supplied from the active supply VCCA. If the power supply labeled VCCB is a backup to supply VCCA in a cold-spared system when OD2 is driving high, current can conduct through the parasitic bias paths in the cold-spared output OD1 and input buffer IB1 of Fig. 3, collectively referred to as cold-spared I/Os. This is an undesirable power state and depending on how the power system is architected determines how severely the system will be impacted.

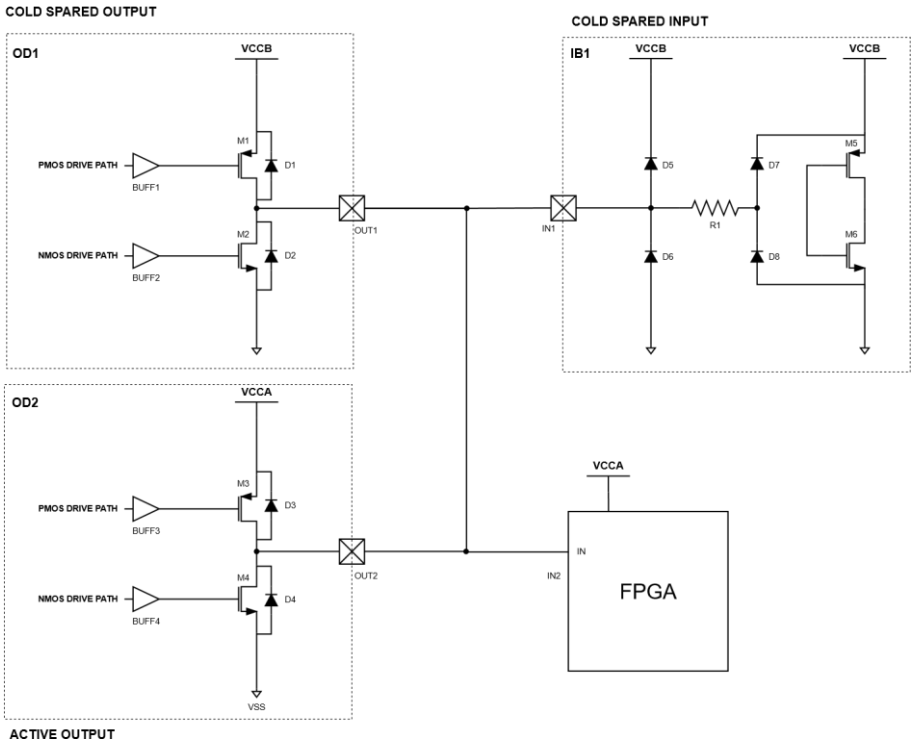

Fig. 3. A cold-spared system. Depending on whether the cold-spared supply is in a high-impedance or low-impedance state, the active output driver could either behave as a weak power supply delivering current to the VCCB or it could be unable to swing its signal level to the level of VCCA. Either case represents a fault condition and leads to uncertainty as to how the circuit will perform.

If the cold-spared supply in the off state could be characterized as high impedance, the active output driver will serve as a weak power supply that will supply VCCB by way of the parasitic bias paths. The voltage level observed at VCCB under this condition is determined by the loading on VCCB, which is challenging to systematically define during this faulty state, and the strength of the PMOS M3 in the output of the active driver OD2 in Fig. 3.

Also, because the circuits that were intended to be cold spared are powered into an unknown state, the outputs of all cold-spared circuitry on VCCB will be biased to unexpected levels. This adds to the uncertainty of how the system operates.

Another faulty scenario is possible when the cold-spared supply VCCB is low impedance in the off state. This is a typical situation when the system is architected with active clamps that hold VCCB to VSS when powered down. In this case, the active output driver OD2 may not be able to supply the current that will be conducted through the parasitic bias paths when the cathodes of cold-spared I/Os have a low resistance path to VSS. This erroneous state would result in an output signal level at the output of OD2 that is unable to swing to the active power supply VCCA.

If the signal of OD2 is below the VIH level of the circuits that it fans out to, for instance the FPGA input in Fig. 3, the logic level of OD2 will not be interpreted correctly. Additionally, since the signal level of OD2 is below VCCA,

it will result in excessive current in the inputs to which OD2 is connected. This is commonly referred to as a shoot-through condition that would result in extra current loading on the VCCA power supply.

To avoid the situations described above, the system designer can add isolation switches in series with all cold sparable input and output circuitry. This option will add components that will drive up the system complexity, making the worst-case analysis (WCA) more challenging and potentially add a greater overall reliability concern to the system.

These extra components also add size, weight, and power (SWaP) to the hardware design. And if the isolation switches are solid state there will be additional opportunities for single-event errors.

Another solution to this problem is to use ICs whose I/Os are specifically designed with cold sparing in mind. For the I/Os to be cold sparable, the parasitic bias paths described above must be eliminated by adding additional circuits to the IC that will isolate these paths.

A subtle complicating factor is that these isolation circuits must activate without the IC having a supply present at the VCC pin since the isolation must work when the IC is cold spared. The I/Os used in all Apogee Semiconductor products have been designed to eliminate the parasitic bias paths that systems designers of redundant systems have had to struggle with in cold-spare systems.

Implementing Cold Sparing

Fig. 4 shows the structure of a standard CMOS input (Fig. 4 part a, repeated here from Fig. 2a) together with a new input buffer structure (part b) developed by Apogee. This new circuit eliminates the diodes D1, D2, D3 and D4 from the standard input buffer.

The first parasitic bias path is eliminated by replacing the stacked diodes D1 and D2 used in the primary ESD clamp with a gate-grounded NMOS labeled M1. This primary ESD clamp is still able to protect the pin from both negative and positive ESD stress even though the high-side diode D1 between the input pin and power supply is eliminated.

The second parasitic bias path that originates from the stacked diodes D3 and D4 used in the CDM clamp in Fig. 4a is replaced with MOSFETs M2, M3, and M4 in Fig. 4b. This new CDM clamp is fully capable of providing the same level of local CDM protection to the input gate oxides of M5 and M6 and eliminating the path to VCC.

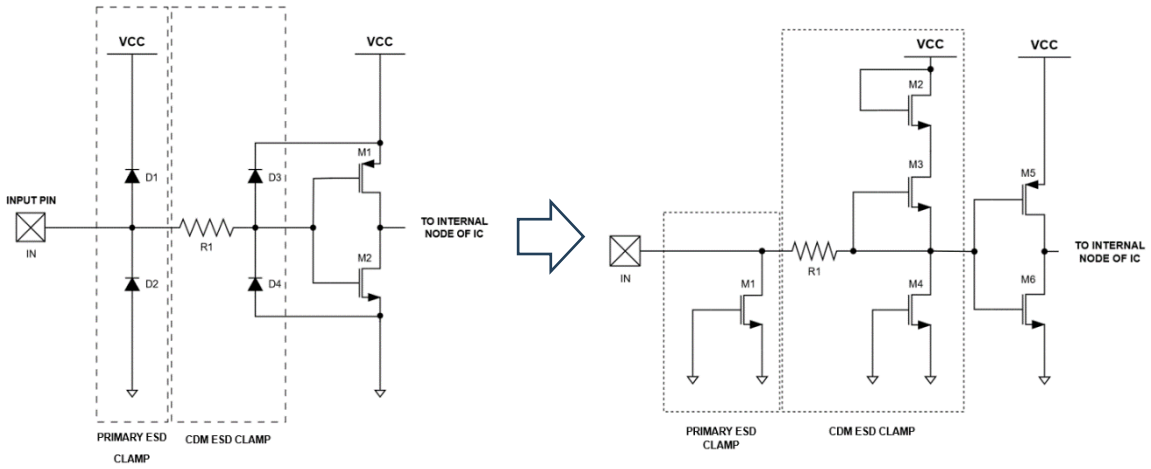

Fig. 4. A standard CMOS input (a) and a cold-spared input (b) used by Apogee. The ESD clamping diodes in the standard CMOS input structure are replaced with MOSFETs to provide the same level of ESD protection while also preventing the undesired fault conditions caused by the clamping diodes.

Fig. 5a shows the structure of a standard CMOS output (repeated from Fig. 2b) together with a new output buffer structure shown in Fig. 5b. Like the input buffer, the output buffer structure shown in Fig. 5b eliminates the parasitic bias path from the stacked diodes D3 and D4 used in the primary ESD clamp by replacing these diodes with a gate-grounded NMOS labeled M4. To eliminate the parasitic bias path to VCC from the back-gate diode D1 of the PMOS M1 in Fig. 5a, M1 is replaced by a set of stacked PMOS devices labeled M1 and M2 in Fig. 5b.

The rail-side device M1 in Fig. 5b has the source and drain connections swapped relative to M2, to reverse the orientation of its parasitic back-gate diode D1. By doing so, diode D1 now blocks the parasitic conduction path that diode D2 would have provided to VCC if M1 were not added in such a manner. This additional circuit is commonly referred to as a reverse blocking path.

However, blocking diode D1 is not enough to prevent a bias path to VCC. This is because the introduction of PMOS M1 provides a new path to supply via diode D2 and the channel of M1. To block this new path, the channel of M1 must be held off by holding the gate of M1 in a state that will prevent channel inversion from occurring. This is accomplished by deriving a control signal labeled VCC FROM PAD whose bias level is derived, and more importantly transiently activated from the signal applied to the output pin OUT in Fig. 5b.

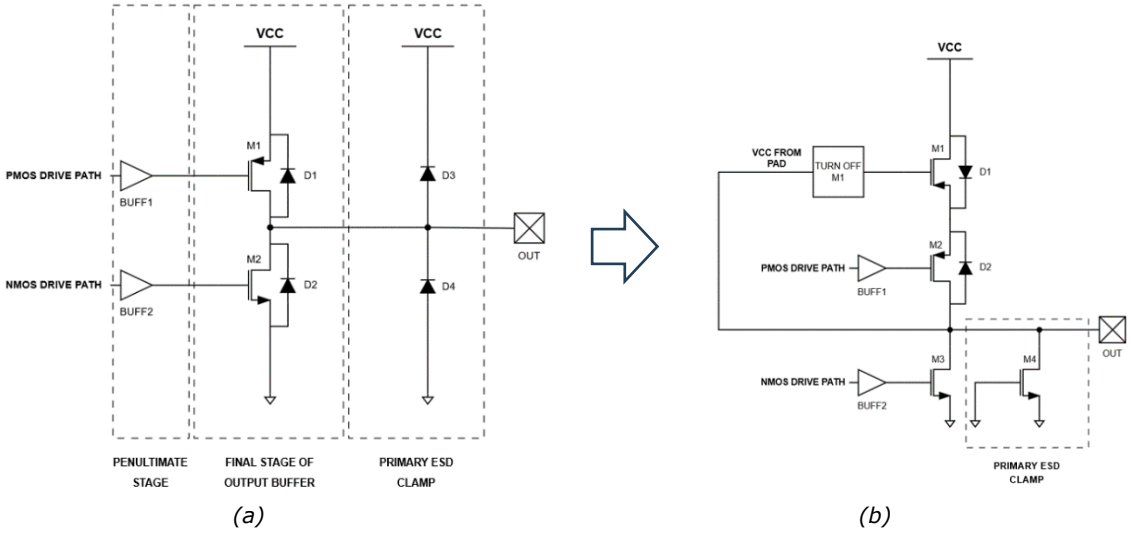

Fig. 5. A standard CMOS output (a) and a cold-spared output (b) developed by Apogee. As with the cold-spared input, MOSFETs in the cold-spared output replace the clamping diodes found in the standard CMOS output. But in this case, an additional bias circuit is needed to block current that could otherwise flow through D2 and M1 to VCC.

A key feature of this bias circuit is that it must not introduce any additional loading that would be seen by the active output driver. This attribute of Apogee Semiconductor's I/Os is referred to as Zero Power Penalty cold sparing and is a key differentiating feature of Apogee Semiconductor's cold-spare I/Os.

The way in which this signal is generated to bias the gate of M1 in a known state is complex and beyond the scope of this article—therefore it is not described here. A comparison in leakage current between an Apogee Semiconductor device with cold-sparable I/Os and a commercial-grade device with standard I/Os is shown in the table.

The commercial-grade device with standard I/Os displays a maximum leakage current of 1000 µA, whereas the Apogee Semiconductor device with cold-spared I/Os demonstrates a significantly lower leakage current, measuring a maximum of 5 µA. The higher leakage current demonstrated by standard I/Os will lead to higher power consumption and lower reliability in redundant systems.

Table. Leakage current comparison between Apogee's cold-sparable I/O and a standard I/O.

	Cold-sparable I/O	Commercial standard I/O
Leakage current (max.)	5 µA	1000 µA

The reverse blocking path that was created with the addition of M1 in the output buffer shown in Fig. 5b results in extra area when compared to the standard output buffer shown in Fig. 5a. Since M1 and M2 are in series, the $R_{DS(ON)}$ of each of these MOSFETs will add together and results in the combined resistance being twice as large as that of M1 in Fig. 5a.

To keep the resistance for the series connection of M1 and M2 in Fig. 5b equal to M1 in the common output buffer of Fig. 5a, the size of M1 and M2 must be doubled to halve the resistance of both M1 and M2. This results in the total area of M1 and M2 of Fig. 5b being four times larger than the area of M1 in Fig. 5a.

Summary

Cold sparing in space power systems requires careful consideration for fault isolation and containment. The requirements typically necessitate protection circuits that increase size, weight, and power. Newer standardized architectures, like Space VPX, specify primary and redundant power supplies that can be immediately "hot swapped" and include control backplane signals like the IPMB that need to be cold spared. To successfully implement this architecture, advanced components are needed to enable smaller 3U form factors.

When combined with the standard triple redundancy found in Apogee Semiconductor I/Os, the Zero Power Penalty cold-spare feature offers system designers an optimal choice for board-level redundant systems that demand outstanding performance in harsh environments. This feature effectively minimizes SWaP while enhancing the reliability of space systems, all while leveraging cutting-edge processes and technologies. Given the widespread use of cold sparing in space applications, all Apogee Semiconductor products in its mixed-signal logic family incorporate the Zero Power Penalty cold-sparing capability, making them well-suited for such applications.

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Mark Hamlyn is the chief executive officer and cofounder of Apogee Semiconductor. Mark has over 19 years of experience in the semiconductor industry, with a strong focus on aerospace for more than 17 years. As a founding member of Apogee Semiconductor in 2017, he previously served as the chief technology officer and as a member of the board of directors. He is located in Plano, Texas and you can contact him via email at markh@apogeesemi.com.

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For more on power protection issues, see How2Power's Design Guide, locate the "Design Area" category and select "Power Protection".