# Designing An Open-Source Power Inverter (Part 19): Controller Design For The Battery Converter

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The last four parts in this series on the Volksinverter[1-18] have provided extensive discussion on the design of the transformer for the battery converter.[15-18] Keeping the focus on this stage, in this article we now explore the design of the control circuit of the boost push-pull (BPP) power-transfer circuit (Fig. 1). As was the case with the magnetics and other aspects of the Volksinverter design covered so far, the subtleties encountered here are broadly applicable to converter control in general.

We will begin this explanation of control circuit design by observing how low output-voltage and output-current conditions on the battery converter's output port complicate converter control. Then, we'll see how to address these requirements by applying a combination of operating modes, and derive the control logic needed to implement these two modes. Based on those logic requirements, a particular control scheme will be recommended. Finally, the various exceptions to the normal controller operating modes will be described.

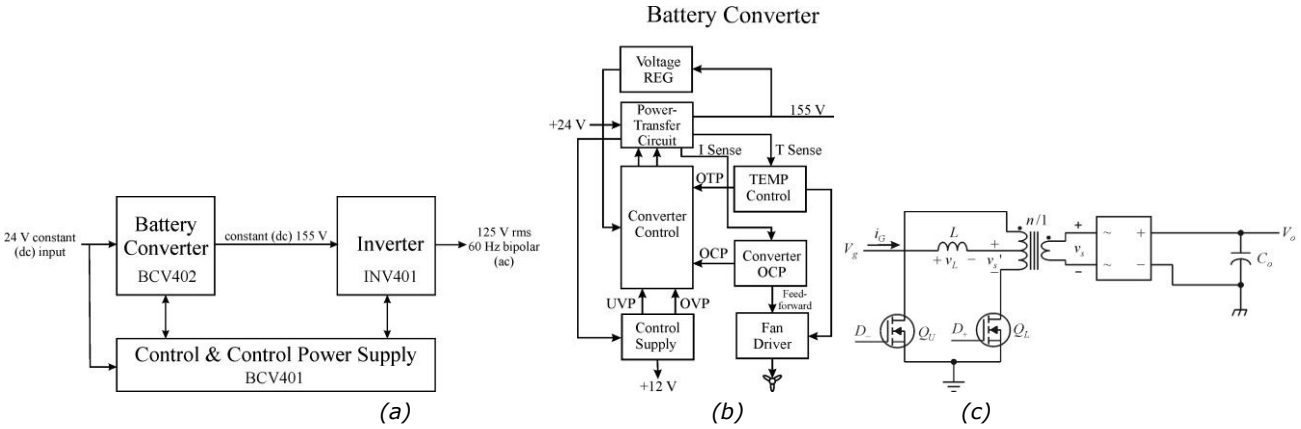


*Fig. 1. The Volksinverter's system block diagram (a), the BCV402 battery converter stage block diagram (b) and the CA (boost) push-pull power-transfer circuit (BPP) (c).*

## Output Port Design Considerations

Thus far, attention has been focused on the input port and its high-current requirement. As can happen so often in design, a concentration on the main problem can cause other essential aspects of the design to be overlooked. In this case, it can lead to neglect of the other port—the output port and how its requirements affect converter design. In particular, two output conditions create problems to be solved:

*Low* $V_o$: During power transitions (power-on and power-off), the converter secondary voltage $V_s$ is referred to the primary winding as $V_s' < V_g$, where $V_g$ is the input port voltage, and the inductor is unable to achieve flux balance over a switching cycle. This cannot be remedied with a dissipative power clamp because the low-$V_o$ state can persist indefinitely with an overloaded or shorted output and would cause excessive clamp power loss.

*Low* $I_o$: The Volksinverter must operate from its full-scale output power down to essentially 0 W for an open output. During on-time each cycle, the CA (boost) inductor is refluxed, and that energy must go somewhere. Unlike the CP (buck) configuration, which outputs zero current at a duty-ratio of $D = 0$, the CA (boost) has a nonzero output. Peak current control requires a peak current greater than 0 A to maintain control.

Both of these output-port problems are solved by either modifying or abandoning the CA push-pull configuration for a power-transfer circuit with output port characteristics like that of the CP-BRG (buck full-bridge) or, what is

commonly found in better commercial inverters, a CP-PP transfer circuit. A previous Volksinverter article concluded somewhat superior performance of a CA-PP over a CP-BRG, but is it superior to the CP-PP?

The attractiveness of the CA over the CP is based on the fact that battery converters have an output voltage much greater than the battery input voltage, and the CA is an up-converting PWM-switch configuration while the CP is down-converting. Only the transformer voltage increase from an inverse turns ratio of 1/n > 1 makes the CP a viable design alternative. Then CP 1/n must be large enough so that secondary on-time voltage $V_s$ > $V_o$.

Thus, 1/n for a CP must be greater than 1/n for a CA with more transformer secondary turns in the same winding area. Consequently, the wire (or bundle) size is reduced along with secondary on-time current $I_s$. However, for a CP, $\bar{i}_O > I_s$ because output current is CCM and increases the average by supplying the output during both on- and off-times.

On the primary side, CP on-time winding voltage is $V_g$ and for CA off-time it is $V_s' > V_g$, reducing CA primary current at the same transfer power. Smaller wire of the primary winding is traded for larger secondary wire to handle the larger CA $I_s > \bar{i}_O$. Therefore, the CA-CP difference is a tradeoff of currents and voltages.

The sole advantage of the CA is a practical one: the primary circuitry conducting input-current $I_g$ is reduced to fuse and inductor while the entire CP primary circuit must conduct more $I_g$ than the CA because it conducts from the input only during on-time. This topic reoccurs with dynamics in mind in the last part of the Volksinverter series.

## Power-Transfer Circuit

An old circuit with a new control scheme solves the "low-output" problem while maintaining the optimizing advantages of the CA. The circuit is shown in Fig. 2. Although this circuit is structurally that of a Weinberg circuit, the refinement also changes the control scheme so that it operates as a dual-mode circuit: a buck (CP) for the low-output condition ($V_s' < V_g$) and a boost (CA) for higher output power requirements. The resulting scheme controls input inductor current down to nearly zero for low output by reducing $D$ and hence the transfer ratio to zero.

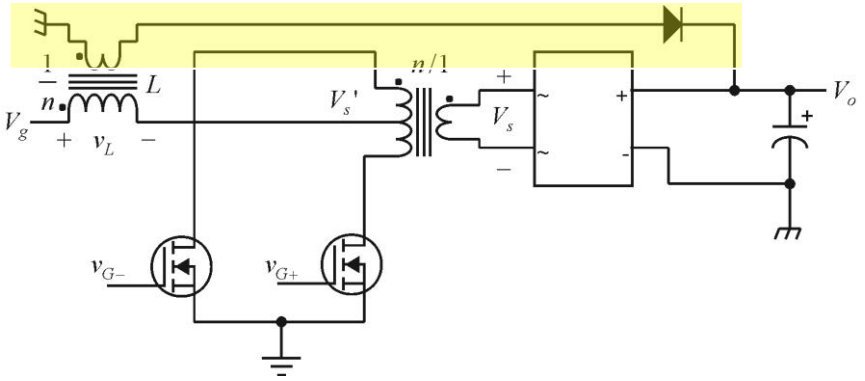


*Fig. 2. Extended BPP power-transfer circuit that operates in both CA (boost) and CP (buck) modes. In contrast with the original power transfer circuit shown in Fig. 1, the input inductor is coupled to a secondary winding that transfers inductor current to the output in CP (buck) mode during off-time and through the transformer during on-time for CP CCM output current.*

The control circuit is designed to drive the two power switches with non-overlapping on-times in CP mode as shown in Fig. 3 for the CP mode of $V_s' < V_g$. As increased load demand increases $D$ to $D$ = 1, $V_s' = V_g$, and the circuit transitions to a push-pull chopper with zero inductor on-time voltage and current ripple at average value $I_L$.

If the commanded peak current has not yet been reached at the end of the switching cycle, the peak-current comparator does not change output PWM state and the on-time is extended (to effectively $D > 1$) as the next switching cycle begins and on-times of the two switches overlap. In this case, it is better to think of $D$ as crossing over from one to zero into CA mode at the onset of overlap, and $D'$ becomes the controlling variable of output current.

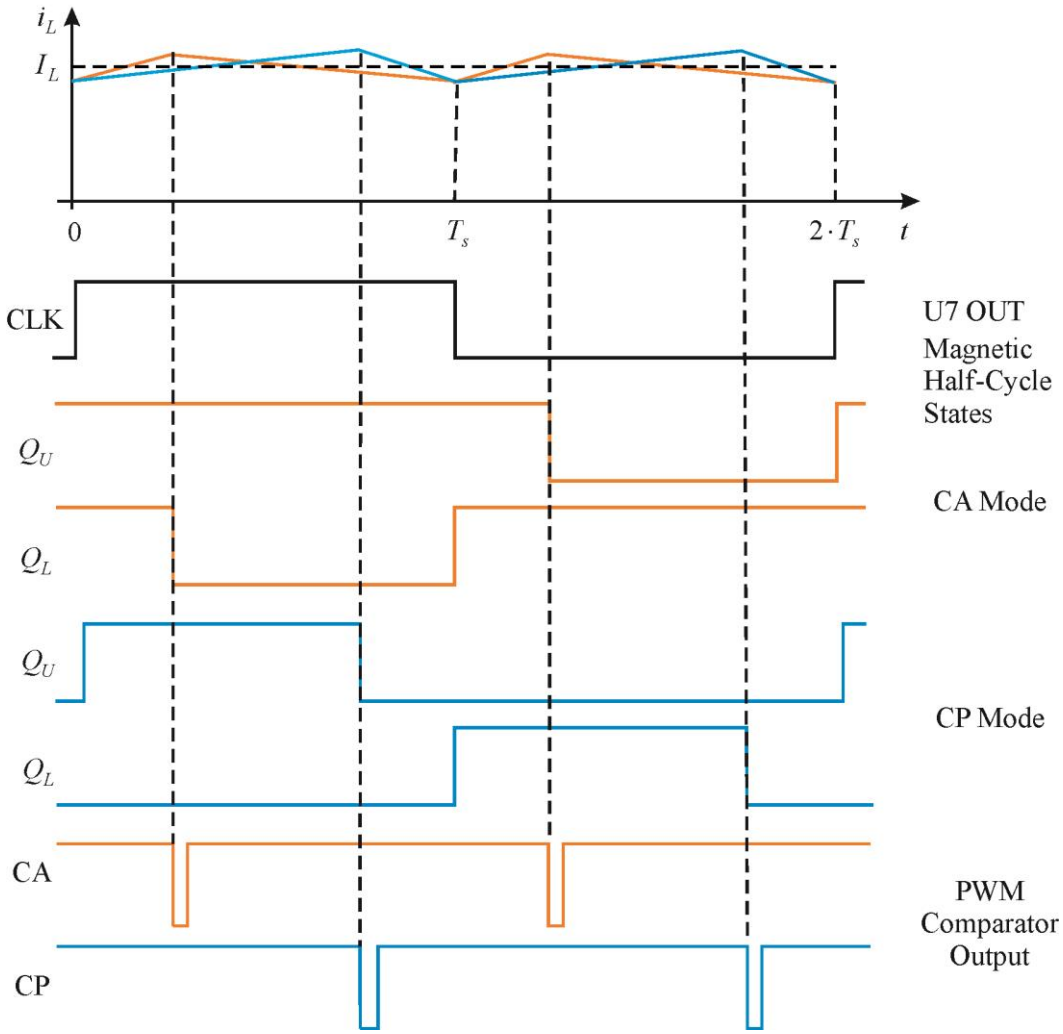


*Fig. 3. CA-CP push-pull power-transfer circuit waveforms, top to bottom: inductor currents, magnetic half-cycle clock CLK states high and low in on-time CA overlapping mode (orange) and CP non-overlapping mode (blue); CP and CA mode peak current comparator PWM outputs that end on-times.*

The BCV401 control board, shown in Fig. 4, completes the voltage control loop of the BCV402 power-transfer circuit. OCP protection circuitry is part of the prototype converter control as U5A and U6A in Fig. 4.

# BCV401 Battery Converter Control

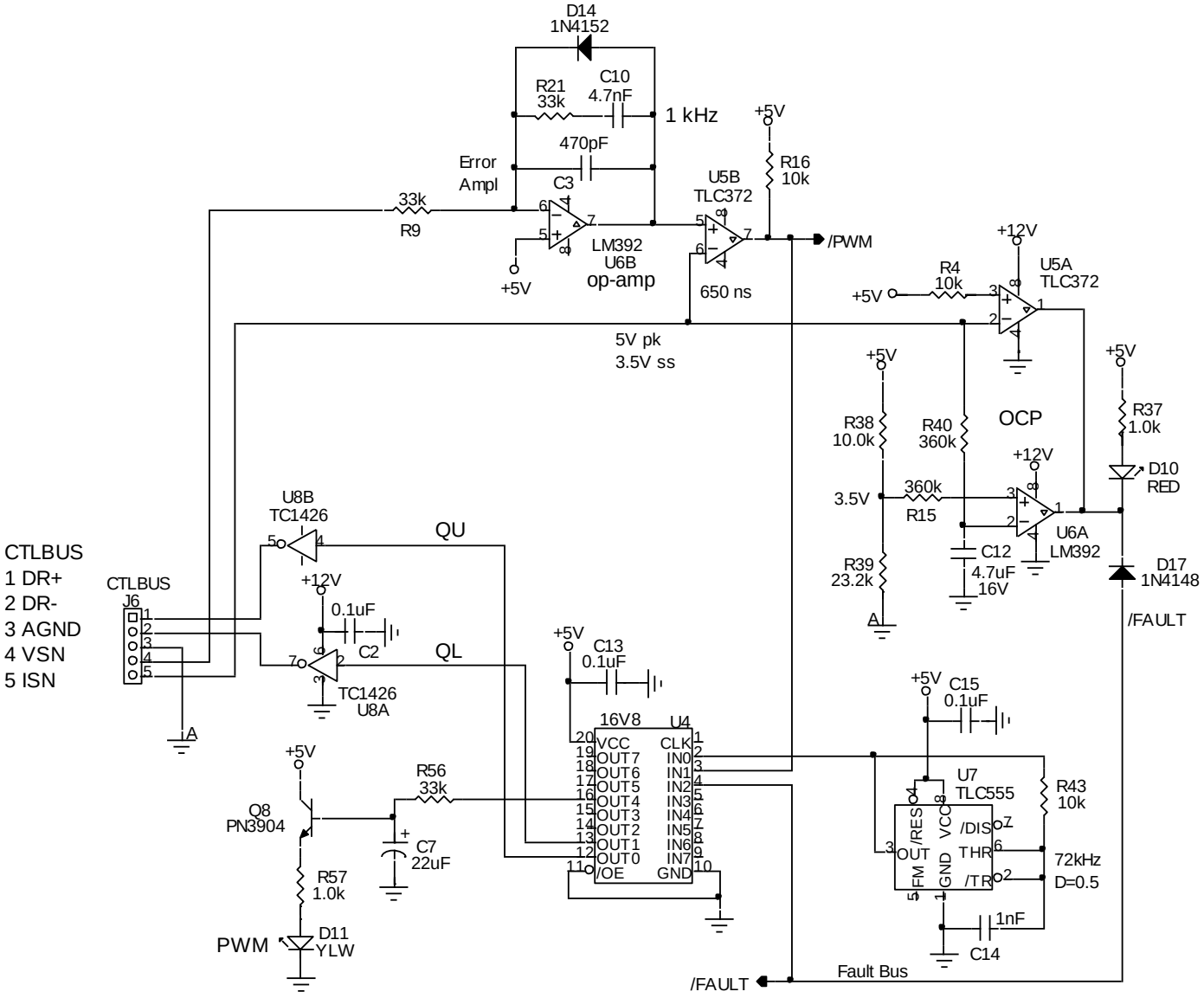


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*Fig. 4. Volksinverter prototype BVC401 control subsystem of the BCV402 power-transfer circuit.*

In CP mode, $D \approx 0$ causes average inductor current $I_L$ to become zero and the output current range extends down to zero. Switch conduction is non-overlapping, and the transfer circuit operates as a Weinberg circuit. As $i_O$ increases, $D$ increases until the chopper state is reached where for each magnetic half-cycle the switch is on for the full switching period $T_s$. The end of on-time in both modes occurs when the switch (and winding) current comparator senses the peak current and its output changes high for the brief time the current exceeds the commanded peak value.

The CP mode is shown in blue (non-overlapping) waveforms in Fig. 3, repeated again in Fig 5. It differs from the usual single-switch CP circuit in that the current for on- and off-times is delivered through different magnetic components. One switch is conducting and power is transferred through the transformer. When it switches off, inductor field current transfers to its secondary winding where the output diode conducts.

The CP mode delivers output current during both times: during on-time, through the transformer, and during off-time, through the coupled inductor. The transfer ratio when both transformer and coupled inductor have the same 1/*n* is

$$\frac{I_g}{I_o} = \frac{I_L}{I_o} = \frac{1}{n} \cdot D$$

By controlling the peak current of $i_L$, shown in the top graph of Fig. 5, the peak-current control loop controls average output current $I_o$ and adjusts it through an outer feedback loop that regulates output voltage $V_o$.

In CA (boost) mode, shown by orange waveforms in Fig. 5, the switch on-times overlap. When both switches are on, the transformer primary winding is shorted, its voltage is zero, and no power is transferred through it. The voltage across the inductor has the polarity (dotted end positive) that causes the inductor secondary winding to shut off the output diode of Fig. 2, and no current is output by it. This is CA operation.

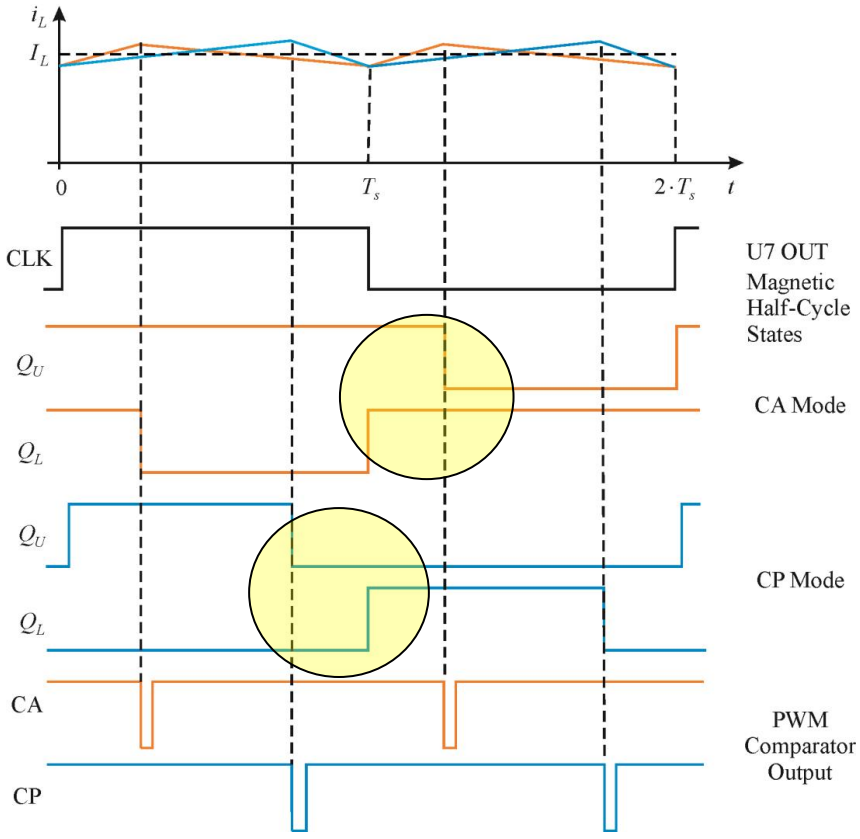


*Fig. 5. CA-CP push-pull power-transfer circuit waveforms. In CP mode, switching waveforms do not overlap, while in CA mode, they do, as highlighted above.*

Then when switch current reaches the commanded peak of the voltage-loop output $v_{Va}$ of error op-amp U6B in Fig. 4, one of the two switches shuts off, $i_L$ conducts through the other transformer primary winding and is

transferred to the output during *D*'. All power in CA mode is delivered through the transformer to the output. The transfer ratio is

$$\frac{I_g}{I_o} = \frac{I_L}{I_o} = \frac{1}{n} \cdot \frac{1}{D'}$$

In CA mode, peak-current control operates in the same way as in CP mode, varying $\hat{i}_L$ sensed by resistors (BCV402 R1 || R2) so that $I_o$ maintains $V_o$ at its commanded value.

For a given $V_g$ and a range of $V_s'$ the CA on-time slope remains constant and not less than the off-time slope magnitude. For the CP, both on-time and off-time slope magnitudes vary with $V_s'$, as shown in Fig. 6.

At the boundary of the CP and CA modes, $D$ = 1, and the circuit functions as a *chopper*. As the on-state extends and overlaps with the other switch on-state, CA mode is entered in which $D$ = 0 and the CA transfer ratio is 1/$n$. Serendipitously, the crossover between modes is continuous without power-transfer discontinuity; the two modes form a continuum of operation.

As CP $D$ = 1 its transfer function is 1/$n$ and at $D$ = 1+, CA mode is entered where the switch overlap time ≈ 0 s and the transfer ratio is (1/$n$)·(1 – $D$') = (1/$n$)·(1 – 0) = 1/$n$, the same as in the CP mode. As overlapping conduction of the CA mode increases, inductor current increases and $D$' decreases. CA flux balance (Fig. 6 green plots; $\Delta\lambda$ = 0 V·s over $T_S$) occurs only for $V_s' > V_g$ and for CP whenever $V_s' \le V_g$. Otherwise, $i_L$ in CA mode ratchets upward and in CP mode ratchets downward over complete cycles.

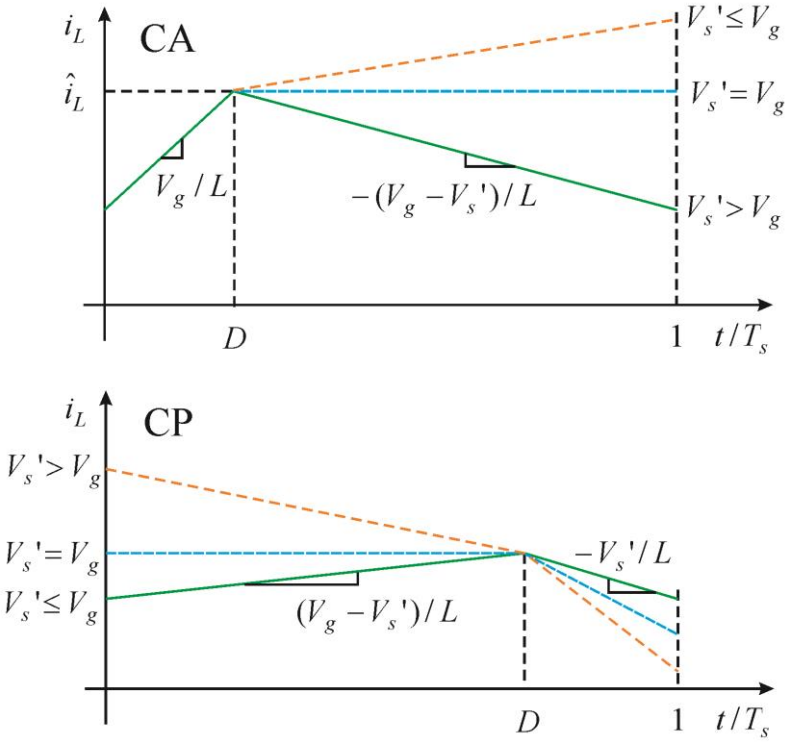


*Fig. 6. Inductor current $i_L$ waveforms for (upper) CA or boost mode of operation and (lower) CP or buck mode. The slope of CA $i_L$ during on-time depends only on $V_g$ whereas for CP, both on- and off-time slopes depend on $V_s'$. CA on-time slope is the maximum CP on-time slope when $V_s'$ = 0 V.*

## *Control Logic Circuit*

Explanation of the control logic circuit in Fig. 4 (repeated below in Fig. 7) begins with U7, a 555 timer designed to oscillate with a 50% duty-ratio at the magnetic frequency of 72 kHz. Each U7 half-cycle is a PWM switching cycle. The CLK clock waveform does not clock the flops in the programmable logic device (PLD), a GAL 16V8, because the logic is configured to be asynchronous by bypassing the register flops.

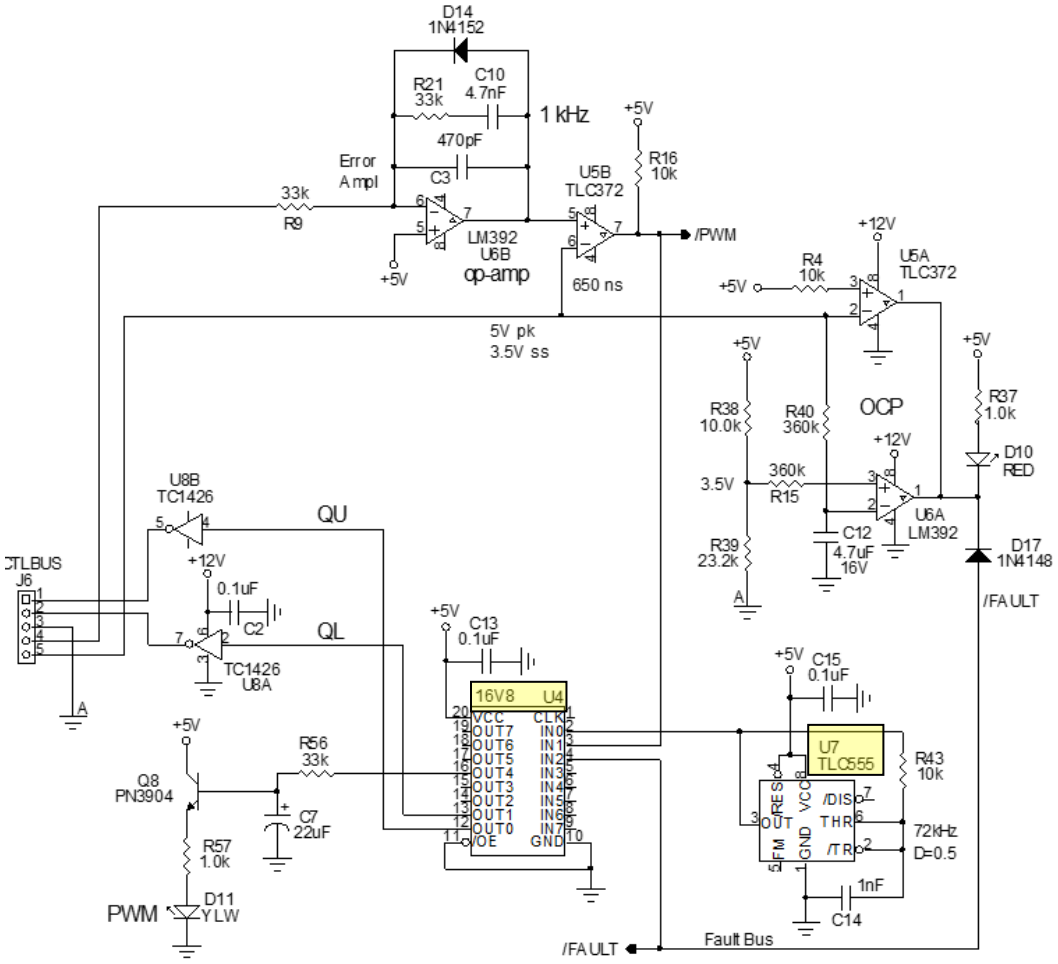


*Fig. 7. Volksinverter BVC401 control subsystem of the BCV402 power-transfer circuit with the 555 timer and GAL PLD highlighted.*

This choice is driven by the need to immediately cause (after logic propagation delays) switch states to change. Most importantly, when either overcurrent asserts /FAULT low or the peak-current comparator U5B output asserts at peak current, an immediate change of state is required, and this necessitates asynchronous logic.

Fig. 8 shows one possible control scheme. The leftmost logic state bit is the mode (CP $M$ = 0, CA $M$ = 1) and the middle and right bits are the power switch states. For instance, the state (110) = (CA, $Q_U$, $/Q_L$). $Q_U$ and $Q_L$ are the two power-switch states, inverted to drive the U8 inverters as $/Q_U$ and $/Q_L$. Equivalently, $Q_U$ = DR+ and $Q_L$ = DR−. With PLD logic, control schemes are changed simply by replacing the PLD programming.

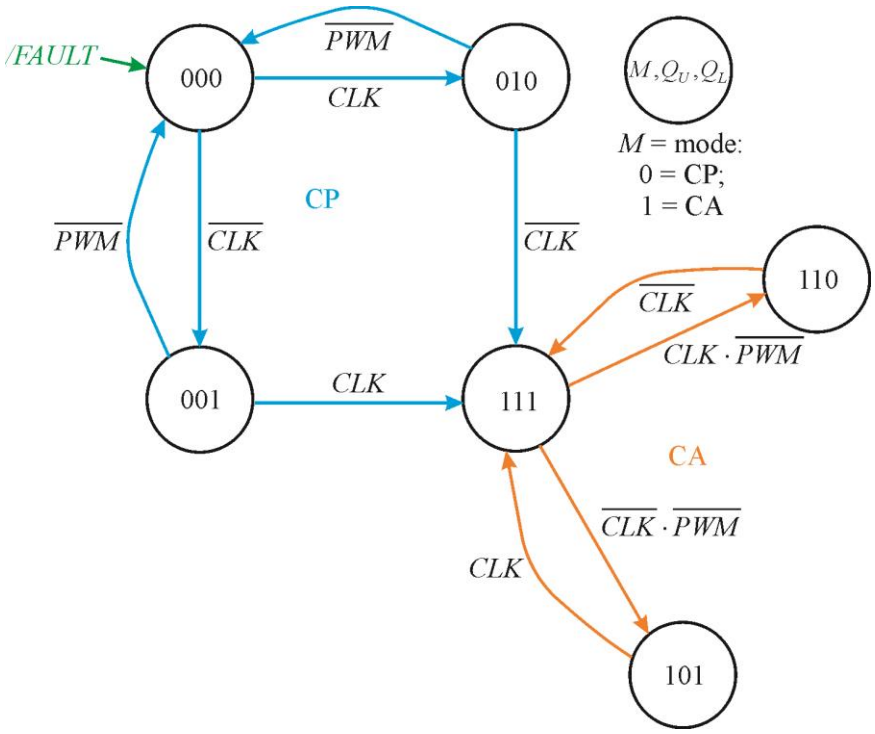


*Fig. 8. Logic flow diagram of CA-CP PP dual-mode control.*

From the logic flow diagram, the reduced boolean logic equations with ($M$, $Q_U$, $Q_L$) are

$$M := (001)\cdot CLK + (010)\cdot \overline{CLK} + (101)\cdot CLK + (110)\cdot \overline{CLK} = Q_U \cdot \overline{Q_L} \cdot \overline{CLK} + \overline{Q_U} \cdot Q_L \cdot CLK$$

$$\overline{M} := (001)\cdot \overline{PWM} + (010)\cdot \overline{PWM} + (011) + (100) + /FAULT$$

$$Q_U := (000)\cdot CLK + (001)\cdot CLK + (010)\cdot \overline{CLK} + (101)\cdot CLK + (110)\cdot \overline{CLK} + (111)\cdot CLK \cdot \overline{PWM}$$

$$\overline{Q_U} := (000)\cdot \overline{CLK} + (001)\cdot \overline{PWM} + (010)\cdot \overline{PWM} + (111)\cdot \overline{CLK} \cdot \overline{PWM} + (011) + (100) + /FAULT$$

$$Q_L := (000)\cdot \overline{CLK} + (001)\cdot CLK + (010)\cdot \overline{CLK} + (101)\cdot CLK + (110)\cdot \overline{CLK} + (111)\cdot \overline{CLK} \cdot \overline{PWM}$$

$$\overline{Q_L} := (000)\cdot CLK + (010)\cdot \overline{PWM} + (001)\cdot \overline{PWM} + (111)\cdot CLK \cdot \overline{PWM} + (011) + (100) + /FAULT$$

The U5B peak-current comparator output is */PWM* (asserted low at the current peak) and *CLK* is the U7 clock generator output. The $Q_U$ and $Q_L$ states of the asynchronous state machine are directly the (inverted) output states driving the inverting switch drivers. Whenever $Q_U$ or $Q_L$ are high, the switch they drive is on. Thus, the controller consists of asynchronous sequential logic with two state bits (four states) as outputs and three input variables.

This amount of logic is excessive for design with 74AHC- or 4000-series CMOS, and a PLD is chosen—one that can be programmed with a simple, low-cost programmer and free software to input the equations and drive the programmer. Although this involves a custom part and conflicts with the Volksinverter goal of minimizing such parts, the GAL 16V8 is not custom and has multiple manufacturers. The only customization is its logic content

and that is open-source as the programming equations given above. (Some other configuring is required to bypass registers and invert the drive outputs.)

A logic-programming or firmware language such as VHDL or Verilog is overkill for this application, and unlike FPGAs, PLDs require minimal firmware programming skills. When made available, the object code for U4 can be downloaded and fed directly to the programmer electronics, bypassing the need for PLD design software. However, corrections, updates and other design modifications are a simple matter of pulling the PLD from the circuit-board socket and reprogramming (or exchanging) it. The PLD also gives users the flexibility of inserting their own control algorithm without a change in the other circuitry on the board.

## *Operational Exceptions*

Three logic variables are inputs to the control logic: *CLK*, */FAULT*, and */PWM*. Only */FAULT* and */PWM* are feedback of the transfer-circuit state. The */FAULT* indicates overcurrent OC (or else some other fault requiring reset to the 000 state) and the */PWM* is an indicator of $V_s'$ through $V_o$. Deviation from normal converter operation identifies exceptional circuit behavior as shown in Fig. 9.

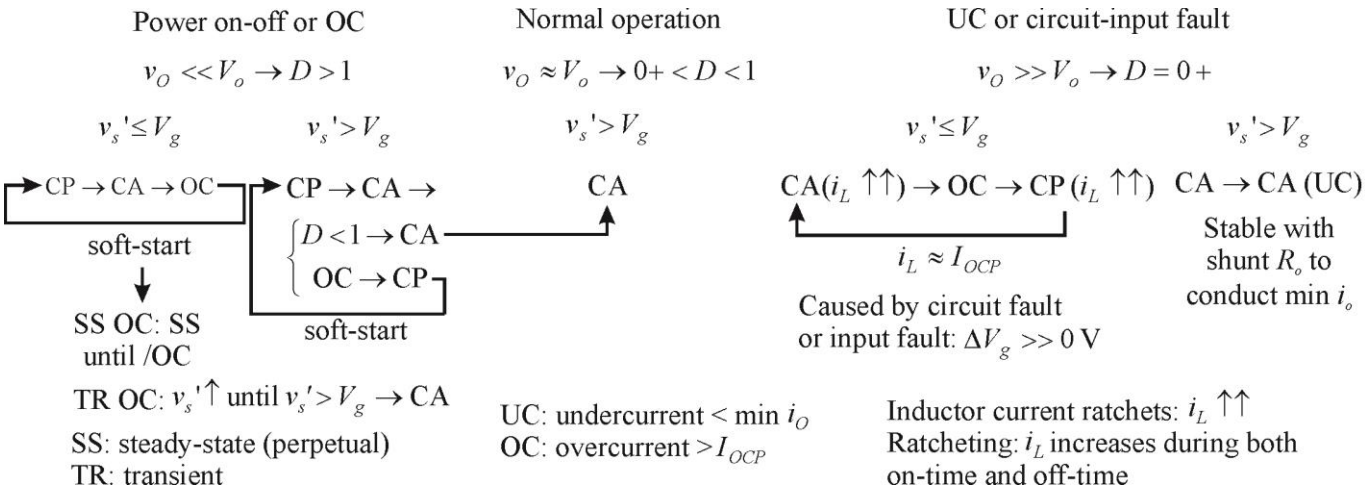


*Fig. 9. Volksinverter operations. Normal operation is the center column, power-on-off or overcurrent is to the left, and undercurrent (open-circuit output) or circuit or input faults are to the right.*

Normal operation is in CA mode, where $v_O$ is being linearly controlled by PWM in its linear range. With $v_O \approx V_o$, $V_s' > V_g$, and both output voltage and current are within their rated ranges ($V_o \approx 160$ V, $I_{UC} < \hat{i}_L \le I_{OCP}$). Then PWM has $D \in (0, 1)$—between 0 and 1 and within its design range. In normal steady-state CA operation, when both switches are on, voltage $v_s' \approx 0$ V at the center-tap of the primary windings of the power-transfer circuit, and inductor voltage

$$v_L(\text{on}) = V_g$$

Inductor current ramps up with a slope of $V_g/L$ and is steepest during on-time. During CA off-time, inductor voltage is

$$v_L = -(V_s' - V_g) = V_g - V_s'$$

Off-time inductor current $i_L$ decreases at the rate of $(V_s' - V_g)/L$ and is shallower in slope than during on-time because in normal operation by design, $2 \cdot V_g > V_s' > V_g$. With opposing on- and off-time slopes, inductor flux balance can be achieved in each switch cycle: $\Delta\lambda = 0$ V·s.

Also to be considered are exceptions to normal operation in CA mode as shown in the center column of Fig. 9. At power transitions (power-on or power-off), $V_s' \le V_g$ as shown for $i_L$ in Fig. 6 and in Fig. 9, left column; $i_L$ increases during both on- and off-time because /*PWM* never occurs ($D > 1$).

At power-on, the /*FAULT* bus is asserted by the undervoltage protection (UVP) circuit. This places control logic in CP state 000. If $V_s' \le V_g$, then $D > 1$. When *CLK* transitions, state (010) or (001) occurs and either switch $Q_U$ or $Q_L$ is on depending on the state of *CLK*. A steep on-time slope of $i_L$ will cause in one CP cycle $i_L$ to increase until $i_L > I_{OCP}$. The OCP circuit asserts /*FAULT*, setting the state to (000) and CP off-time.

However, during the prior on-time, some charge was delivered to output capacitor $C_o$ and $v_s'$ increased. Typically, *L* is large enough to avoid OC, and with no /*PWM* to keep the state machine in CP mode, it advances in Fig. 8 to (111) in CA mode from either (010) or (001).

In CA mode, $i_L$ continues to increase, ratcheting upward, because there is no PWM and no off-time. When the OCP circuit asserts /*FAULT*, the state is reset to (000) and this *soft-start* cycling of CP → CA → OCP → CP repeats until either the output OC fault is removed or lessened so that $v_O$ increases to where $v_s' > V_g$.

Then in CP, $i_L$ decreases during the entire (on-time) cycle, ratcheting down ($i_L \downarrow\downarrow$). Flux balance in CP mode requires $V_s' \le V_g$. Then (Fig. 9, left column, right side) the CP → CA → CP soft-start loop repeats until $v_O \approx V_o$, voltage regulation resumes, and operation reverts to normal.

When soft-starting in CP mode at low $v_s'$ and no off-time, eventually *D* exceeds 1, changing the mode to CA. This mode change is continuous as *D* changes from 1 for CP non-overlapped switch conduction to 0 in CA mode on-time. As the /*PWM* pulse delays further, CA *D* increases, increasing $i_L$.

At power-off, the control PS +5-V and +12-V outputs are disconnected from $V_g$, no voltage is available to drive the power switches on, they are shut off, and $C_o$ across the converter output is discharged by the inverter load. Both PS outputs have output capacitors that discharge to 0 V, but while they do if they hold up longer than $C_o$ (that is, $v_O$), then the Fig. 9 left column repeats.

The other extreme in exceptions is the right column in Fig. 9—an open-circuit or undercurrent (UC) load or any transient load removal causing $v_O >> V_o$ and PWM below the low end of its range. The PWM comparator cannot be driven to the ISN low range limit of 0 V but can only decrease to around 0.5 V. This leaves $D > 0$, or $D = 0+$. The converter is in normal operation in CA mode before the exception.

This scenario can occur if a load is suddenly removed from the output, causing an open circuit and $i_L \approx 0$ A. Then the voltage-regulating PWM decreases *D* to its minimum value of $D = 0+$ where a small amount of current is output each cycle. CP and CA modes both input power each cycle from the input port and it must go somewhere yet not exceed the discharge rate $I_{UC}$ of $C_o$.

In CP mode, if load current decreases (such as from an output open-circuit) causing $v_s' > V_g$, the inductor flux is unbalanced, the voltage-control loop decreases *D*, the inductor defluxes, and $I_L$ decreases to nearly zero. Yet the CP mode delivers current to the output for the full cycle unless it becomes DCM. The CA has some advantage in that current is only output during off-time. For this exception, $i_L$ for both CP and CA modes would become DCM.

The OCP circuit has a dual function. It not only protects against overcurrent but also becomes part of the control loop for exceptional conditions. The peak-current control loop through U6B and U5B of ordinary operation has a minimum duty-ratio of

$$D_{\min} = \frac{t_{dly}}{T_s}$$

where $t_{dly}$ is the delay time from when the current peak in the power switch(es) occurs (fed back as scaled voltage across sense resistor $R_s$ of the BCV402) until the power switches shut off. If $i_O$ is in a range from 0 A to $I_{UC} = I_{omin}$ corresponding to

$$t \in [0\text{ s}, t_{dly}] \Rightarrow D \in [0, D_{min}]$$

then current ratcheting occurs at $D = D_{min}$.

This form of ratcheting is the incremental cycle-by-cycle increase of current caused by the failure of the control circuit to maintain flux equilibrium because it cannot control $D$ below the value of $D_{min}$. The switches are on too long and the switching cycle ends with more peak current than commanded. Eventually, this ratcheting causes switch current to exceed the OCP threshold, /FAULT is asserted, the controller state is reset to CP (000), and the power switches are shut off.

If converter shunt output resistance is not low enough to prevent $v_O$ from increasing, the resulting control behavior for persistent low $i_O$ is bursts of cycles as OCP control alternates with the peak-current loop in a *burst-mode* operation—a kind of *chirp* behavior.[19] Some commercial converters have a "chirp mode" whereby attempts are made to supply some output current until a load fault clears. The BCV401 scheme operates the converter at the switching frequency of *CLK* that allows rapid recovery from a fault mode.

The Weinberg circuit in CP mode transfers current to the secondary winding of the PWM-switch inductor. By design, it can be diverted either to the output or returned to the power input port at $V_g$. The output option avoids a chirp mode only if the minimum output current is above an amount that keeps $D > D_{min}$. Otherwise, the diode can be connected to the $V_g$ node instead of $V_o$, to recirculate input power back to the input port.

The final exception, of $v_O >> V_o$ and $v_s' \leq V_g$ is an odd one, for $v_s' \approx v_O/n$. If somehow $V_g$ instantly increases, this might be possible, but that does not happen with batteries and a short (low-inductance) battery cable at the input port. The other possibility would be a circuit fault requiring shutdown and repair—a situation not requiring control to address. If these conditions were to occur, a soft-start-like cycle occurs that holds $i_L \approx I_{OCP}$. In a short time, $I_{OCP}$ would decrease to the steady-state OC threshold in which the converter can run continually.

By combining CP and CA modes with OCP control, the full range of allowable $I_o$ can be controlled. Inductor flux imbalance causes inductor current ratcheting and OCP modes that output constrained current until the fault clears. Then $V_o$ again rises as the transfer circuit storage capacitor charges and the voltage control loop again functions.

The peak-current loop supplies PWM within the outer voltage control loop. Peak-current control dynamics are quite involved and explained in another *How2Power Today* article series.[20] Error amplifier U6B has frequency compensation for stable voltage-control loop behavior. Integration capacitor C3 forms a pole at the origin while R21 and C10 add a zero at 1 kHz. This is a typical form of compensation for outer-loop voltage control of peak-current controllers.

D19 limits peak current comparison to a diode drop above the full-scale peak value of 5 V. Whenever $v_O << V_o$, rising $i_L$ asserts the OCP (5 V) instead of the higher PWM threshold (at about 5.6 V); the PWM allows continual on-time. The OCP circuit then takes over control of the current loop, determining off-time by asserting /*FAULT*.

An output from the U4 PLD is averaged by RC integrator R56-C7 and drives Q8 which lights D11 to a brightness that varies with $D$ for a visual indication of PWM activity. U9A and B are inverting MOSFET gate drivers that output through the control bus (CTLBUS) connector to the BCV402.

## Conclusion

This dual CA-CP scheme is new and its possible behaviors are still being studied to make sure the theory of operation is complete and correct. The BCV402 power-transfer circuit has not been tested to satisfactory

completion yet on the bench but is not expected to present as many unanticipated problems as the BCV401 control subsystem.

If you have an interest in off-grid battery-input inverters, consider joining the Volksinverter project as an Innovatia Assistant so that you can participate in and benefit from ongoing inverter development. This includes all aspects of the project including the detailed design of the magnetic components. The design of the BCV402 power-transfer magnetics will appear in the next article in this series.

**Acknowledgement**

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6. "Designing An Open-Source Power Inverter (Part 6): Kilowatt Inverter Control Circuits" by Dennis Feucht, How2Power Today, August 2022.
7. "Designing An Open-Source Power Inverter (Part 7): Kilowatt Inverter Magnetics" by Dennis Feucht, How2Power Today, September 2022.
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13. "Designing An Open-Source Power Inverter (Part 13): The Differential Boost Push-Pull Power-Transfer Circuit" by Dennis Feucht, How2Power Today, June 2023.
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17. "Designing An Open-Source Power Inverter (Part 17): Transformer Winding Design For the Battery Converter—Alternative Configurations" by Dennis Feucht, How2Power Today, May 2024.

18. "Designing An Open-Source Power Inverter (Part 18): Transformer Winding Design For The Battery Converter—Secondary Winding Design" by Dennis Feucht, How2Power Today, July 2024.
19. Control modes such as burst mode and peak-current control are explained in more detail in *Power Converter Design Optimization*, D. Feucht, Innovatia (innovatia.com), in the volume *Converter Dynamics* in the chapters "Converter Control" and "Peak Current Control".
20. "Special Series On Current-Mode Control" by Dennis Feucht, How2Power.com.

**About The Author**

*Dennis Feucht has been involved in power electronics for 40 years, designing motor-drives and power converters. He has an instrument background from Tektronix, where he designed test and measurement equipment and did research in Tek Labs. He has lately been working on projects in theoretical magnetics and power converter research.*

For further reading on power supply control topics, see the How2Power Design Guide, locate the Design Area category and select "Control Methods".