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Dynamic Load Stepping: A New Paradigm For Determining GPU/ASIC Power Rail Stability And Impedance

by Steve Sandler, Picotest, Phoenix, Ariz.

As GPUs, ASICs, and CPUs continue to push the boundaries of performance, the power systems that support them face unprecedented challenges. Before these advanced processors can be safely powered and tested, their power rails must undergo rigorous assessment. This means in-system testing of voltage regulators (VRMs) without the processors installed, implying use of some type of electronic load.

However, such testing is challenging as the dramatically increasing performance demands of modern processors require the e-loads to emulate massive, arbitrary current draw profiles at nanosecond edge speeds. While such challenging load profiles are being applied to the power system, engineers must evaluate critical factors like stability, large-signal voltage responses, and crosstalk between adjacent power rails.

The escalating power densities in smaller advanced chip sockets, combined with the widespread use of refrigerated liquid cooling systems, further complicate testing. These cooling solutions often obscure key test points and necessitate longer cables, amplifying ground loop errors and making traditional testing techniques impractical. Methods such as load step response testing, Bode plot analysis, and even modern impedance measurements are falling short when applied to today's high-current, high-speed power planes.

This article explores the limitations of the traditional approaches to power rail assessment, highlights the innovations driving a new generation of electronic loads, and introduces dynamic load stepping as a paradigm-shifting solution for assessing the demanding power requirements of cutting-edge GPUs, CPUs, and ASICs.

In The Beginning

When I began my career in power electronics almost five decades ago, we tested stability using a step load, which at the time used a resistor. We used clip-leads to connect the resistor across the power supply. We used one of the clip-leads to connect the resistor or disconnect the resistor, creating the step. It wasn't elegant, but it worked well enough until we got a bit fancier.

In the fancier version we used a transistor switch. We switched the transistor on, placing the resistor across the output and we switched the transistor off opening the resistor connection. The bipolar transistor was driven from an external pulse generator. It was simple, but it worked better than using a clip lead.

Keep in mind that Alex Lidow hadn't invented the HEXFET yet, which would have made this easier. At the end of the day, this worked as a rudimentary test for the control loop stability of our (mostly) linear regulators.

A bit later, in March 1980, Dean Venable presented his paper at Powercon 7, titled "Practical Techniques For Analyzing, Measuring And Stabilizing Feedback Control Loops In Switching Regulators And Converters".[1] This won the best paper award, and he went on to popularize the Bode plot measurement and ultimately created his company, Venable Instruments, where he made frequency response analyzers (FRAs) which are still produced today.

While the Bode plot proved useful, engineers still did step load testing, in addition to the Bode plot, as an additional stability verification. This turned out to be with good reason and many articles have been written about the limitations of Bode plots.[2,3] Devices then started to get more integrated and many, three-terminal regulators, for example, didn't provide access for Bode plot measurements. Switchers have become complex with multiple internal loops. Newer methods were needed.

Impedance turned out to be an effective measurement that correlates with the step load response and provides reliable design insight. This became the fundamental basis of power integrity evaluation and Larry Smith created target impedance in 2007, the fundamental power integrity design criteria.[4]

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This worked well, but still had weaknesses in that it assumed that the PDN impedance was flat. If it wasn't, it was possible to create rogue waves whose superposition somewhat nullified the assessment.[5, 6] It also didn't tell us about voltage regulator module (VRM) stability, which is still a key factor in power supply design.

In 2011, I developed NISM, non-invasive stability measurement, which extracted stability information from impedance data.[7] The NISM result relates to the Nyquist stability margin, which coincides with the step load response. We now had a complete set of tools for stability assessment that worked, whether the data was extracted from impedance data, step load data, or Bode plot data.

This was hugely beneficial and the NISM impedance assessment started showing up in instruments like the Keysight E5061B and OMICRON Lab Bode VNAs. NISM is now available in many instruments and EDA tools such as PSpice and Keysight ADS. Traditional Bode and NISM assessments have worked well for a while now, but recently, even newer, more daunting challenges have appeared.

While impedance is a small signal, linear measurement, non-linear controllers can provide ambiguous data. Not that impedance is to be abandoned; it is still a very useful design tool, but more techniques are needed to expand our portfolio to extract high-current, large-signal responses, crosstalk, and thermal design (TDP) testing. And we still need to extract VRM stability information.

Some systems have the added complexity that they cannot run steady-state loads. One example is pulsed power amplifiers for radar systems. In these applications, in addition to the non-linear control topology that requires large-signal testing, the system cannot be operated long enough to complete VNA impedance sweeps as required by NISM.

On the other hand, impulse or step testing allows a very short operating time to extract the information. The minimum operating time is the period of the lowest frequency of interest. For example, extracting information starting at 1 kHz requires the system to operate for only 1 millisecond.

Fortunately, a well-designed, minimally invasive, step load can create the necessary stimulus for these applications and give us the test data we need. Extracting stability information is a bit more difficult and not quite as mainstream. However, when I developed NISM, I also developed a time domain counterpart, called SEPIA, which stands for stability evaluation for power integrity analysis. While there was little interest in SEPIA in the past decade, necessity has made it more popular.[8]

SEPIA uses inverse Laplace and/or FFT to convert the pulse data to impedance and/or directly to Q (a stability derivative so to speak). Time domain measurement uses linear scales while VNA measurements use log scales. This is true in both the X and Y axes and results in greatly reduced dynamic range in the time domain measurements, but the large current steps counterbalance this loss. The good news is that it is now feasible to use large-signal, dynamic load stepping to excite and assess even the highest-powered GPU boards.

This is not to say that the migration to high-speed dynamic testing is simple. Maintaining high speed, minimally invasive dynamic performance practically eliminates the use of traditional electronic loads (e-loads), which can interact with the power supply control loop. I showed this issue in my book, Power Integrity.[9] These conventional e-loads are too slow, too capacitive, and the interconnects to them are too inductive. Most high-power boards also don't offer connectivity to support such a load.

Responding to these limitations, a test solution developed by Picotest overcomes the shortcomings of conventional e-loads to enable high-speed dynamic load stepping.

The interconnect limitation is solved by moving the step loader to a probe format so that it is close to the test board, minimizing the interconnect impedance and maximizing the speed. This resolves the interconnect inductance, but also moves the thermal aspects to the probe head. In other words, the probe itself must dissipate a massive amount of power, demanding water cooling.

Picotest's solution addresses another test issue. In cases where conventional e-loads cannot generate sufficiently high current loads, typically custom e-loads are designed for a particular BGA pattern and socket. But then, supporting the large variety of BGAs and sockets is also a challenge. With the Picotest solution, this

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challenge is met by reducing the load design to an array of miniature load cells, drivers and fanout distribution drivers. This simplifies each new design to the placement of well-defined GaN load cells on a printed circuit board where the load cells work in tandem to produce the nanosecond load steps required.

This method eliminates the need for spring-ping interposers that would insert significant impedance or elastomer interposers which have limited life cycles. Additionally, either of these solutions would also be custom designed for each socket.

The load controller is a separate 16-bit board, with its own application software. This allows the controller to be multi-application, while reducing the cost of the in-socket load board, which only contains the dynamic load. A cooling manifold is placed on top of the in-socket load for cooling, and depending on the application, this is often water-cooled, particularly for AI, data center and high-performance computing applications. Fig. 1 below presents an example of one of Picotest's in-socket load boards employing the GaN load cells.

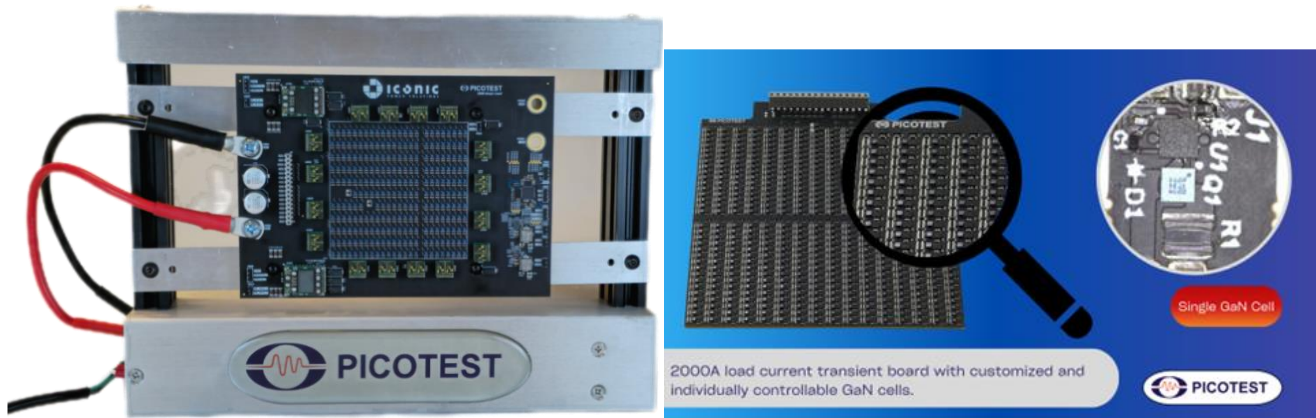

Fig. 1. Picotest's dynamic load stepping solution. In a lateral power delivery design, the voltage regulator modules are around the outside perimeter of the ASIC. In the continued push for improved efficiency, there is concern about the power loss in the PCB planes, which is not insignificant, but... GaN cells enable fast load current transitions and can be combined to source thousands of amps/ns, and still be water-cooled by a custom manifold. One of Picotest's in-socket load boards is shown in socket on the left and by itself on the right with a closeup of a load cell in the upper right hand corner.

With the Picotest solution, dynamic loading has evolved significantly to meet our new challenges. High-speed, minimally invasive, step loaders are capable of 2,000 A/ns or more with up to 11-bit, 1-A resolution at 66 MSPS. These GaN-based loads fit in ASIC style sockets, are capable of steady state TDP testing, and can be programmed on the fly to emulate ASIC workflow.

These devices meet the challenge of non-linear controllers, crosstalk assessment, and multiple power domain support. SEPIA can be used to directly extract stability information, and even extract a lumped broadband model. Impulse testing can be used to extract impedance information to microohm levels and even generate a Bode plot.[10] Figs. 2 through 5 highlight the capability of the load board and its 11-bit 66-Msamples-per-second controller hardware and software to emulate various loading profiles.

While we have come full circle with a return to load-step testing, clearly this is not your grandfather's step loader.

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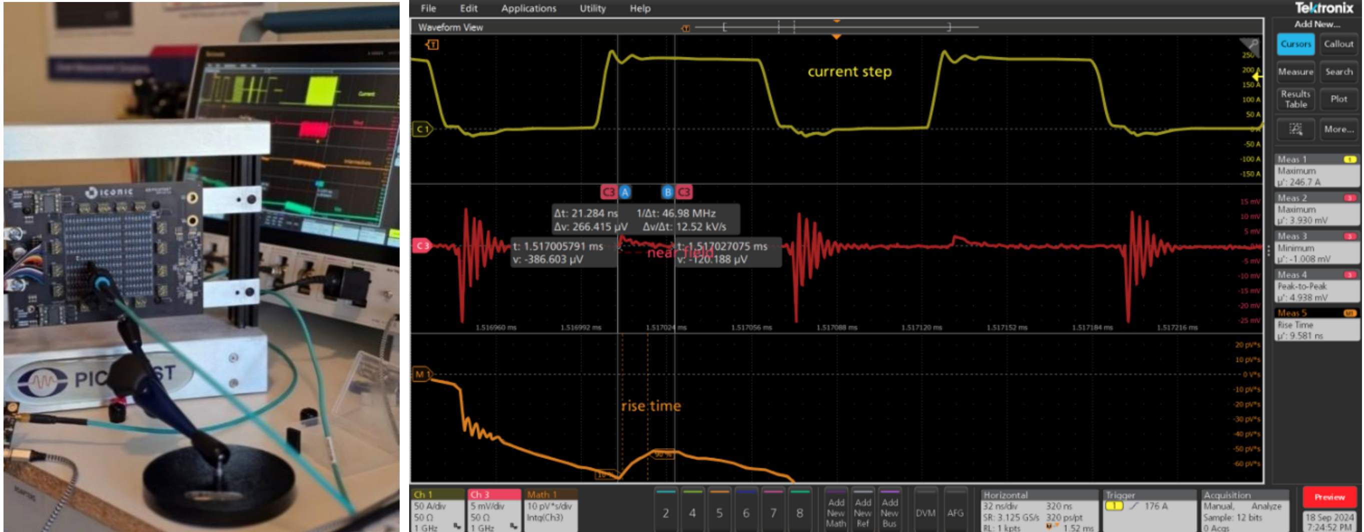

Fig. 2. GaN power transistors have enabled significant advancements in transient step load testing, pushing the current magnitude and edge speeds to thousands of amps/ns while allowing complex user pattern control.

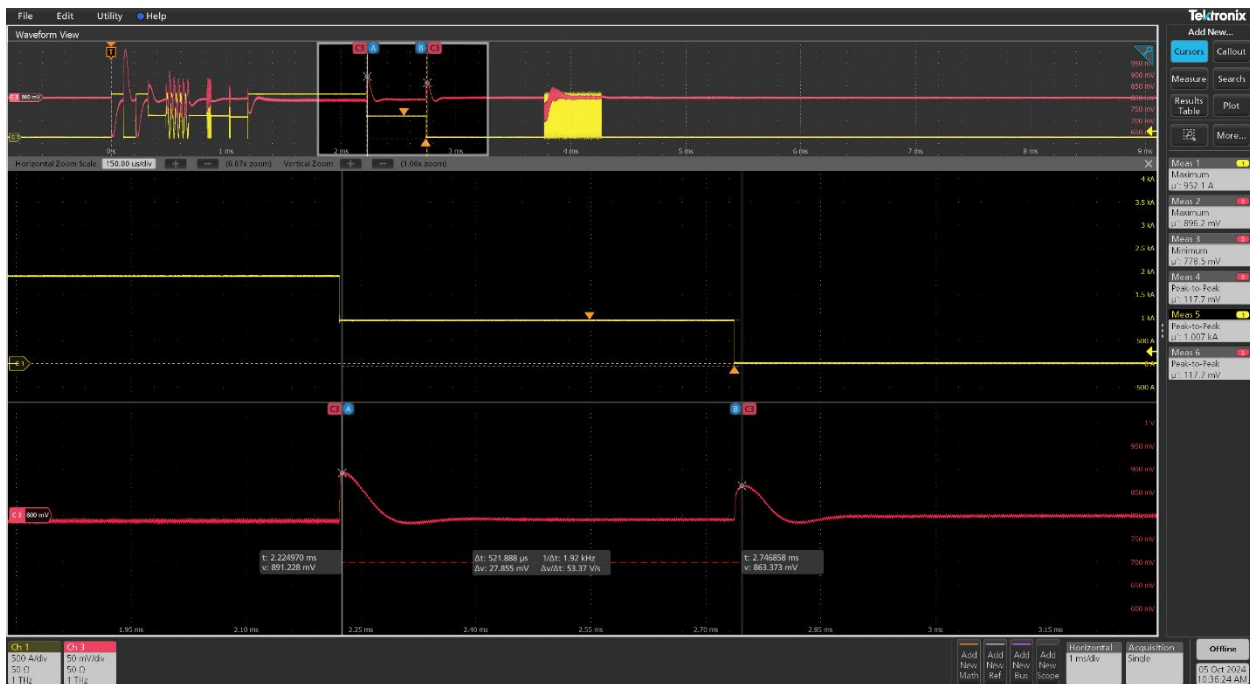

Fig. 3. At high currents, the output response isn't linear. In this screenshot, the response to a 2000-A to 1000-A load current step is not the same as the response to a 1000-A to 0-A step. This large signal effect is due to much greater inductor energy stored at 2 kA than at 1 kA, since energy is related to the square of the current, not the current. Note: even the shape is different.

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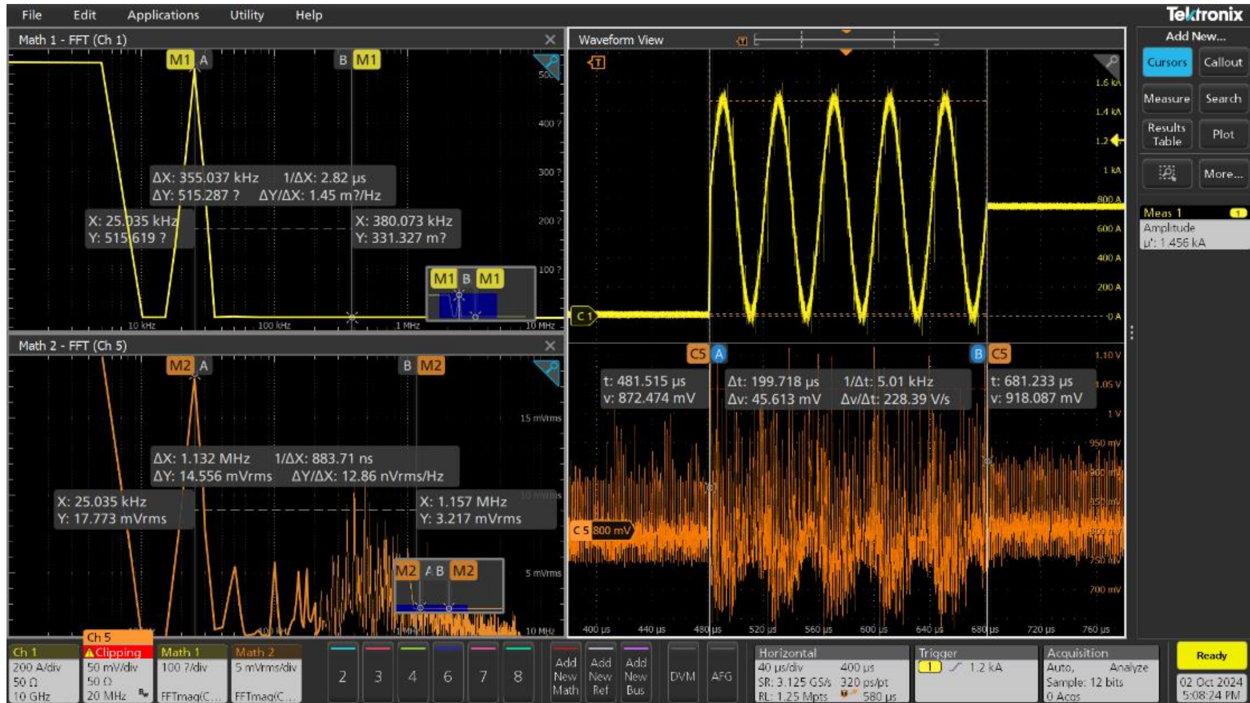
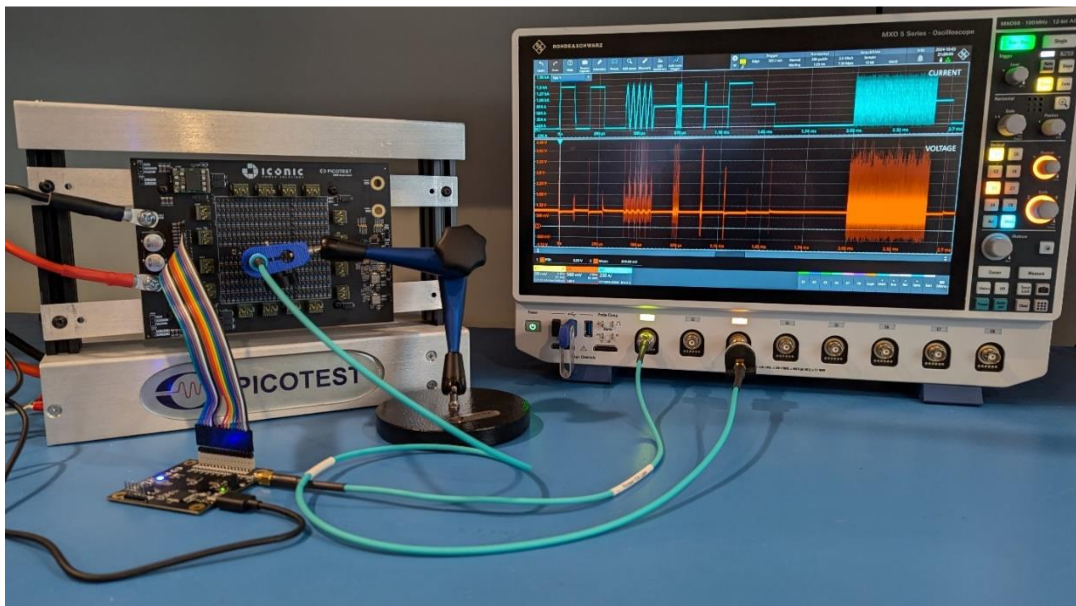


Fig. 4. 32 µΩ in a two-port shunt-through is -118 dB. With a source power of even 25 dBm, this requires a measurement at -93 dBm, which is close to the typical noise floor. And most VNAs can't get to 25-dBm signal output. Using a high-speed, in-socket load, we can measure the voltage simulated by a 1500-A peak-to-peak sine wave and use FFT to calculate impedance.



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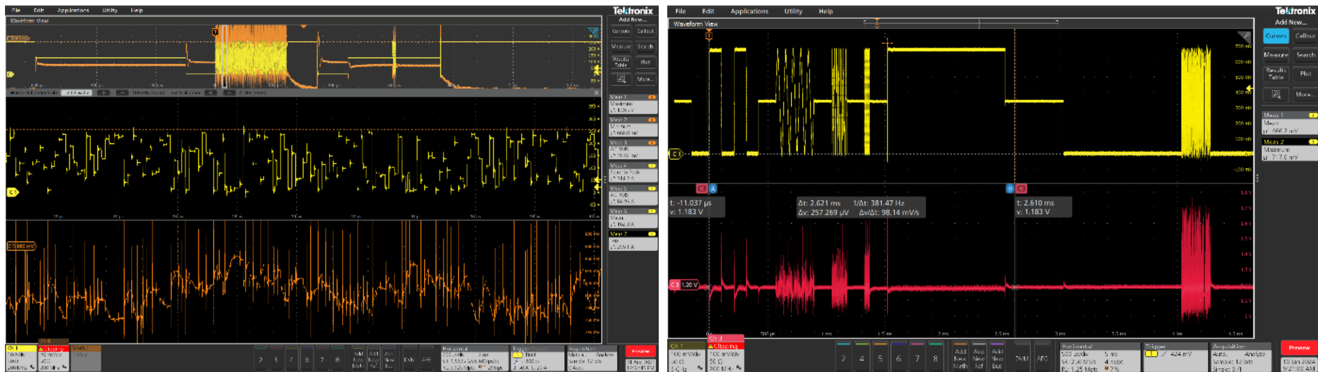

Fig. 5. Transient load step testing has come a long way. 2000-A/ns patterns (Sine, step, pseudo-random) test the latest ASICS.

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About The Author

Steven Sandler is the managing director of Picotest, a company specializing in precision test and measurement equipment. Sandler is also the founder and chief engineer of AEi Systems, where he leads development of high-fidelity simulation models for all types of simulators as well as the design and analysis of both power and RF systems. Sandler has over 30 years of experience in engineering and is a recognized author, educator and entrepreneur in the areas of power, RF and instrumentation. His book, "Power Integrity: Measuring, Optimizing and Troubleshooting Power Related Parameters in Electronics Systems," was published by McGraw-Hill Education.

For further reading on power supply stability testing, see the How2Power Design Guide, locate the "Design Area" category and select "Stability".

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