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Current-Mode Controlled DC-DC Regulators (Part 3): CC-CV Regulation

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This article, part 3 of a multipart series, examines a constant-current, constant-voltage (CC-CV) dual-loop architecture for a dc-dc regulator that provides a constant output voltage or constant output current, depending on the application requirement and operating condition. Previously, part 1 reviewed the small-signal behavior^[1] of the CV loop, including considerations for slope compensation, and presented the control-to-output transfer function for a buck regulator. Part 2 examined compensation design^[2] for the CV loop, while simultaneously optimizing the load transient performance.

In this installment, I list several applications with current-source-type loads that require CC-CV operation, and outline incumbent designs for the CC circuit that work as an add-on to a conventional dc-dc regulator with a CV loop. These are cases that essentially require the designer to modify a CV regulation scheme by supplementing the feedback loop with external circuits. I then detail a CC-CV integrated circuit (IC) approach with low external component count, reduced cost, accurate current-setpoint performance and improved transient response.

The proposed IC implementation is unique in that it selects the minimum of the currents from the transconductance error amplifiers in the CV and CC loops. This selected error current then flows in a shared compensation component network, the resultant compensation (COMP) voltage becoming the reference command of the inner current loop of the current-mode architecture detailed in parts 1 and 2.

The small- and large-signal dynamics of the CV and CC loops are quite similar, and only one error amplifier is active at a given time, thus minimizing loop interactions and yielding a seamless handoff from CV regulation to CC and vice versa. Simulation results of the CV and CC loops, and a laboratory testbed based on a commercially available CC-CV synchronous buck controller (the LM5190-Q1) illustrate the performance characteristics of the dual-loop architecture.

CC-CV Applications

A notable application of CC-CV is found in multicell battery stacks within a high power-density battery energy storage system. Other applications that require CC functionality include the battery backup unit (BBU)^[3] for the 48-V bus in server racks, supercapacitor (supercap) energy backup systems, and current limiting during power expansion in portable power stations.

As an example, Fig. 1 shows the block diagram of a power-architecture to charge an 11S lithium-ion battery, highlighting the CC-CV functionality of the dc-dc regulator. For example, the 11S6P (18650 type) battery pack specified in an Open Compute Project Open Rack version 3 (OCP ORv3) server BBU module^[4] operates from 28.6 V to 44 V and charges at up to 5 A, depending on the previous depth of discharge of the battery capacity.



Fig. 1. An 11S6P battery pack in an ORv3 server BBU charged by a dc-dc regulator with CC-CV.

Meanwhile, Fig. 2 illustrates the CC-CV charging profile^[5] of a supercap module in applications such as batteryassisted engine starting (especially for cold or frequent starts); graceful system shutdown for robots; emergency backup energy for industrial computers; wind turbine pitch control; and industrial peak load shaving and power transient buffering. During the CC interval, the dc-dc regulator provides a constant current into the supercap, while the voltage freely increases. Thus, the CC loop maintains the current at a constant reference value until the voltage reaches the selected CV threshold. At this point, the supercap voltage remains constant, corresponding to the maximum charge value, while the current reduces to zero.

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In this way, both the CC and CV control loops of the dc-dc regulator act on the system to fulfill the charging objective. Providing optimal charging speed, accuracy and efficiency, the regulator should also ensure a seamless transition between CC and CV modes and thus achieve reliable charging performance.



Fig. 2. Typical CC-CV charging profile of a supercap where the mode transition from CC to CV depends on the regulation voltage, V_{REG} .

The charging profile for a Li-ion battery is similar to that for a supercap, but includes trickle charge and precharge phases before the fast-charge CC phase. In addition, the battery charging process ends when the battery current tapers to a minimum or terminal value in the CV phase, typically 3% of the CC current.

CC-CV Circuit Examples

Table 1 shows several discrete implementations using a shunt resistor for current sensing. Attaching a CC circuit can require the addition of discrete components for current sensing, thus increasing the overall size.

	CV-CC	CC-CV	Dual loop		
Simplified schematic	Rs Vour U1 Current sense amp R1 C1 FB R2 VREF	Vour Rs Iour FB R2 R3	Vour R _{FB1} Voltage R _{FB2} Voltage Voltage Voltage Voltage Voltage Voltage Voltage Voltage		
Regulation	Vout	I _{OUT}	V _{OUT} or I _{OUT}		
Protection	I _{OUT}	Vout	V _{OUT} or I _{OUT}		
IOUT accuracy	5% to 10%	10% to 15%	5%		
Vout accuracy	1% (internal reference)	5% to 10%	1% (internal reference)		
Drawback	Slow current protection	Slow voltage protection	Oscillation between the loops		

Table 1. Discrete solutions for CC-CV that interface to the feedback (FB) node of a conventional dc-dc regulator.

In general, the circuits in Table 1 add size and cost to the implementation and yield unsatisfactory results, particularly if your design requires accurate current regulation. High-side sensing^[6] is generally preferable, as © 2025 How2Power. All rights reserved. Page 2 of 8



placing a shunt on the low side breaks the ground return plane. Moreover, low-side sensing causes an offset in the CV regulation, as the controller is typically referenced at power ground to drive the power switches (and not referenced to the load side of the shunt).

While there are devices that co-package the shunt and current-sense amplifier^[7], the emphasis in the following sections is on minimizing external component count by availing of the current sensing that already exists within the dc-dc regulator for current-mode control.

Enhanced Dual-Loop CC-CV Architecture

Fig. 3 shows a dc-dc regulator circuit using the LM5190-Q1 buck controller with integrated CC-CV functionality^[8] from Texas Instruments (TI). The schematic includes a supercap load modeled as an RC circuit, where R_{SC} is the equivalent series resistance and C_{SC} is the equivalent capacitance, representing the power loss and the energy storage effect during the charging process, respectively. A system microcontroller (MCU) can manage the state of charge and dynamically adjust the CV and CC regulation targets to ensure a successful charging process.



Fig. 3. Schematic of a CC-CV regulator powering a supercap load.

Rs in Fig. 3 designates the shunt for current sensing, used for both peak current-mode control and CC regulation. Clearly, this obviates the need for the current-sensing element shown in the circuits of Table 1. Inductor dc resistance (DCR) current sensing is also possible, not only to avoid the power loss, size and cost related to the shunt, but also to maximize the thermal connection from the buck inductor to the V_{OUT} copper planes for increased heat spreading. This makes it feasible to implement CC-CV regulation without using a shunt or discrete current-sense element.

As shown by the detailed structural diagrams for the CV and CC loop paths in Fig. 4, the proposed IC implementation is unique in that it selects the minimum of the currents from the transconductance error amplifiers in the CV and CC loops. Highlighted in red in Fig. 4, the minimum function block "IMIN selector" performs this function by selecting whichever error current is lower, apropos the loop that should be regulating at that time.



For example, the CC loop takes control when the IMIN selector directs the current from the current-loop error amplifier. The selected error current flows in a shared type-II compensation network, the resultant COMP voltage then becoming the reference command of the inner current loop of the peak current-mode architecture. You can design the small-signal dynamics of the CV and CC loops to be almost identical, with only one error amplifier active at a given time, thus minimizing loop interactions and yielding a seamless handoff from CV regulation to CC and vice versa.



Fig. 4. Functional diagram of the CC-CV regulator highlighting the CV loop (a) and the CC loop (b). The CC loop requires only two additional external components.

As highlighted in Fig. 4b, the IMON/ILIM pin acts as a monitor of the average inductor current and a currentlimit setting. IMON sources a current proportional to the voltage drop across the shunt, R_s . The CC loop starts to regulate the current when the IMON voltage reaches the current-loop error amplifier reference of 1 V.

Meanwhile, ISET is another noninverting input to the current-loop error amplifier, facilitating dynamic, on-thefly changes of the CC regulation setpoint without manipulation of the IMON/ILIM signal. The CC circuit requires only two additional external components: RIMON to program the CC regulation setpoint and CIMON to optimize the stability and transient response of the CC loop.

Design Expressions For The CC Loop

Based on the circuit of Fig. 4b, select the IMON pin resistance using equation 1 for a given CC setpoint:

$$R_{\rm IMON} = \frac{V_{\rm REFI}}{g_{\rm mIMON} I_{\rm OUT-CC} R_{\rm S} + i_{\rm OFFSET}}$$
(1)

where $V_{REFI} = 1 V$, $g_{mIMON} = 2 mS$ and $i_{OFFSET} = 25 \mu A$.

Equation 2 derives the output current from an IMON pin voltage reading as

$$I_{OUT} = \frac{\left(V_{IMON}/R_{IMON}\right) - i_{OFFSET}}{g_{mIMON}R_{S}}$$
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Finally, equation 3 defines the ISET pin voltage to adaptively adjust the CC setpoint, IOUT-CC (adj), as

$$V_{ISET} = \left(g_{mIMON}I_{OUT-CC(adj)}R_{S} + i_{OFFSET}\right)R_{IMON}$$
(3)

Design Example

Table 2 specifies the circuit operating conditions, power-stage component values and control circuit parameters of a design using the LM5190-Q1 controller operating at a switching frequency of 400 kHz. The load in this example requires CV and CC regulation setpoints of 12 V and 8 A, respectively. When considering the voltage derating of capacitors with ceramic dielectric, four 22- μ F, 25-V, X7R, 1210 output capacitors derate to a total effective value of 32 μ F at 12 Vdc.

Power-stage parameters				Buck controller parameters			
VIN (nom)	48 V	Lo	6.8 µH	Rs	5 mΩ	gmEA-V	1 mS
Vout-cv	12 V	Rdcr	12 mΩ	Gs	10	g mEA-I	1 mS
Iout-cc	8 A	Соит	32 µF	Se	180 mV/µs	REAout	250 MΩ
Fsw	400 kHz	Resr	1 mΩ	g mIMON	2 mS	Cbw	25 pF

Table 2. Power-stage and controller parameters for a CC-CV buck regulator design.

Selecting standard E96 resistor values of 93.1 k Ω and 6.65 k Ω for the feedback divider yields a CV voltage setpoint of exactly 12 V, calculated in equation 5:

$$V_{OUT} = V_{REFV} \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) = 0.8V \left(1 + \frac{93.1k\Omega}{6.65\,k\Omega} \right) = 12\,V$$
(5)

Using equation 1, you can find a suitable value for R_{IMON} as

$$R_{\rm IMON} = \frac{V_{\rm REFI}}{g_{\rm mIMON}I_{\rm OUT-CC}R_{\rm S} + i_{\rm OFFSET}} = \frac{1V}{2\,{\rm mS} \times 8A \times 5{\rm m}\Omega + 25\,\mu{\rm A}} = 9.53\,{\rm k}\Omega \tag{6}$$

Choose C_{IMON} as 4.7 nF to place the IMON pole coincident with the load zero in the CC loop—the next installment in this series will extensively detail the reasoning behind this choice.

Circuit Simulation

Fig. 5 presents a SIMPLIS simulation schematic using a CC-CV regulator configuration defined by the power-stage and controller parameters from Table 2 and Fig. 4.

The element with reference designator X1 in Fig. 5 is the SIMPLIS clock edge trigger to locate the periodic operating point (POP) of the circuit before running the time-domain analyses. The POP works on the full nonlinear switching time-domain model of the circuit and enables subsequent transient simulations.





Fig. 5. SIMPLIS schematic of the proposed CC-CV architecture.

Fig. 6 shows the voltage and current waveforms when applying and removing a transient load of 6 Ω . Notably, the CC loop engages and regulates the average inductor current to 8 A once the IMON voltage reaches 1 V.



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Experimental Results

Fig. 7a shows the same CV-to-CC-to-CV load transient response measured with a corresponding hardware implementation^[9] and an electronic load set in constant-resistance mode. Even though the current slew rate is not as high as that in the simulated result of Fig. 6, the output current regulates to 8 A once the IMON voltage hits the 1-V reference. With the scope set to XY display mode and infinite persistence, Fig. 7b demonstrates a brickwall current-limiting characteristic.



Fig. 7. Measured load transient response (a) and brickwall current-limiting characteristic (b).

Summary

Numerous applications require the regulation of both output voltage and output current. Current-source type loads typically require the addition of a CC loop to a traditional dc-dc regulator with a CV loop. The primary objective of this article was to describe an integrated solution for a CC-CV buck regulator based on a buck controller IC with an enhanced dual-loop architecture that minimizes interaction of the CV and CC loops, thus achieving a clean transition from CV to CC and vice versa. Results from simulation and bench measurement validate the performance of the CC-CV regulator.

The next installment in this series will examine small-signal analysis and measurement of the dual-loop system in a CC-CV buck regulator.

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For further reading on current-mode control, see the "<u>How2Power Design Guide</u>," locate the Design Area category and select Control Methods.