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CS MANTECH Presents Latest Developments In Compound Semiconductor Manufacturing And Device Technology

CS MANTECH 2025, the International Conference on Compound Semiconductor Manufacturing Technology, will be held May 19-22 at the Hilton New Orleans Riverside. CSMANTECH is a not-for-profit organization whose focus is to provide a forum for members of the compound semiconductor community to exchange and discuss new ideas to better serve the public in general.

They accomplish this objective through the annual CS MANTECH conference, which is comprised of technical papers, talks, workshops, and manufacturer exhibits. The conference is open to anyone interested in the latest advances in compound semiconductor manufacturing and device technology. This article presents an overview of the CS MANTECH 2025 program and highlights some of the power semiconductor-related talks in the program.

Returning To The Big Easy

As Jansen Uyeda of Northrop Grumman and the technical program committee chair for CS MANTECH observes in his 2025 conference highlights, "This year marks the third time we are holding our conference in New Orleans, Louisiana (NOLA), a historic city internationally recognized for its vibrant and colorful culture and unmatched rich musical and culinary scene. We are excited to be back in NOLA and harness the energy of the 'Big Easy' to continue the long CS MANTECH tradition of providing you with an exceptional technical and social networking experience."

He continues, "Our Executive and Technical Program Committees have done an outstanding job over the past year to solicit and organize a program that addresses the latest developments in CS manufacturing and technologies… CS MANTECH 2025 kicks off with the CS MANTECH Workshop on Monday, May 19th. The theme for this year's workshop is 'Characterization and Measurement for Success in Compound Semiconductors,' providing fundamental understanding of the characterization and measurement techniques critical for high yield CS manufacturing."

"In parallel, the Reliability of Compound Semiconductors (ROCS) Workshop, will be held to offer attendees a forum to present the latest results on CS reliability. A unique aspect of ROCS is the collaborative discussions on the latest in CS reliability and how to overcome barriers for wider technology adoption and application," says Uyeda.

Monday's workshops are followed by the first social and networking event—the Exhibitor Reception at 6:00 PM in the Hilton New Orleans Riverside Churchill ballroom. Attendees can meet with customers, suppliers, and collaborators, while enjoying hors d'oeuvres and drinks.

A Program Rich With Plenaries, Technical Sessions, And Networking Opportunities

Uyeda's description of the first day of the conference offers some program highlights, but also a sense of how the conference is organized and the general flow of the daily conference schedule:

"The CS MANTECH technical conference starts on Tuesday, May 20th, beginning with the Opening and Awards Ceremonies, that will include the 2024 Best Paper awards, Sponsorship Recognition, and a Conference Overview. We will begin each day of the conference with a single-track Plenary session, followed by parallel track technical sessions. Our first Plenary Session to kick-off the conference features speakers Professor Grace Xing from Cornell University and Professor Steven DenBaars from the University of California Santa Barbara. Professor Xing will speak on "AlN and Ga_2O_3: Materials of the Future or Reality?" and Professor DenBaars will speak on "Recent Advances in III-Nitrides for MicroLED and Visible Laser Materials & Devices".

"Following the first plenary session, we will transition to parallel technical sessions on Power Devices, Lasers, Manufacturing Challenges & Innovations, RF Devices, and Advance Packaging & Integration. These sessions are composed of both invited and regular and student contributed talks. Invited speakers featured during the first day of technical sessions represent leaders and technologists from North Carolina State University, Kyocera LSD, Renesas, Fujitsu, and Nexperia," says Uyeda.

He continues, "Lunch will be provided in the Exhibits Hall (Churchill Ballroom), offering attendees additional opportunities to connect with existing and new suppliers. Following Tuesday's technical sessions, we will hold the Student Forum to provide an opportunity for students to explore career opportunities through networking with members of the CS community from industry, academia, and government."

"Finally, the much-anticipated CS MANTECH International Reception will be held to close the first day of conference," says Uyeda. Stay tuned for the announcement on the location of this reception.

On Wednesday, May 21st the conference continues with highlights such as a second plenary session, featuring Mike Holmes from the U.S. Defense Advanced Research Projects Agency (DARPA) speaking on the Next Generation Microelectronics Manufacturing (NGMM) project and Bertrand Parvais from IMEC, offering an overview of compound semiconductor work in Europe.

Parallel technical sessions follow the plenary and there will be two special topic sessions focused on the U.S. Microelectronics Commons (MEC). Day 2 concludes with a CS MANTECH MEC Hub Panel session followed by a CS MANTECH MEC hub networking event."

On Thursday, May 22nd, the third and final day of the conference, the last plenary session will feature Hui-Hsin (Anna) Tseng from TSMC, presenting an "Overview of TSMC's Green Manufacturing Initiative". The second plenary speaker will be announced soon. Parallel tracks follow the plenary session. The lunch break is scheduled as free time for attendees to explore New Orleans, but then the conference continues in the afternoon with additional talks.

Beyond the plenary talks, the program includes invited speakers, plus regular and student contributed papers and talks in all sessions. As Uyeda, says "These contributions are from academia, government, and industry, and make up the foundation of our CS MANTECH conference. Like previous CS MANTECH conferences, these papers bring cutting-edge concepts that are often our first look at things that will change our industry for years to come. This extends to our Poster Session, which will end the technical portion of the conference, and is a great opportunity to interact with the authors to gain valuable insights and build new relationships."

The conference concludes with a Capstone Talk from Gregg Harry of American University and the LIGO Scientific Collaboration on "Development of large area substrate transferred aluminum gallium arsenide coated mirrors for future gravitational wave detectors". After the capstone, there will be a closing ceremony where awards for Best Poster, Conference Feedback Drawing, and Conference Contest will be announced.

A list of conference sessions and other scheduled activities appears below in the Program At A Glance. This is followed by a selected list of power-semiconductor-related papers being presented at this year's conference.

For more on the conference agenda, see the Advanced Technical Program. Or for information on the exhibition, registration or other details, see the conference website.

Conference At A Glance

SUNDAY, May 18th

6:00 PM – 8:00 PM	**REGISTRATION** *Registration Desk (Level 1)*

MONDAY, May 19th

7:00 AM – 7:00 PM	**REGISTRATION** *Registration Desk (Level 1)*
7:00 AM – 8:00 AM	**BREAKFAST** *Grand Ballroom C (Level 1)*
7:50 AM – 5:40 PM	**CS MANTECH WORKSHOP** *Grand Ballroom A (Level 1)*
8:00 AM – 5:00 PM	**ROCS WORKSHOP** *Grand Ballroom B (Level 1)*
12:20 PM – 1:20 PM	**LUNCHEON FOR WORK-SHOPS** *Grand Ballroom C (Level 1)*
6:00 PM – 9:00 PM	**EXHIBITOR RECEPTION** *Churchill (Level 2)*

TUESDAY, May 20th

7:00 AM – 7:00 PM	**REGISTRATION** *Registration Desk (Level 1)*
7:00 AM – 8:00 AM	**BREAKFAST** *Churchill (Level 2)*
8:00 AM – 5:00 PM	**EXHIBIT HOURS** *Churchill (Level 2)*
8:00 AM – 8:30 AM	**OPENING CEREMONIES** *Grand Ballroom A & B (Level 1)*
8:30 AM – 10:00 AM	**SESSION 1: PLENARY I** *Grand Ballroom A & B (Level 1)*
10:00 AM – 10:30 AM	**BREAK** *Churchill (Level 2)*
10:30 AM – 12:00 PM	**SESSION 2A: POWER DEVICES I** *Grand Ballroom A (Level 1)*
10:30 AM – 12:00 PM	**SESSION 2B: LASERS** *Grand Ballroom B (Level 1)*

12:00 PM – 1:10 PM	**EXHIBITS LUNCH** *Churchill (Level 2)*
12:20 PM – 1:10 PM	**EXHIBITOR FORUM** *Location TBD*
1:10 PM – 3:00 PM	**SESSION 3A: POWER DEVICES II** *Grand Ballroom A (Level 1)*
1:10 PM – 3:00 PM	**SESSION 3B: MANUFACTURING CHALLENGES & INNOVATIONS** *Grand Ballroom B (Level 1)*
3:00 PM – 3:30 PM	**BREAK** *Churchill (Level 2)*
3:30 PM – 5:00 PM	**SESSION 4A: RF DEVICES** *Grand Ballroom A (Level 1)*
3:30 PM – 5:00 PM	**SESSION 4B: ADVANCED PACKAGING & INTEGRATION** *Grand Ballroom B (Level 1)*
5:00 PM – 6:00 PM	**STUDENT FORUM** *Chequers (Level 2)*
5:00 PM – 6:00 PM	**EXHIBITOR FORUM** *Location TBD*
6:00 PM – 10:00 PM	**INTERNATIONAL RECEPTION** *Location TBA*

WEDNESDAY, May 21st

7:00 AM – 7:00 PM	**REGISTRATION** *Registration Desk (Level 1)*
7:00 AM – 8:30 AM	**BREAKFAST** *Churchill (Level 2)*
7:00 AM – 8:30 AM	**WoMANTECH Connect** *Prince of Wales (Level 2)*
8:00 AM – 11:00 AM	**EXHIBIT HOURS** *Churchill (Level 2)*
8:30 AM – 10:00 AM	**SESSION 5: PLENARY II** *Grand Ballroom A & B (Level 1)*
10:00 AM – 10:30 AM	**BREAK** *Churchill (Level 2)*

10:30 AM – 12:00 PM	**SESSION 6A: HETEROGENEOUS INTEGRATION** *Grand Ballroom A (Level 1)*
10:30 AM – 12:00 PM	**SESSION 6B: OPTOELECTRONICS I** *Grand Ballroom B (Level 1)*
12:00 PM – 1:20 PM	**LUNCH BREAK**
1:20 PM – 3:00 PM	**SESSION 7A: SUBSTRATES & MATERIALS** *Grand Ballroom A (Level 1)*
1:20 PM – 3:00 PM	**SESSION 7B: U.S. MICROELECTRONICS COMMONS HUB SESSION 1** *Grand Ballroom B (Level 1)*
3:00 PM – 3:20 PM	**BREAK** *Outside Grand Ballroom A & B (Level 1)*
3:20 PM – 4:50 PM	**SESSION 8A: GALLIUM OXIDE** *Grand Ballroom A (Level 1)*
3:20 PM – 4:50 PM	**SESSION 8B: U.S. MICROELECTRONICS COMMONS HUB SESSION 2** *Grand Ballroom B (Level 1)*
5:00 PM – 6:00 PM	**CSM MICROELECTRONICS COMMONS HUB PANEL DISCUSSION** *Jefferson Ballroom (Level 3)*
6:00 PM – 7:00 PM	**CSM MICROELECTRONICS COMMONS HUB NETWORKING** *Jefferson Ballroom (Level 3)*

THURSDAY, May 22nd

7:00 AM – 11:00 AM	**REGISTRATION** *Registration Desk (Level 1)*
7:00 AM – 9:30 AM	**BREAKFAST** *Churchill B (Level 2)*
8:20 AM – 9:50 AM	**SESSION 9: PLENARY III** *Grand Ballroom A & B (Level 1)*
9:50 AM – 10:20 AM	**BREAK** *Outside Grand Ballroom A & B (Level 1)*

10:20 AM – 12:00 PM	**SESSION 10A: OPTOELECTRONICS II** *Grand Ballroom A (Level 1)*
10:20 AM – 12:00 PM	**SESSION 10B: YIELD IMPROVEMENTS IN CS MANUFACTURING** *Grand Ballroom B (Level 1)*
12:00 PM – 1:20 PM	**LUNCH ON YOUR OWN** *Lunch not provided*
1:20 PM – 3:00 PM	**SESSION 11A: OPTOELECTRONICS III** *Grand Ballroom A (Level 1)*
1:20 PM – 3:00 PM	**SESSION 11B: WAFER PROCESSING** *Grand Ballroom B (Level 1)*
3:00 PM – 4:00 PM	**POSTER SESSION** *Churchill B (Level 2)*
4:00 PM – 4:30 PM	**CAPSTONE TALK** *Churchill B (Level 2)*
4:30 PM – 5:30 PM	**CONFERENCE CLOSING** *Churchill B (Level 2)*

Power-Related Highlights From The CS MANTECH 2025 Program

Tuesday, May 20, 2025

Session 2A: Power Devices I

Chairs: Yoganand Saripalli, Texas Instruments and Dilip Risbud, Renesas Electronics

10:30 am — Invited Presentation
2A.1 "Realizing Practical Doping in AlN for Power Electronics," Roman Collazo, NC State University

11:00 am — Student Presentation
2A.2 "Vertical GaN Trench MOSFETs with HfO_2/Al_2O_3 Layered Gate Dielectric," E. Brusaterra, E. Bahat Treidel, P. Paul, I.Ostermay, F. Brunnerm and O.Hilt, Ferdinand-Braun-Institut (FBH), Berlin, Germany

11:20 am — 2A.3 "1700 V Breakdown Monolithic Bidirectional GaN/AlGaN MISHEMTs with a Thin Buffer Grown on SiC Substrate," F. Benkheilifa,[1] S. Leone,[1] R. Reiner,[1] M. Basler,[1] H. Czap,[1] D. Grieshaber,[1] L.Kirste,[1] Frank Bernhardt,[1] S.Moench, [1,2] and R. Quay [1,3]

1. Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany
2. Institute of Electrical Energy Conversion IEW, University of Stuttgart, Stuttgart, Germany
3. Department for Sustainable Systems Engineering, INATECH, University of Freiberg, Freiberg, Germany

11:40 am — Student Presentation
2A.4 "The Effect of Operating Temperatuire on the On-State Performance of Quasi-Vertical Gallium Nitride MOSFETs," J. Evans,[1] F. Monaghan,[1] R. Harper,[2] A. Withey,[3] C. Colombier,[4] M. Elwin,[1] and M. Jennings[1]

1. CISM, Swansea University, Swansea, United Kingdom
2. CSC, Pascal Cl, St. Mellons, Cardiff, United Kingdom

3. Vishay Newport, Newport, United Kingdom
4. CS Connected, Cardiff, United Kingdom

Session 3A: Power Devices II

Chairs: Shiva Rai, Applied Materials and Martin Huber, NexGen Wafer Systems

1:10 pm Invited Presentation
3A.1 "GaN HEMT and SiC Power MOSFETs for Hard Switching applications, a Long-Term Perspective," Marco Zuniga, Renesas Electronics, San Franscisco, Calif.

1:40 pm Student Presentation
3A.2 "Normally-Off N-Polar GaN/AlN Transistors with p-NiO Gate Stacks," C. Zhang,[1] Y. Yin,[1] I. Furuhashi,[2] M. Pristovsek,[2] M. Kuball,[1] and M.D. Smith[1]
1. Center for Device Thermography and Reliability, University of Bristol, Bristol, United Kingdom
2. Center for Innovative Research of Future Electronics, Institute for Material Science and Systems for Sustainability, Nagoya University, Nagoya, Japan

2:00 pm 3A.3 "Vertical GaN-on-Tugsten High Voltage pn-Diodes," E. Bahat Treidel,[1] E. Brusaterra,[1] L. Deriks,[2] S. Danylyuk,[2] E. Brandl,[3] J. Bravin,[3] F. Brunner,[1] and O. Hilt,[1]
1. Ferdinand-Braun-Institut (FBH), Berlin, Germany
2. Fraunhofer Institute for Laser Technology, Aachen, Germany
3. EV Group, St. Florian am Inn, Austria

2:20 pm Student Presentation
3A.4 "High Voltage Design Strategies for Gallium Oxide Power Devices," N. Edwards,[1] A.M. Muinz,[1] J. Evans,[1] J. Mitchell,[2] D. Goodwind,[1] E. Chikoidze,[3] A. Perez-Tomas,[4] M. Vellvehi,[4] F. Monaghan,[1] Owen Guy,[1] C.Fisher,[1] A. Huma,[2] C. Colombier,[5] and Mike Jennings[1]
1. CISM, Swansea University, Swansea, United Kingdom
2. KLA (SPTS Division), Newport, United Kingdom
3. GeMAC, Versailles, France
4. IMB-CNM, Barcelona, Spain
5. CSconnected, Cardiff, United Kingdom

2:40 pm 3A.5 "1000-Hour HTRB Test in 1200 V Lateral HEMTs with Engineered P-GaN Gate," S. Kumar,[1] M. Borga,[1] D. Cingu,[1] K. Geens,[1] A. Vohra,[1] B. Bakeroot,[1,2] N. Posthuma,[1] and S. Decoutere,[1]
1. imec, Leuven, Belgium
2. CMST. Imec and Ghent University, Ghent, Belgium

Session 4A: RF Devices
4:20 pm 4A.3 "Dual-gate RF HEMT based on P-GaN/AlGaN on Si Technology For Future X-band On-chip RF and Power Electronics," A. Eblabla, W. Sampson, A.M. Bhat, A. Collier, E. Yadollahifarsi, and K.Elgaid, Centre for High Frequency Engineering, Cardiff University, Cardiff, United Kingdom

Wednesday, May 21, 2025

Session 7A: Substrates & Materials

Chairs: Wei Zhang, AXT and Yohei Otoki, Sumitomo Chemical

2:20 pm 7A.4 "SmartSiC 150 & 200 mm Engineered substrate: Solving SiC Power Devices Bipolar Degradation," E. Guiot,[1] F. Allibert,[1] J. Leib,[2] T. Becker,[2] R. Bagchi,[2] G. Gelineau,[3] S. Barbet,[3] R. Lavielle,[3] P. Godignon,[3] and W. Scharzenbach,[1]
1. SOITEC, Bernin, France
2. Fraunhofer IISB, Erlangen, Germany
3. Univ. Grenoble Alpes, CEA, Leti, Grenoble, France

Session 8A: Gallium Oxide

Chairs: James Spencer Lundh, U.S. Naval Research Lab and Peter Ersland, MACOM

3:50 PM 8A.2 "kV-Class β-Ga2O3 Trench Schottky Barrier Diodes: Double Drift Layer Design and Breakdown Analysis," V.S. Charan, A.K. Bhat, H. Huang, M.D. Smith, J.W. Pomeroy, and M. Kuball, Center for Device Thermography and Reliability, HH Wills Physics Laboratory, University of Bristol, Bristol, United Kingdom

4:10 pm Student Presentation
8A.3 "Vertical Schottky Barrier Diodes with Optical Floating Zone Growth of β-Ga_2O_3 Single Crystals and Electrical Defect Study," V.L. Ananthu Vijayan,[1,2] V.S. Charan,[2] C.A. Dawe,[3] V.P. Markevich,[3] M.P. Halsall,[3] A.R. Peaker,[3] S.M. Babu,[1] and M. Kuball,[2]
1. Crystal Growth Centre, Anna University, Chennai, India
2. Center for Device Thermography and Reliability, HH Wills Physics Laboratory, University of Bristol, Bristol, United Kingdom
3. Photon Science Institute and Department of Electrical and Electronic Engineering, The University of Manchester, Manchester, United Kingdom

4:30 pm Student Presentation
8A.4 "Gallium Oxide Trench Schottky Barrier Diodes with Field Plate Edge-Termination," A.K. Bhat, V.S. Charan, M. Smith and M. Kuball, University of Bristol, Bristol, United Kingdom

Thursday, May 22, 2025

Session 10B: Yield Improvement In CS Manufacturing

Chairs: Mario Faria, Tignis and Steve Mahon, Feldman Engineering

10:20 AM 10B.1 "Mapping Defects in SiC Wafers Using a Multi-Channel Convolutional Neural Network," J.C. Gallagher, N.A. Mahadik, R.E. Stahlbush, K.D. Hobart, and M.A. Mastro, U.S. Naval Research Laboratory, Washington, D.C.

11:00 AM 10B.3 "Determination of 4H-SiC Drift Layer Quality with Mercury Probe Capacitance-Voltage (CV) and Current-Voltage (IV) Measurements," M.G. Coco Jr.,[1] F. Ramos,[1] B. Kim,[1] S.M. Lee,[1] D. Hanser,[1] R.J. Hillard,[2] S. Frey,[2] T. MacRaea,[2] B. Vigh,[3] A. Marton,[3] G. Zsakai,[3] J. Janisco-Csathy,[3] and P. Horvath[3]
1. Veeco Instruments, Somerset, N.J.
2. Semilab U.S.A., Billerica, Mass.
3. Semilab, Budapest, Hungary