Protect And Enhance High-Power Designs With Integrated Solid-State Isolators

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In high-power designs, an isolation technique with several integrated features can mean the difference between a product that meets and even exceeds customer expectations and one that generates numerous customer complaints. To achieve this isolation, an integrated solid-state isolator (SSI) based on coreless transformer (CT) galvanic isolation provides many design benefits.

Unlike optical-based solid-state relays (SSRs), an integrated SSI driver can provide the required isolation and energy transfer to ensure proper operation and extended life for high-power systems as well as several integrated protection features. The integrated features include a dynamic Miller clamp (DMC), overcurrent and overtemperature protection (OTP), undervoltage lockout protection, fast turn-on and more.

These coreless transformer-based isolators enable on and off control, acting like a relay switch without requiring a secondary-side, isolated power supply. Combined with MOSFETs and IGBTs, Infineon's SSI family enables cost-effective, reliable, and low-power solid-state relays capable of controlling loads in excess of 1,000 V and 100 A for a variety of applications. This includes battery management systems, power supplies, power transmission and distribution, programmable logic controllers, industrial automation, and robotics as well as smart building applications such as HVAC controllers and smart thermostats.

In this article, we'll describe the features and characteristics of Infineon's integrated SSI drivers and then present a series of examples demonstrating how these devices can be combined with power MOSFETs and other supporting components to replace conventional DIN-rail and panel-mount SSRs. The calculations and data required for selection of MOSFETs, buffer capacitor, current-sense shunt resistor and RC filter components, overvoltage protection device (TVS or MOV), coupling capacitor, and input resistor are presented as is the calculation for leakage current.

Component lists are presented for the resulting SSI plus power MOSFETs solutions and these are compared against the conventional SSRs they are meant to replace. These comparisons encompass electrical operating parameters such as voltage and current, voltage drop, protection features, leakage current, minimum load current, dV/dt and turn-on and -off response times.

Energy Transfer Through Coreless Transformer Isolation

The main design feature of the integrated SSI family is a coreless transformer which enables power transfer across a galvanic isolation barrier of up to 10 mW. This eliminates the need for an isolated power supply for the switch reducing the bill of material (BOM) volume, component count, and cost. It also provides a fast turn-on and -off feature (≤1 µs) to ensure that the safe operating area (SOA) of the switch is adhered to. All variants meet UL1577 for 5700-Vrms isolation and IEC 60747-17 for 8000-Vpeak isolation. With an output voltage up to 18 V, an Infineon SSI provides an ideal solution for driving a broad range of MOSFETs and IGBTs (Fig. 1).

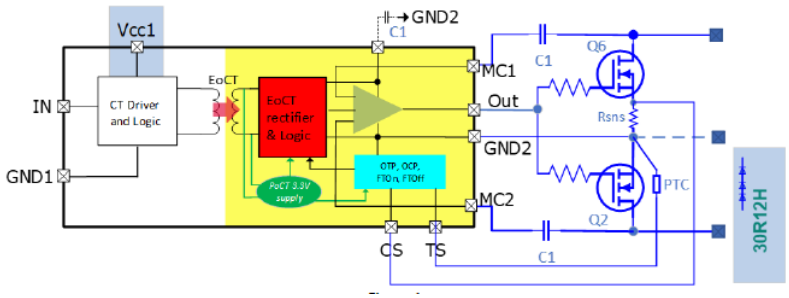


Fig. 1. Highly integrated solid-state isolators, such as the iSSI30R11H/12H, easily drive MOSFETs or IGBTs, and do not require an isolated bias supply.

Integrated Protection

Depending on the application's need and product variant selected, the iSSIx0RxxH portfolio offers a dynamic Miller clamp, and undervoltage lockout (latch-off) protection as well as overcurrent protection (OCP) and overtemperature protection (OTP). The latter feature can be triggered either via an external positive temperature coefficient (PTC) thermistor/resistor or a MOSFET's integrated direct temperature sensor (iSSI30R12H).

In the event of a failure (overcurrent or overtemperature), the SSI triggers a latch off. Once triggered, the protection reacts quickly, turning off in less than 1 µs. With this capability, it is able to support the AC-15 system tests required for electromechanical relays according to the IEC 60947-5-1 under appropriate operating conditions.

Overcurrent Protection

With solid-state relays, a common problem is addressing fast overcurrent or short circuit events in the range of 20 A/µs up to 100 A/µs. Isolation issues often result in a short circuit with an extremely high current level that is defined by the power source's impedance and cabling resistance.

Fig. 2 shows a circuit for implementing the overcurrent protection capability of the iSSIx0R1xH. The shunt resistor (R_{Sh}) and its inherent stray inductance (L_{Sh}) generate a voltage drop that is monitored by the current sense comparator. Noise on the grid needs to be filtered out from the shunt signal, so an external filter (C_F and R_F) complements the integrated filter. When the comparator triggers, it activates the fast turn-off and latches the fault leaving the system in a safe state.

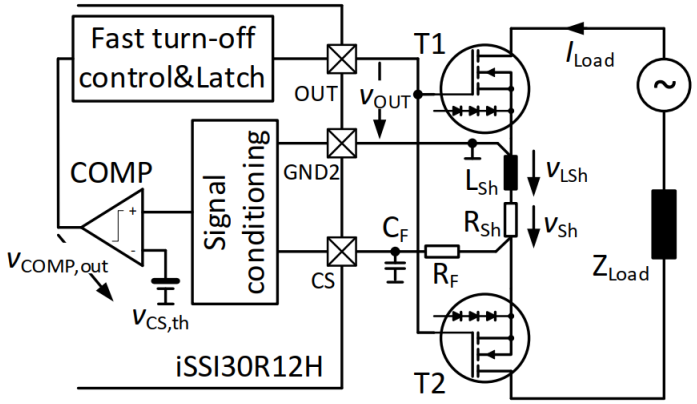


Fig. 2. Circuitry to implement overcurrent protection using an iSSI30R12H isolator driver.

Overtemperature Protection

Another issue when operating solid-sate relays is the slow overload events that heat up the switches and the current sensor (shunt). Increased load current and insufficient thermal management can additionally shift the overall temperature above the power transistor's thermal limits.

Fig. 3 shows an example of the overtemperature protection using an iSSI30R12H. The Infineon SSI turns off two IPT60T022S7 MOSFETs with integrated temperature sensors configured in a common-source mode. The sensing MOSFET heats up from the load current until the sensor voltage decreases below the comparator trigger threshold. As a result, the Infineon SSI's output is turned off within 500 ns. This means that the switched transistors do not violate their safe operating area.

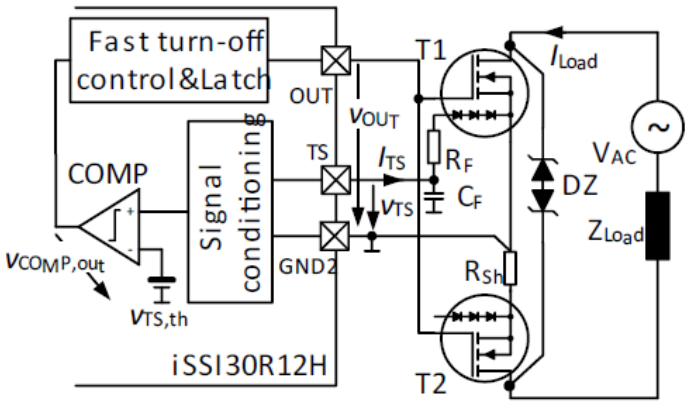


Fig. 3. The iSSI30R12H's overtemperature protection triggers within 500 ns.

Dynamic Miller Clamping Protection

Some products in Infineon's SSI family also have an integrated dynamic Miller clamp to protect against spurious switching due to surge voltages and fast electric transients as well as the dv/dt of the line voltage. The dv/dt applied by the connected ac voltage creates capacitive displacement currents through the parasitic capacitances of a power transistor. This can lead to parasitic turn-on of the power switch by increasing the voltage at its gate node during its "off" state. The dynamic Miller clamping feature ensures that the power switch remains safely in the off state.

Satisfying UL, IEC And Other Requirements

All products in the solid-state isolator family are designed to meet essential UL and IEC specifications. Depending on the desired features (see Table 1), SSI products are available in either a full featured DSO 16-pin (PG-DSO-16-33) or an optimized 8-pin (PG-DSO-8-66) package. Both packages are 300-mil wide-body designs with high creepage and clearance to meet UL 1577 and reinforced isolation to satisfy IEC 60747-17 requirements (planned). They are also qualified for industrial applications meeting relevant tests of JEDEC47/20/22.

Matched with the appropriate power switches, the isolator drivers enable designs with a much lower on-resistance compared to optically driven/isolated solid-state solutions. This translates to longer lifespans and lower cost of ownership in system designs. As with all solid-state isolators, the devices also offer superior performance compared to electromagnetic relays, including 40% lower turn-on power loss and increased reliability due to the elimination of moving or degrading parts.

Table 1. Design options within the Infineon SSI family.

Sales number	VIN range	VCC1 range	IOUT pk	Features	Package
iSSI20R02H	TTL/CMOS	2.85 V to 3.5 V	175 µA	OTP or OCP, DMC	PG-DSO-8-66
iSSI20R03H			175 µA	OTP and OCP	PG-DSO-8-66
iSSI20R11H			400 mA	Fast Ton, OTP or OCP	PG-DSO-8-66
iSSI30R11H			400 mA	Fast Ton, OTP and OCP, DMC	PG-DSO-16-33
iSSI30R12H			400 mA	Fast Ton, OTP (CoolMOS Tsense) and OCP, 2x DMC	PG-DSO-16-33

In summary, the integrated capabilities of an iSSIx0RxxH include:

- No isolated bias supply requirement
- Galvanic isolation up to 5.7 kV rms
- Minimization of heatsinking requirements
- Widest range of controllable switches
- Large application platforms
- Elimination of spurious switch turn-on
- Compliance with UL 1577 and IEC 60747-17 requirements

Isolate And Protect

The right choice of isolation can mean the difference between design success and failure, and a shorter vs. longer design-in process. An isolation technique with numerous integrated features can provide this differentiation, thereby addressing the high voltage circuitry's needs in multiple market segments and end applications.

Application Examples

The new Infineon SSIs bring several advantages in many industrial applications. We will show here a couple of examples in power distribution, where nowadays SSRs based on TRIACs or SCRs are used (Figs. 4 and 5).

In industrial environments there are large cabinets housing all power distribution devices. Between them you can find circuit breakers, power metering devices, fuses and solid-state relays (SSRs).

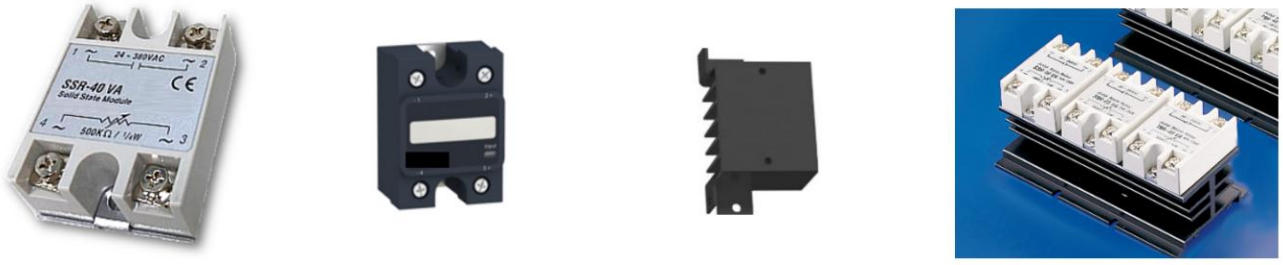
These SSRs accomplish the task to power up lighting lines, ventilation groups, air conditioners, refrigeration lines, etc. Their advantage versus standard electromechanical relays (EMRs) lies in the longer reliability and remote controllability of these devices.

On the other hand, these SSRs suffer from a few problems due to the nature of their implementation using controlled diodes:

- High-power dissipation
- Large heat sink and space required
- No protections, requiring external fuse or circuit breakers
- No easy dc operation (complex thyristor forced commutation technique).
- No fault monitoring

(a) *(b)* *(c)* *(d)*

Fig. 4. DIN rail-mount SSR (a, b and c) and a DIN rail fuse socket (d).



(a) *(b)* *(c)* *(d)*

Fig. 5. Panel mount SSRs (a and b), a heat sink example (c) and a possible mounting solution (d).

Let's reference some examples now, by using commercially available devices and comparing with a solution designed around combinations of an Infineon SSI with two or more MOSFETs.

An SSR For DIN Rail Mount

We start by comparing an SSR for DIN rail mount against an SSI solution. The SSR's main characteristics follow in Table 2.

By reading this data, we understand that this device must dissipate around 8 W when working at its maximum power ratings and doesn't have any protection embedded.

This means that a good portion of its package size is occupied by the heat sink that, in a closed cabinet as usually is the case for DIN-rail mounting devices, may not be able to dissipate correctly. Consequently, excessive heat may shorten the SSR's life considerably.

Now, let's compare the SSR described above with a possible solution using the novel Infineon SSI component. We'll start by creating the BOM.

Table 2. Commercial DIN-rail SSR characteristics.

Specification	Single-phase SSR, 6 A, DIN rail
Type	Random voltage switching SCR output (as pictured in Fig. 4a)
Operating voltage and current	4- to 32-Vdc input 24- to 280-Vac output, 6 A
Maximum voltage drop	<1.3 V (on state) P_{diss} max =1.3 V x 6 A = 7.8 W
Maximum I^2T for fusing	410 A^2.s for 8.33 ms at 60 Hz 375 A^2.s for 8.33 ms at 60 Hz No protections
Maximum leakage current	0.1 mA (off state)
Load current	0.15 A to 6 A
dV/dt	500 V/µs off state at maximum voltage
Response time	0.5 cycle (turn off) 0.1 ms (turn on)

MOSFET Selection

We are targeting an ac application, therefore we need to select a couple of CoolMOS FETs as shown in Fig. 1. The table below shows the available devices from Infineon.

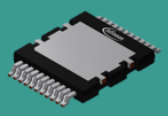
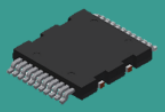
Our target is to reduce the power dissipation on the SSR, while in on-state by a factor of 3 or more at full output current. Therefore, we can calculate the following $R_{DS(ON)}$:

$$R_{DS(ON)} = \frac{Pdiss}{3 * 2 * Imax^2} = \frac{7.8}{3 * 2 * 6^2} = 36\ m\Omega$$

where Pdiss is the max power dissipation and Imax is the max output current of the reference SSR.

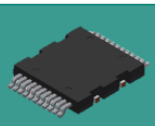
Now, looking at Table 3, we can select the IPT60T022S7 power MOSFET in the TOOL package, with its 22-mΩ resistance at 25°C, in consideration that its $R_{DS(ON)}$ on will double at the maximum operating temperature of 150°C.

Table 3. 600-V CoolMOS S7 and CM8 high-voltage MOSFETs.

$R_{DS(on,max)}$ [mΩ]	 TO220	 TOLL	 QDPAK TSC	 QDPAK BSC	TO247-3	TO247-4
65	IPP60R065S7	IPT60R065S7	IPDQ60R065S7			
37-40	IPP60R040S7/ IPP60R037CM8	IPT60R040S7/ IPT60R037CM8	IPDQ60R040S7/ IPDQ60R037CM8	IPQC60R040S7	IPW60R037CM8	IPZA60R037CM8
22	IPP60R022S7	IPT60R022S7	IPDQ60R022S7	-		
16-17	IPP60R016CM8	IPT60R016CM8	IPDQ60R017S7/ IPDQ60R016CM8	IPQC60R017S7	IPW60R016CM8	IPZA60R037CM8
7-10			IPDQ60R010S7/ IPDQ60R007CM8	IPQC60R010S7		

By selecting a CoolMOS of the T-series, with integrated temperature sensors shown in Table 4, we can more precisely and quickly track the temperature of its die and effectively protect the device. As a result, the risk of having to replace the SSR because of an overload is reduced to a minimum. For this reason, the selected device for this example is the iSSI30R12H, shown in Table 1 and Fig. 1, with independent thermal and current sense input pins.

Table 4. 600-V CoolMOS S7T high-voltage MOSFETs with integrated temperature sensors.

$R_{DS(on,max)}$ [mΩ]	 TOLL PG-HSOF-8	 QDPAK TSC PG-HDSOP-22-1	 QDPAK BSC PG-HDSOP-22-101
65	IPT60T065S7		
40	IPT60T040S7		
22	IPT60T022S7	IPDQ60T022S7	IPQC60T022S7
17		IPDQ60T017S7	IPQC60T017S7
10		IPDQ60T010S7	IPQC60T010S7

Minimum Buffer Capacitance Cbuf_min

The minimum capacitance Cbuf_min to be connected to terminal BUF is calculated from the following formula:

$$Cbuf\_\min = 1.2 * \frac{Qm1 + Qm2}{Vbuf_{th\_min} - Vg\_min}$$

with Qm1 and Qm2 being the related MOSFETs' gate charges at the desired turn-on gate voltage (Vg_min), $Vbuf_{th\_min}$ being the minimum fast turn-on comparator threshold voltage, from the iSSI30R12H datasheet and

Vg_min the required minimum gate-source voltage of the MOSFETs at turn-on. The safety factor of 1.2 covers the gate charge tolerance.

The Qm1 and Qm2 values need a deeper discussion: in ac operation with MOSFETs in the off-state, one of the two devices will always be working as a synchronous rectifier, while the other one will be open. For this reason, the gate charge at turn-on of the MOSFET in body diode conduction will not see the Miller plateau and will be lower. Therefore, the Qm values are different and can be estimated from the device characteristic in the datasheet (Fig. 6).

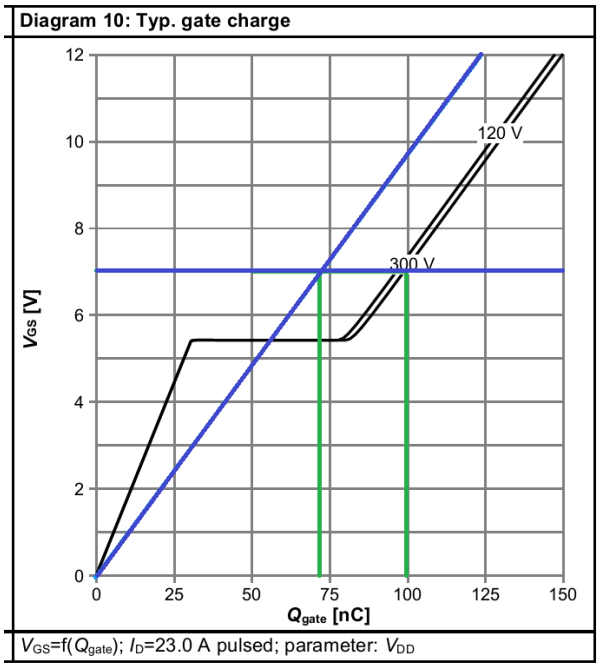


Fig. 6. Extrapolation of Qm1 and Qm2 from the gate-charge characteristic.

For our design using iSSI30R12H and IPT60T022S7 we then have the following:

- Qm1 = 100 nC (CoolMOS open)
- Qm2 = 70 nC (CoolMOS in body-diode conduction)
- $Vbuf_{th\_min}$ = 10 V (from iSSI30R12H datasheet)
- Vg_min = 7 V (required minimum turn-on gate-source voltage)

In our case this yields:

$$Cbuf = 1.2 * \frac{100\,nC + 70\,nC}{10\,V - 7\,V} = 68\,nF$$

Leakage Current In Off-State

When the SSR is in the off-state, since no airgap is present there will be some leakage current flowing though the MOSFETs. This current comes from two effects—zero-gate-voltage drain current (I_{DSS}) and output capacitance, energy related ($C_{o(er)}$).

The second parameter is defined as follows: $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 300 V. For our IPT60T022S7 CoolMOS, the values from the datasheet are the following:

I_{DSS} = 50 µA (typ) at V_{DS} = 600 V, V_{GS} = 0 V, T_j = 150°C

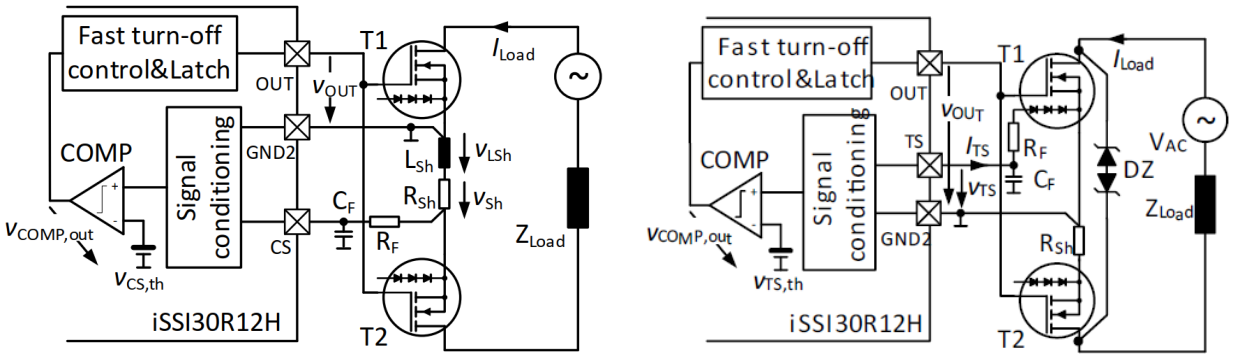
$C_{o(er)}$ = 303 pF at V_{GS} = 0 V, V_{DS} = 0 to 300 V

Looking once again at the application diagram in Figs. 2 and 3 (repeated below), we notice that, when the MOSFETs are off, at every semi sinusoid of the ac line, one device is conducting via its body diode while the other sees the full 0-V to 320-V voltage variation. By calculating the current flowing through this parasitic equivalent output capacitance, for a 50-Hz ac power line, we obtain

$$I_{Co(er)} = \frac{320}{\frac{1}{2 * \pi * 50 * 303\ pF}} \cong 30.5\ uA$$

Then, considering the two effects, the total leakage current from our SSR in off-state is calculated to be at worst case:

$$Ileak_{25} = I_{DSS} + I_{Co(er)} = 5\ uA + 30.5\ uA \cong 35.5\ uA$$



Figs. 2 and 3 (again). Circuitry to implement overcurrent protection using an iSSI30R12H isolator driver.(left) The iSSI30R12H's overtemperature protection triggers within 500 ns (right).

Protection: Short Circuit

Now we can add extra value to our SSR built with MOSFETs instead of SCRs or TRIACs.

An SCR or a TRIAC in conduction will stay in that condition naturally until the current decreases below the minimum holding value and there is no way to open the circuit in a short-circuit condition.

For this reason, often this type of SSR requires a fuse in series, as show in Fig. 4d, though fuses are very slow to react (tens of milliseconds), take an extra module (18-mm) DIN rail space and need to be replaced after intervention. In many cases, SSRs are supplied by a single circuit breaker, to reduce the space and cost of the solution. However, this means that, when the circuit breaker triggers to protect one of the SSRs with short-circuited load, all other SSRs and their supplied lines will be turned off.

By using the Infineon SSI, driving a couple of CoolMOS FETs, this problem can be easily overcome, saving space, money and more effectively protecting the power line circuits and loads.

A less evident effect is also related to the energy accumulated in the cables during short circuit protection. If a fuse or a circuit breaker takes tens of milliseconds to trigger, during this time big energy is accumulated in the cables, proportional to their parasitic inductance, per the following formula:

$$E_L = \frac{1}{2} Lp * Isc^2$$

where L_p is the parasitic inductance value of the cables and I_{sc} is the short circuit current at the time of circuit interruption. This energy will then be generating a high-voltage spike across the opening device, potentially damaging other parts of the circuit or the SSR itself.

Now, how do we protect it with the Infineon SSI?

Let's first decide the triggering level for our 6-A SSR: the voltage threshold of the CS input of the Infineon SSI is set at 200 mV, this to provide good precision and enough margin not to trigger for simple temporary overloads as capacitive inrush currents.

We'd like to set the overcurrent intervention level at about 10 times the rated current. Considering that the protection is very fast to react, we must run our calculation considering the peak voltage value of the current sinusoid, therefore:

$$Rsh = \frac{200\,mV}{10 * \sqrt{2} * 6\,A} \cong 2.36\,m\Omega => 2.4\,m\Omega$$

This means that in normal operation the total resistance at 150°C and the voltage dropout of our SSR using 2x IPT60T022S7 and a shunt resistor, will be:

$$Rssr = 2 * 2 * 22\,m\Omega + 2.4\,m\Omega \cong 90.4\,m\Omega Vssr = \ 90.4\,m\Omega * 6\,A\ \cong 542\,mV$$

which is 58% lower than the 1.3 V of the device using SCRs. That will ensure a much smaller heat sink with less than one-half the weight and size.

To properly protect without false triggering for noise, as mentioned in the section on overcurrent protection and shown in Fig. 2, we need to add a low-pass filter on the CS input. Our lab tests indicate that a good filter value for most applications, ranges from 500 kHz to a few megahertz. By considering an intermediate point we can choose a filter pole frequency of about 1.5 MHz, leading to these selections:

$$Rf_{oc} = 100\Omega,\ Cf_{oc} = 1nF$$
$$Fp\_oc = \frac{1}{2 * \pi * Rf * Cf} \cong 1.59MHz$$

Thanks to this minimum filtering and to the strong pull-down current in protection, the expected turn-off time on protection will be

$$T_{OCprot} = \ t_{CS\_off} + \frac{Qg}{IIoff\_fast\_sat} = 1\ us + \frac{150\ nC}{488\ mA} = 1.48\ us$$

where, from datasheets and in worst case t_{CS_off} = 1 µs, Qg = 150 nC, and $I_{off\_fast\_sat}$ = 488 mA.

Protection: Overtemperature

Thanks to the Infineon iSSI30R12H SSI's built-in temperature protection the S7T CoolMOS can be monitored for temperature and efficiently protected. The driver sources a bias current of 50 µA needed for the readout of the integrated temperature sensor and detects the voltage dropout across the diodes stack, triggering at a typical threshold voltage of 1.095 V, which correlates to a max junction temperature of ≈155°C.

The integrated comparator includes a noise filter for safely detecting the sensor signal. However it is a good practice to complement this noise filter with an external RC filter, as shown in Fig. 3, of about the same transition frequency as the OCP filter. Therefore a good choice is again the following:

$$Rf_{ot} = 100\ \Omega,\ Cf_{ot} = 1\ nF$$
$$Fp_{ot} = \frac{1}{2 * \pi * Rf * Cf} = \frac{1}{2 * \pi * 100\ \Omega * 1\ nF} \cong 1.59\ MHz$$

TVS Or MOV Diode Dimensioning

A TVS diode or MOV must be added to protect the CoolMOS from clamping excessive energy in overvoltage, which could occur when the MOSFET opens suddenly to protect a short circuit situation. This added device is shown as DZ in Fig. 3. Its mounting should be very close to the power pins of the SSR and the drain of the

MOSFETs. The clamping device must be selected with diode breakdown voltage (V_{BR}) higher than the peak value of the SSR peak operating voltage and lower than the CoolMOS breakdown voltage (V_{BR_DSS}).

In our case, considering a maximum operating voltage of 280 Vac and bidirectional operation (ac), we can select a diode as follows:

$$Vpeak = 280\,Vac * \sqrt{2} \cong 396\,V$$

Therefore, a good selection is a TVS with a standoff operating voltage of 400 V and a clamping voltage somewhere between 450 V and 500 V.

Peak pulse power dissipation must be selected based on the design and environmental choices. However, usually values between 1500 W and 3000 kW are good selections, depending also on the space available on the PCB. A good option is, for example, the SMCJ400CA, with 1500-W peak power capability.

Miller Clamping Protection

Surge voltages and fast electric transients, such as when opening inductive loads, result in fast dv/dt across the opening switches that, through their parasitic capacitances, may lead to unwanted parasitic turn-on. The Miller clamping feature designed into the iSSI30R12H prevents this from occurring.

According to the iSSI30R12H datasheet we must limit the voltage on the MC pins to a max of 3.6 V and the input resistance at those points is 600 Ω max. As an initial assumption let's consider the fastest occurring dv/dt rates that may appear in an ac application, across the SSR pins, to be around 10 V/ns. Please note that this is about 1 million times faster than the relatively slow dv/dt of the line voltage, which turns out to be equal to w*Vmax = 320 V * 2*π * 50 Hz ≅ 100 V/ms, in 230-Vac grids.

Also note that one of the two switches in common-source configuration will always be conducting through its body diode. So at every moment only one of the two capacitors will be injecting current into the related MC pin.

Based on the information given in the iSSI30R12H datasheet, we can calculate the following:

$$I_{MC} = \frac{V_{MC}}{R_{MC}} = \frac{3.6\,V}{600\,\Omega} = 6\,mA$$

Therefore, the min coupling capacitor value for the MC pin can be derived from the following:

$$C_{MCmin} = \frac{I_{MC}}{dV_{max}/_{dt}} = \frac{6\,mA}{10\,V/_{ns}} = 0.6\,pF => 1\,pF$$

which we can round up to C_{MC} = 1 pF, considering that we may eventually add a clamping Zener DZ = 3.3 V between each MC pin and GND2, as shown in Fig. 7. However, this clamping Zener is often not needed considering the high current limit capability of 100 mA for short pulses (<1 µs) happening on those pins.

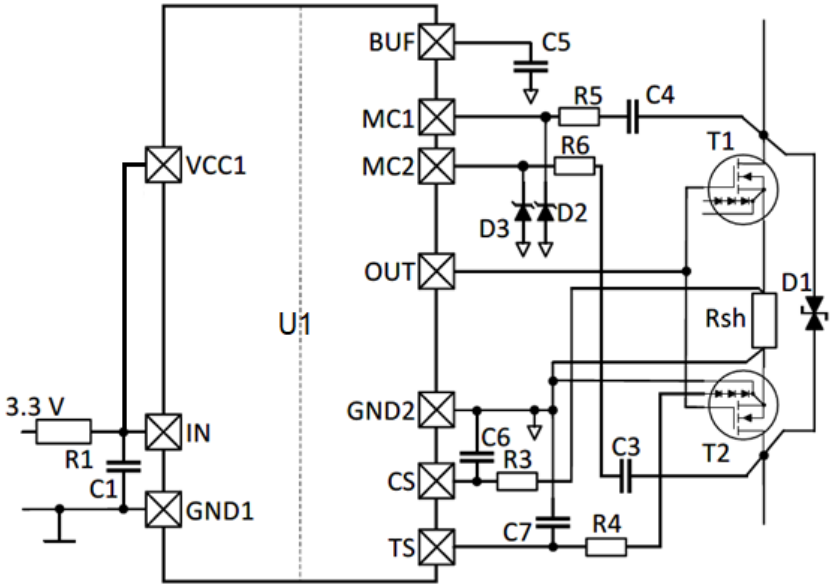


Fig.7. SSR application schematic.

Input Stage

The iSSI30R12H allows for separated Vcc1 (supply) and IN (input signal), making it possible to drive several devices in parallel from a microprocessor output operating at 3.3 V. In this case we need only a single input with wide range, therefore we can short Vcc1 and IN together. This way we will have a single input resistor to calculate based on the Vcc1 supply voltage of 3.3 V typ, which has an internal regulator clamping at 3.5 Vmax.

For an industrial SSR the common operating input voltage is usually between 12 V and 24 V, therefore we can calculate the drop-down resistor as follows:

$$Rin = \frac{V_{in-min} - Vcc1_{max}}{Iin} = \frac{12\ V - 3.5\ V}{16\ mA} = 531.25\ \Omega => 536\ \Omega\ (E48)$$

Now we must verify if the input power dissipation at $V_{in\text{-}max}$ is still within specifications, therefore:

$$Pin\_\max = \frac{V_{in-max} - Vcc1_{max}}{Rin} * Vcc1_{max} = \frac{24\ V - 3.5\ V}{536\ \Omega} * 3.5\ V \cong 134\ mW$$

From the datasheet, this is still well below the maximum limit of 200 mW at Ta = 85°C. However, it must be noted that in this condition the external resistor will dissipate

$$P_{Rin\_max} = \frac{(V_{in-max} - Vcc1_{max})^2}{Rin} = \frac{(24\ V - 3.5\ V)^2}{536} = 784\ mW$$

This is not so efficient and we have to consider a resistor of 1 W to 1.5 W for the supply input; however, in case of efficiency or thermal limitations a small dc-dc converter with a low-tolerance output voltage of 3.3 V can be used or a smaller input range may be selected.

The bypass capacitor can be derived directly from the datasheet operating parameters, which shows a max value of 4.7 nF. Therefore we can choose

$$Cin = 3.3\ nF$$

Component Summary And SSR Comparison

Now we have all the components for the output stage of the SSR DIN rail mount application, as per Table 5 and the schematic in Fig. 7, which is repeated below.

Table 5. Component summary for a 600-V, 6-A SSR.

Schematic reference	Calculation reference	Value	Comments
U1	U1	iSSI30R12H	Infineon SSI
T1, T2	IPT60T022S7	IPT60T022S7	Infineon CoolMOS T-series
Rsh	Rsh	2.4 mΩ	Shunt resistor
D1	TVS	SMCJ400CA	1500 W in SMC package
D2, D3	DZ	3.3 V	Diode zener 500 mW
R3, R4	Rf_{oc}, Rf_{ot}	100 W	SMD resistor
R5, R6	none	0 W	Not used
C3, C4	C_{MC}	1 pF	2-kV SMD capacitor
C5	Cbuf	68 nF	50-V SMD capacitor
C6, C7	Cf_{oc}, Cf_{ot}	1 nF	50-V SMD capacitor
R1	Rin	536 W	1-W resistor
C1	Cin	3.3 nF	25-V SMD capacitor

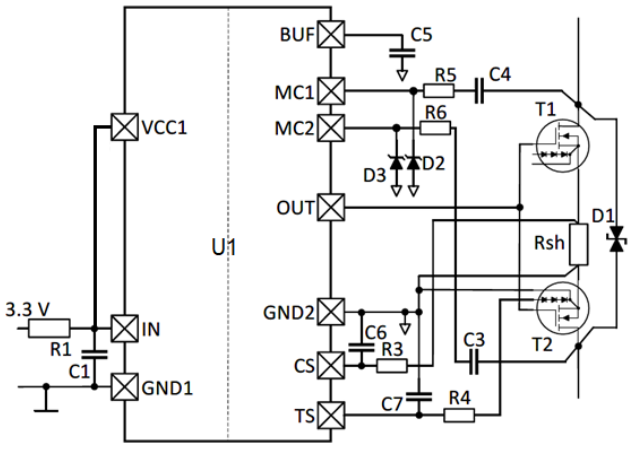


Fig.7 (again). SSR application schematic.

Now we can add a column to Table 2 and compare the present SSR design using the parts iSSI30R12H + 2x IPT60T022S7, versus our initial reference.

Table 6. DIN rail SSR solution comparison.

Specification	Single-phase SSR, 6 A, DIN rail	Single-phase SSR, 6 A, DIN rail (iSSI30R12H + 2x IPT60T022S7)
Type	Random voltage switching SCR output	Random voltage switching MOSFETs output
Operating voltage and current	4- to 32-Vdc input 24- to 280-Vac output, 6 A	12- to 24-Vdc input 24- to 280-Vac output, 6 A
Maximum voltage drop	< 1.3 V (on state) P_{diss} max =1.3 V X 6 A = 7.8 W	< 542 mV (on state) P_{diss} max = 0.542 x 6 A = 3.25 W
Maximum I^2T for fusing	410 A^2.s for 8.33 ms at 60 Hz 375 A^2.s for 8.33 ms at 60 Hz No protections	Overcurrent protection set at 60 Arms (≅ 85 A peak) Overtemperature protection set at MOSFETs' Tj = 155°C
Maximum leakage current	0.1 mA (off state)	< 36 µA at Tj = 25°C
Load current	0.15 A to 6 A	0 A to 6 A (no minimum holding)
dV/dt	500 V/µs off state at maximum voltage	>10 V/ns, with protection
Response time	0.5 cycle (turn off) 0.1 ms (turn on)	~2.5 ms (turn on) <1.5 µs (turn off in OCP and OTP)

An SSR For Panel Mount

We will now compare an SSI solution to an SSR for panel mount. The main characteristics for this device are given in Table 7.

Table 7. Commercial-panel-mount SSR characteristics.

Specification	Pre-assembled "Hockey Puck"
Type	Single-phase panel mount (as pictured in Fig. 5a) SCR output/zero voltage switching
Operating voltage and current	3- to 32-Vdc input 24- to 280-Vac output, 25 A
Maximum voltage drop (Power dissipation)	< 1.35 V (on state) P_{diss} max =1.35 V x 25 A = 33.75 W
Maximum I^2T for fusing	370 A^2.s for 8.33 ms at 60 Hz* 380 A^2.s for 10 ms at 50 Hz* *No protection
Maximum leakage current	0.1 mA (off state)
Load current	0.05 A to 25 A
dV/dt	500 V/µs off state
Response time	0.5 cycle (turn off) 0.5 cycle (turn on)

MOSFET selection

Similar to the discussion in the "An SSR for DIN rail mount" section, our target here is again to reduce the power dissipation on the SSR, while in the on-state, by a factor of 3 at full output current. Therefore calculating the $R_{DS(ON)}$ we obtain

$$R_{DS(ON)} = \frac{Pdiss}{3 * 2 * Imax^2} = \frac{33.75}{3 * 2 * 25^2} = 9\ m\Omega$$

Looking at Tables 3 and 4 the choice goes to the IPDQ60R007CM8, a 600-V, 7-mΩ at 25°C CoolMOS FET, which will have an $R_{DS(ON)}$ slightly higher than the target resistance at 150°C. However, at an average operating

temperature of 85°C, with about 1.45 x 7 = 10.15 mΩ, it will be a good compromise without the need to parallel two devices (see Fig. 8). This also neglects the shunt resistance power dissipation.

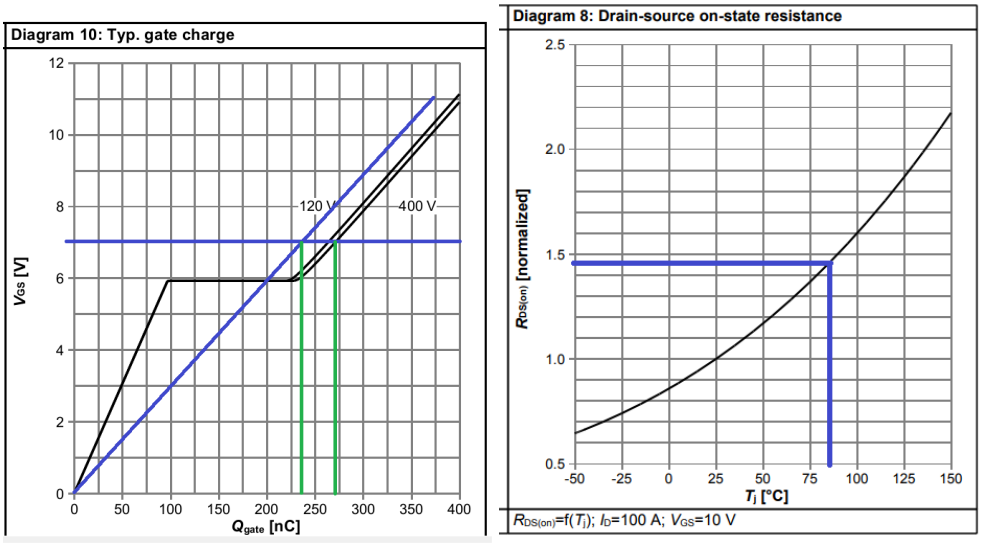


Fig. 8. $R_{DS(ON)}$ and Q_g values for IPDQ 60R007CM8.

Alternatively, and for better thermal protection, two IPDQ60T010S7 devices in parallel can be used, providing around 5-mΩ resistance. This would exceed our target, at the price of a slightly higher solution cost.

Temperature Protection

The selected CoolMOS FET doesn't have the integrated temperature sensors as in the S7T series. Therefore we need an external PTC to protect the devices from overheating and a different solid-state isolator must be chosen, in this case the iSSI30R11H (see Table 1), and made to read the PTC voltage feedback.

The PTC selected in this case is the B59721A0100A062, whose characteristic in shown in Fig. 9.

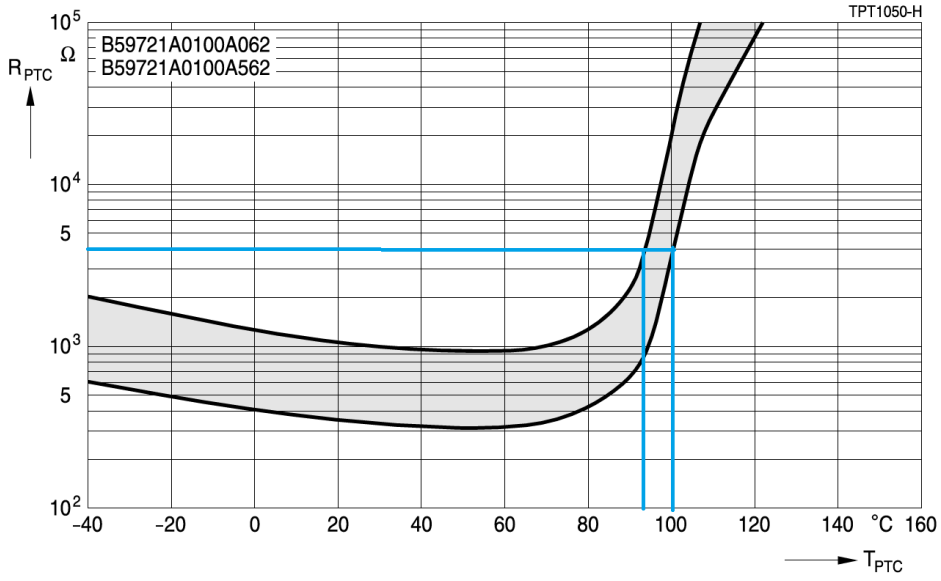


Fig. 9. PTC characteristic for the B59721A0080A062.

In the iSS30R11H the thermal protection triggers at VTS,th2 = 200 mV. Considering the internal current 50 µA (typ) generator, the protection in this case will trigger at the PTC typical resistance of

$$R_{OTPtyp} = \frac{200\ mV}{50\ uA} = 4\ k\Omega$$

which, from Fig. 9, corresponds to a measured heat-sink temperature between 92°C and 100°C. Of course, in this calculation the internal generator and V_{TS} threshold min and max values have to be taken in account for a more careful protection setup.

Component Summary And SSR Comparison

Now we can repeat all the calculations from the previous paragraph. Fig. 8 shows the $R_{DS(ON)}$ and Q_g values for the IPDQ60R007CM8, obtained from the datasheet and needed for the elaboration.
The new component values, referenced in Fig. 7 (repeated below again) are then shown in Table 8.

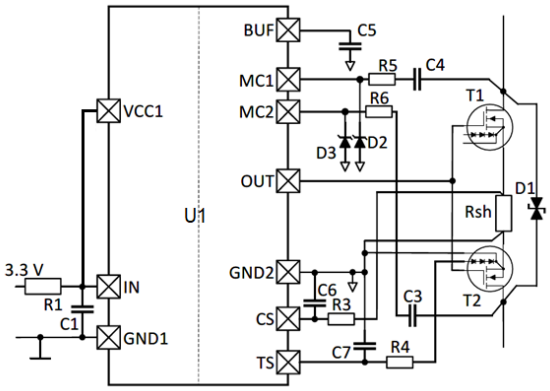


Fig. 7 (again). SSR application schematic.

Table 8. Component summary for a 600-V, 25-A SSR.

Schematic reference	Calculation reference	Value	Comments
U1	U1	iSSI30R11H	Infineon SSI
T1, T2	IPT60T022S7	IPDQ60R007CM8	Infineon CoolMOS 8 R-series
Rsh	Rsh	590 µΩ	Shunt resistor
D1	TVS	SMCJ400CA	1500 W in SMC package
D2, D3	DZ	3.3 V	Diode zener 500 mW
R3, R4	Rf_{oc}, Rf_{ot}	100 Ω	SMD resistor
R5, R6	None	0 Ω	Not used
C3, C4	C_{MC}	1 pF	2-kV SMD capacitor
C5	Cbuf	220 nF	50-V SMD capacitor
C6, C7	Cf_{oc}, Cf_{ot}	1 nF	50V SMD capacitor
R1	Rin	536 Ω	1-W resistor
C1	Cin	3.3 nF	25-V SMD capacitor
PTC	R_{OTPtyp}	B59721A0100A062	Temperature sensor

Now comparing the performances of this SSR design using the parts iSSI30R11H + 2x IPDQ60R007CM8, versus our initial reference we obtain the results shown Table 9.

Table 9. Panel-mount SSR solution comparison.

Type	Single-phase panel mount SCR output, zero voltage switching	Single-phase panel mount Random-voltage-switching MOSFET output
Operating voltage and current	3- to 32-Vdc input 24- to 280-Vac output, 25 A	12- to 24-Vdc input 24- to 280-Vac output, 25 A
Maximum voltage drop	<1.35 V (on state) P_{diss} max = 1.3 X 25 = 33.75 W	<522 mV (on state at 85°C) P_{diss} max = 0.522 x 25 A = 13.05 W
Maximum I^2T for fusing	370 A^2.s for 8.33 ms at 60 Hz* 380 A^2.s for 10 ms at 50 Hz* *No protections	Overcurrent protection set at 250 Arms (≅ 350 A peak) Overtemperature protection set at MOSFETs' Tc = 92°C to 100°C.
Maximum leakage current	0.1 mA (off state)	<66 µA at Tj = 25°C
Load current	0.05 A to 25 A	0 A to 25 A (no minimum holding)
dV/dt	500 V/µs off state at maximum voltage	>10 V/ns, with protection
Response time	0.5 cycle (turn off) 0.1 ms (turn on)	<2.0 µs (turn off in OCP and OTP) ~8 ms (turn on)

Summary And Conclusions

A new family of solid-state isolators has been recently introduced by Infineon Technologies to simplify the manufacturing of solid-state relays for industrial and commercial applications. These controllers have been developed to perfectly drive Infineon CoolMOS and provide SSRs with unmatched performance.

The main benefits of an SSR built with this new kit part solution are lower power dissipation (50% or less) than comparable SSR and TRIAC solutions; smaller heat sink and space required, lower weight; and overcurrent and overtemperature protection, eliminating the need for an external fuse, saving space. Other benefits are intrinsic dc operation (MOSFETs output stage, fast commutation); no minimum load current; lower leakage current and >1000 times dV/dt immunity.

This allows—for the first time—the ability to easily build short-circuit-protected SSRs, lower the power dissipated and reduce the space needed for this function in a power distribution cabinet.

References

1. iSSI20R02H, iSSI20R03H, iSSI20R11H, iSSI30R11H, and iSSI30R12H Infineon's coreless-transformer advanced solid-state isolators datasheet, Solid State Relays and Isolators page.
2. Eval-iSSI30R11H user guide board description and iSSI30R11H Infineon's coreless-transformer advanced solid-state isolator (Infineon SSI), user guide, Solid State Relays and Isolators page.
3. Eval-iSSI30R12H user guide Board description and iSSI30R12H Infineon's coreless-transformer advanced solid-state isolator (Infineon SSI), user guide, Solid State Relays and Isolators page.
4. "Infineon introduces new Solid-State Isolators to deliver faster switching with up to 70 percent lower power dissipation," Feb 28, 2024, Market News.
5. Solid State Isolators product family, training and documentation.

About The Authors

Davide Giacomini is marketing and application director at Infineon Technologies, leading the Power ICs group, responsible for new product definition and promotion, with a focus on high-power solid-state and switching applications for the industrial and automotive markets.

Davide has over 29 years' experience in the design and application of high-voltage integrated circuits for power supplies, motor drives systems and solid-state devices. His main interests include ac-dc and dc-dc converters in industrial and automotive environments, solid-state relays and circuit breakers, traction and auxiliary inverters for hybrid and full electric vehicles.

Davide holds 12 patents in the HVIC and power electronics system fields and is a senior member of the IEEE organization.

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