

Improving Validation Of Power Supply Re-Rush Performance Through More Accurate Sensing Of AC Line Peaks

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Switch-mode power supplies that support a wide range of input voltages (up to 277 Vac) in real applications can operate in various ac transient conditions such as voltage sags and surges, dropouts, line frequency deviations, etc. Although these conditions are detailed in power supply specs and replicated with conventional programmable ac sources during qualification, some power supplies that pass extensive qualification tests may still have a significant failure rate in the field due to ac transients associated with the so-called re-rush event.

The root cause of these failures has been isolated to overstress of the power factor correction (PFC) stage. This overstress may not be detected during power supply qualification due to the limited transient current capability of the existing ac grid-emulating equipment. To address this issue, a small-size transient test instrument operating from an actual ac grid and having much higher current capabilities was introduced in reference [1].

This article examines the impact of the ac peak voltage detection accuracy on replicating the worst-case re-rush condition and discusses shortcomings of the direct input voltage sensing technique. It then presents a simple technique based on voltage derivative sensing for improving the accuracy of such detection. The article concludes with some tips on designing a differentiator amplifier to implement this method.

Re-Rush Current

Voltage waveforms associated with ac line dropout and recovery causing the re-rush current spike are shown in Fig. 1. In this diagram input ac line voltage V_{IN} is represented by the green line, and PFC output (bulk cap) voltage V_C by the blue line.

During comparatively short ac line dropouts or in extended hold-up time applications, the resistor limiting the inrush current magnitude usually remains shorted. Consequently, it no longer limits the input current while the bulk cap provides energy to the load (dc-dc converter) such that the voltage across the cap can drop below the peak ac voltage level.

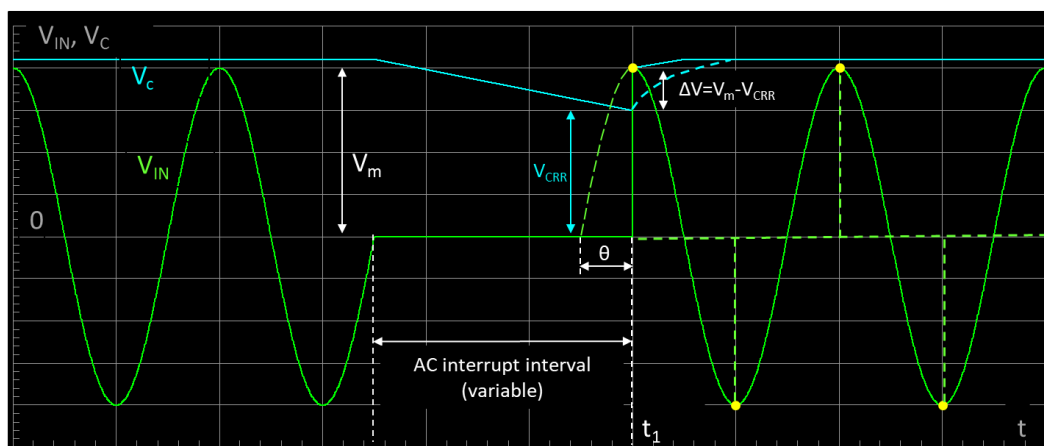


Fig. 1. Timing diagram illustrating the re-rush event. When PFC output voltage V_C (blue line) drops below the input ac voltage peak level (t_1) the re-rush current magnitude can be several times the initial inrush current magnitude and can cause PFC component failures. The dashed blue line represents V_C when a current limiting circuit is active during the re-rush condition.

If the ac line recovers at a phase angle close to 90 or 270 degrees (e.g. time t_1), an inrush or, more specifically, a “re-rush” current^[2] flows through the primary-side components. This current magnitude depends on the voltage difference between the input voltage magnitude V_m and bulk cap voltage V_{CRR} at the time of recovery (t_1). It can be several times the initial inrush current magnitude and cause PFC components to overstress.

In some cases, PSU designers use control algorithms and solid-state switches to activate the current control feature^[3, 4] during the re-rush event. This action limits the re-rush current magnitude at a lower level and slows the cap charge process spreading it in time (dashed blue line in Fig. 1).

However, this magnitude is still many times greater than the steady-state input PSU current and in some cases can cause PFC inductor core saturation. This means that even in the current limiting case, to ensure PSU robustness the re-rush performance also needs to be validated in conditions as close to real as possible. In other words, it must be proven that the re-rush magnitude is limited by the circuit inside the PSU and not by the programmable ac source used in the test.

Worst-Case Re-Rush Current Detection Challenge

As mentioned above, in the general case, the re-rush current magnitude I_{rr} depends on the voltage difference ΔV between the ac voltage level at the time of recovery and the voltage across the bulk cap. For a case where the input voltage exceeds the bulk cap voltage it can be described by the following equation:^[1]

$$I_{rr} = \frac{\Delta V}{R_{\Sigma}} = \frac{V_m |\sin \theta| - V_{CRR}}{R_{\Sigma}} \quad (V_{CRR} < V_m |\sin \theta|) \quad (1)$$

where V_m is the input voltage magnitude, θ is the ac recovery phase angle, V_{CRR} is the bulk cap voltage at the recovery time, and R_{Σ} is the total equivalent resistance (cumulative impedance) in the re-rush current path.

The dc-dc converter, loading the PFC stage, has a typical supply cutoff voltage of 300 V. This means that at, say, $V_{IN.RMS} = 264$ Vac the numerator in (1) may reach 72 V, while R_{Σ} in real applications does not exceed a few hundred milliohms.^[1] This causes I_{rr} to reach several hundred amps, making inrush-validation with existing conventional equipment unreliable.

The efficient small-size transient test instrument with a 1-kA peak rating introduced in reference [1] enables power supply designers and customers to validate their equipment using either existing live ac grids with variacs setting the desired voltage level or capacitor-buffered traditional programmable ac sources. A simplified functional block diagram of this instrument setup is shown in Fig. 2.

The instrument incorporates a high-current-rating solid-state relay (SSR) interrupting the ac power to the unit under test (UUT) and recovering it at the time when the ac voltage is supposed to reach its peak levels (i.e. at 90- and 270-degree phase angles):

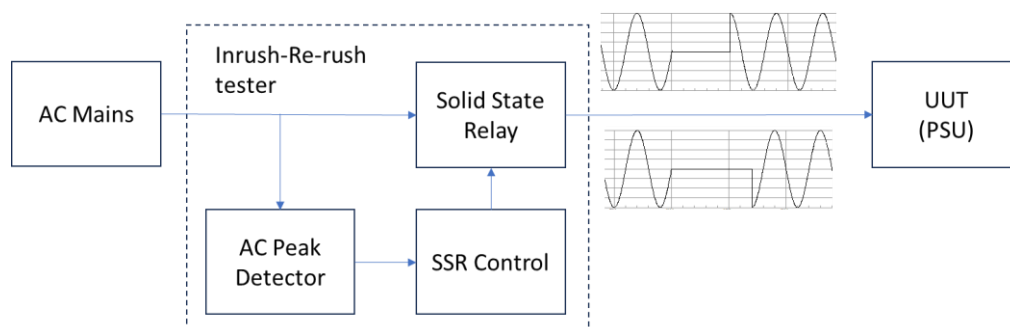


Fig.2 Simplified block diagram of the high-current-capacity inrush current tester setup. The instrument interrupts the ac power to the unit under test (UUT) and recovers it when the ac voltage is supposed to reach its peak levels (i.e. at 90- and 270-degree phase angles) to replicate the worst-case re-rush current condition.

Such an instrument can be used with or without active re-rush current control. One of the major challenges in replicating the worst-case re-rush condition in both cases is activating the SSR precisely when the line voltage reaches its peak level. This timing is critical because this is when the difference between the input voltage magnitude and the bulk cap voltage reaches its absolute maximum. In other words, accurate detection of the peak plays a crucial role in replicating the worst-case scenario for re-rush currents.

In real applications when the instrument sensor monitors the actual ac line voltage signal, we need to consider the inaccuracy of the peak-voltage-level detection network and the corresponding SSR controller trip point $V_{thr.actual}$. Such inaccuracy is associated with sensed voltage and voltage reference variations, divider component tolerances, comparator offsets, thermal drifts, etc., and represents the most typical cause of variations in analog circuits.

To accommodate the error associated with such inaccuracy, a certain margin Δ for the SSR controller's trip point needs to be factored into the equation for I_{rr} :

$$I_{rr.measured} = \frac{V_{thr.actual}}{R_{\Sigma}} = \frac{V_m(1 - \Delta - V_c/V_m)}{R_{\Sigma}}$$

This margin corresponds to the boundary between V_m and $V_{thr.actual}$ that must be considered to ensure that the controller will always activate the SSR with all mentioned component variations. By determining the error in the re-rush current magnitude as a ratio of the difference between the actual peak voltage- and the measured levels to the actual re-rush current magnitude:

$$Err = \frac{I_{rr.act} - I_{rr.measured}}{I_{rr.act}} = \frac{V_m - V_{CRR} - V_m(1 - \Delta - V_{CRR}/V_m)}{V_m - V_{CRR}}$$

and assuming the worst-case scenario ($|\sin\theta| = 1$) we can obtain the equation for the re-rush current magnitude detection error as a function of the V_{CRR}/V_m ratio and the margin Δ associated with voltage sensing and control circuit component variations:

$$Err = \frac{V_m \left(1 - \frac{V_{CRR}}{V_m}\right) - V_m(1 - \Delta - V_{CRR}/V_m)}{V_m \left(1 - \frac{V_{CRR}}{V_m}\right)} = \frac{\Delta}{\left(1 - \frac{V_{CRR}}{V_m}\right)}$$

The set of curves plotted based on this equation for the margin Δ ranging from 0.01 to 0.05 and the relative cap voltage V_{CRR}/V_m at the recovery time ranging from 0.7 to 0.95 is shown in Fig. 3.

As follows from the curves in Fig. 3, the detection error when a direct input voltage sensing technique is used is significant. When cap voltage at the time of ac recovery approaches the peak ac voltage ($V_{CRR}/V_m = 0.95$), despite the absolute re-rush current magnitude reduction (Eq.1), such an error can even approach the 100% level. An additional challenge in setting the trip point appears when the voltage magnitude varies with the application, so the trip point level must be adjusted based on the used line RMS voltage and its measured magnitude.

All this makes it relevant to examine how a more-accurate ac peak voltage detection can be provided in the instrument described in reference [1] and how the SSR can always get activated at the moments corresponding to the highest (worst-case) re-rush current magnitudes regardless of the applied input RMS voltage.

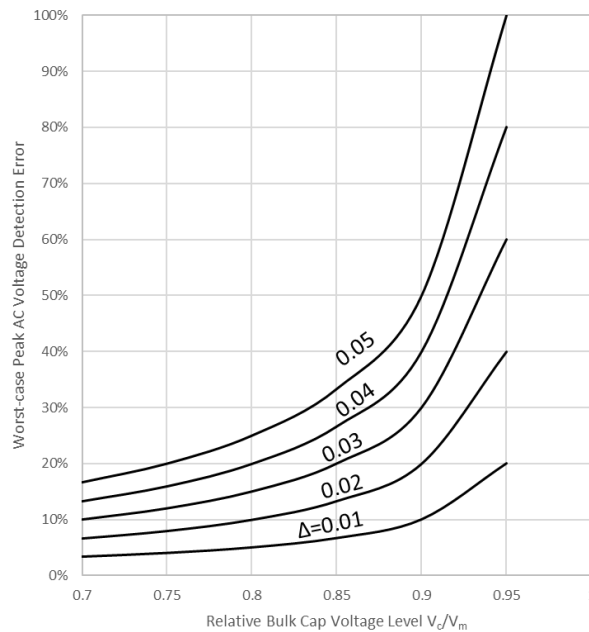


Fig. 3. Worst-case peak re-rush current magnitude detection error for direct voltage sensing case as a function of relative bulk cap voltage level V_{CRR}/V_m at different detector circuit threshold margins Δ , representing sensing components' variations.

The Voltage Derivative Sensing Approach

To improve the accuracy of the worst-case re-rush current magnitude detection let's consider the derivative of the sensed input voltage signal and compare it to the direct voltage sensing case. The derivative technique is commonly used in calculus to identify where a function reaches its local maximum or minimum. The blue line in Fig. 4 shows the timing diagram of the original sinusoidal input voltage waveform. It represents the sensed input voltage within a quarter of the line frequency period or a 0 to $\pi/2$ phase angle range. When a direct voltage sensing technique is used, the SSR must be activated when the sensed signal crosses the $V_{m1} = V_m - \Delta$ level.

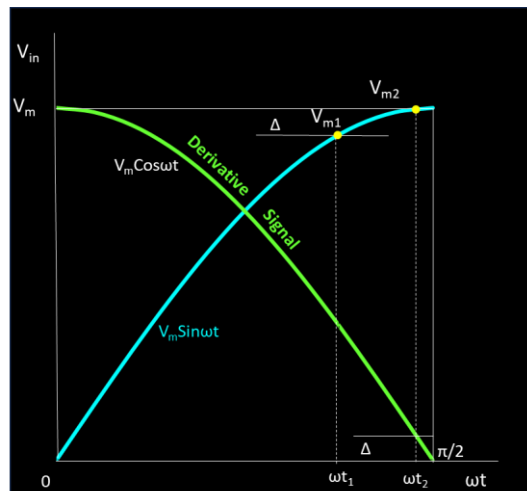


Fig. 4. Timing diagram of the sensed sinusoidal input voltage waveform (blue line) and its derivative (green line). By sensing the derivative of the input voltage signal the peak ac voltage detection error can be reduced ($V_{m2} > V_{m1}$).

Let's suppose we use a differentiator network producing the same signal magnitude as in the direct sensing case as shown in Fig. 4 by the green line. In such an arrangement we need to trip the control circuit activating the SSR in Fig. 2 when the derivative signal level crosses the zero axis or in a real application drops below the margin level Δ (Fig. 4).

With the SSR controller trip point having the same margin Δ as in the conventional (direct voltage signal sensing) case the diagram indicates that the trip voltage level in the derivative case V_{m2} appears to be noticeably closer to the actual line voltage peak condition than V_{m1} corresponding to the direct sensing case.

$$V_{m2} = V_m \sin \omega t_2 = V_m \sin\left(\frac{\pi}{2} - \frac{\pi}{2} + \cos^{-1} \Delta\right) = V_m \sin(\cos^{-1} \Delta) = V_m \sqrt{1 - \Delta^2} \quad (2)$$

Thus, for the derivative sensing, the error for the worst-case re-rush current detection will be

$$Err_{DER} = \frac{V_m \left(1 - \frac{V_{CRR}}{V_m}\right) - V_m \sqrt{1 - \Delta^2}}{V_m \left(1 - \frac{V_{CRR}}{V_m}\right)}$$

Fig. 5 shows a set of curves plotted based on this equation for the same parameter ranges as in the direct sensing case (Fig. 3). As can be seen from the comparison of the graphs in Figs. 3 and 5, the worst-case peak ac voltage detection error can be reduced by almost two orders of magnitude. As follows from equation (2), sensing the derivative signal also makes the peak detection accuracy, which can be defined as a ratio (V_{m2}/V_m), magnitude and line-frequency independent.

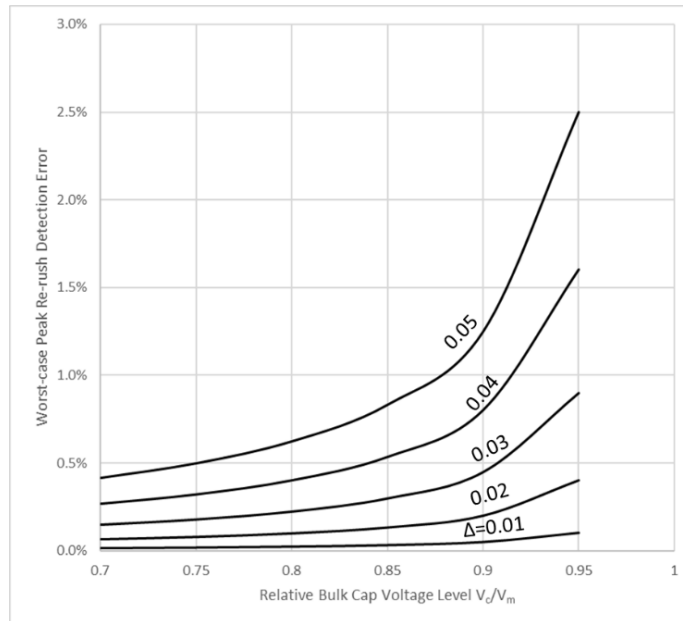


Fig. 5. Worst-case peak ac voltage detection error as a function of relative bulk cap voltage level V_c/V_m at different control circuit threshold margins Δ , representing sensing components' variations (derivative signal sensing case).

Differentiator Amplifier Component Selection Considerations

The output voltage of a conventional differentiator amplifier is described by the equation

$$V_o = -RC \frac{dV_{in}}{dt}$$

where R and C are the feedback resistor and input cap values, respectively.

In the above comparison, we assumed that the sensed voltage magnitudes are equal in the direct and derivative sensing cases. To meet this condition in practice we need to select the gain of the differentiator amplifier at the line frequency so that its output voltage magnitude equals the input voltage magnitude V_m . To get the same output voltage magnitude $V_{om} = V_m$ at $V_{in}(t) = V_m \sin \omega t$ and $V_o(t) = -\omega RC V_m \cos \omega t$ we need to provide $\omega RC = 1$. A negative sign in the above equation indicates that the input signal is fed to the inverting input of the opamp.

For easier tracking of 90- and 270-degree phase angles the signal fed to the differentiator amplifier input can be inverted (U1 in Fig. 6). This will also make the output signal match the green line waveform in Fig. 4. The condition $\omega RC = 1$ must be met at the lowest line frequency. This will guarantee that at higher line frequencies detection errors will not exceed levels shown in Fig. 5 diagrams.

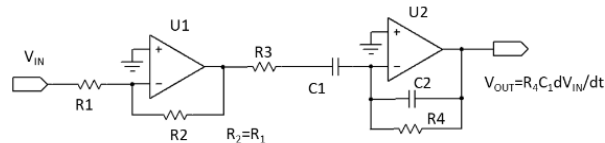


Fig. 6. Practical differentiator network. Using gain-limiting components C2 and R3 in the differentiator amplifier U2 helps to reject high-frequency noise if voltage sensing is performed on the primary side.

If the voltage sensing is performed on the primary side, high-frequency noise can affect the differentiator circuit operation and make it unstable. This can happen due to increased differentiator amplifier gain at the switching frequency and its harmonics.

To prevent this from happening the high-frequency gain of the circuit needs to be limited by adding an extra resistor in series with the input cap and/or an additional small value cap across the feedback resistor (R3 and C2 in Fig. 6). Such a circuit acts like a differentiator amplifier at low frequencies and an amplifier with resistive feedback and an integrator at higher frequencies providing a much better noise rejection.

References

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About The Author



Viktor Vogman is currently retired from [Power Conversion Consulting](#) where he applied his skills as an analog design engineer specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign [patents](#) and has authored over 20 articles on various aspects of power delivery and analog design.

For more on power protection in power supply design, see How2Power's [Design Guide](#), locate the "Design area" category and select "Power Protection".