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MLCCs Are At The Forefront Of Capacitor Miniaturization

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Point-to-point leaded component wiring was commonly used in electronic systems from the 1930s to very early 1960s. Before the printed circuit days, it wasn't uncommon to encounter leaded components soldered to tube sockets, binding posts, or terminal strips to create circuitry and systems. The passive components used back then were very large (e.g. 0.1-µF capacitors with 3 cc of volume) and had thick wire leads to provide rigidity and prevent long leads from shorting due to physical shock or vibration.

Those days ended with the emergence of transistors, printed circuit boards, and miniature molded, fluidized dipped, and powder-coated leaded passive components, including capacitors. These types of capacitors were significantly smaller and lighter than the previous generation of leaded capacitors due to new designs, materials, and processing and packaging technology. As such, the volume of a leaded 0.1-µF capacitor shrunk from around 3 cc to around 1 cc.

And while that was certainly impressive at the time, those days now seem like the stone age given that today's engineers can find EIA case size 0201 multilayer ceramic capacitors (MLCCs) with a capacitance of 10 µF (see Fig. 1). For a more direct comparison, a 10-µF capacitor built the old way, for point-to-point-based systems, would have a volume of around 300 cc. Today, you can find 0201 10-µF capacitors with a volume of just 5.5 x 10^{-5} cc!

This article begins with an overview of the market and technology trends, including the developments in materials and manufacturing processes, that have been driving down the size of MLCCs. A comparison of EIA case sizes illustrates the reductions in board space requirements and weight made possible by successively smaller standard packages.

Another stage in device miniaturization is producing lower-profile MLCCs, which allow mounting within IC packages and embedding in IC substrates and pc boards, along with other benefits. This leads to some discussion of other capacitor types, such as silicon and MOS, which have even lower package heights than the thinnest MLCCs but lower voltage ratings as well. Another device type not to be ignored is the single-layer ceramic (SLC) capacitors, which offer some advantages where wire bonding is required.

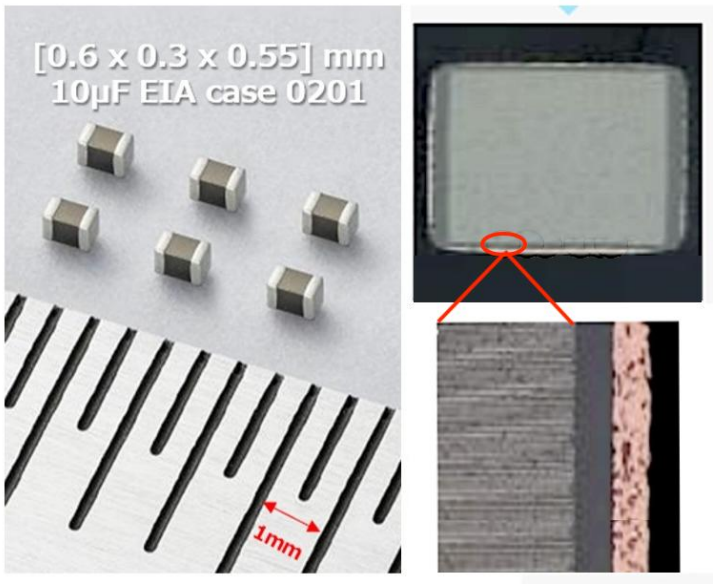


Fig. 1. 10-µF EIA 0201 MLCCs pictured next to a standard ruler (in) and in cross section (right).

The Driving Forces Behind Miniature MLCCs

MLCCs have achieved spectacular size reductions due to improved material systems, advanced manufacturing developments, and modernized designs.

Material scientists and engineers have made enormous strides in ceramic dielectric formulation and particle size distribution since the 1960s and continue to advance the technology. Today, the highest purity dielectrics and electrodes allow passive component manufacturers to create compact, exceptionally high-layer-count surface-mount technology (SMT) MLCCs that can approach capacitance densities of around 150 µF/mm³.

These MLCCs typically feature dielectric layers on the order of 1/100th the diameter of a human hair and 500 or more electrode layers in a small case. In fact, today's electrode and dielectric layers can be so thin that even small case size packages can contain very large active areas. For example, 0201 SMT MLCCs with 200,000 µm² of active area are readily available on the market.

Advanced manufacturing methods have improved as well, enabling the consistent laydown, patterning, and stacking of alternating ceramic and electrode layers with exceptional reliability and repeatable electrical characteristics. But the manufacturing advances don't stop there; they have progressed well beyond internal electrode stacking.

The MLCC packaging and electrical and visual testing processes have also been fully automated and optimized. Now, once a stack (i.e., the equivalent of a wafer start) has been completed, manufacturers can dice, fire, and terminate hundreds of millions of individual ceramic capacitors per day. Such high volumes allow manufacturers to create great efficiencies and therefore reduce MLCCs costs.

Design-wise, most of the advancements to-date have focused on case size reductions for very valid reasons. Smaller MLCCs take up less space on PCBs and weigh less, which enables the higher-density component counts needed to satisfy increasing product functionality demands and supports the electronics miniaturization trend. Smaller case size MLCCs also provide significant advantages in applications since the capacitors can be placed close to the load to optimize circuit performance.

Contextualizing The Advantages Of Miniature MLCCs

A good way to view and understand the magnitude of reduced-case-size MLCCs is to consider the reduction in board area when smaller case size parts replace larger ones in a 10-by-10 array of MLCCs. In the example below, we look at both the PCB board area savings and weight reductions achieved when a 10-by-10 array of 0805 MLCCs is replaced by smaller case size MLCCs. The table shows the massive board area savings and dramatic weight reductions achieved by using smaller case sizes.

Table. MLCC size and weight by EIA case size.

Size	Typical Chip Size (mm)	Mounting Area Ratio*	Weight (g/100pcs)	Weight Down Ratio
0805	2.0 x 1.25	100.0%	2.346	100.0%
0603	1.6 x 0.8	56.0%	0.901	38.4%
0402	1.0 x 0.5	25.7%	0.281	12.0%
0201	0.6 x 0.3	12.0%	0.043	1.8%
01005	0.4 x 0.2	7.1%	0.010	0.4%
008004	0.25 x 0.125	4.2%	0.001	0.1%

The Thinning Of MLCCs And Other Developments

Now that it's much easier to create small-case-size MLCCs, leading passive component manufacturers are turning their attention to the next stage of miniature MLCC product development: reducing the height of MLCCs.

Height reductions have the potential to positively impact the performance of MLCCs around complex ICs—and particularly in main board, die/land side, and embedded applications, which traditionally and respectively require MLCCs with thicknesses of 300 µm, 220 µm, and 150 µm (see Fig. 2 below). For comparison, standard general-purpose MLCCs might have the following maximum thicknesses by case size: 0201, 550 µm; 0402, 800 µm; and 0603, 1020 µm.

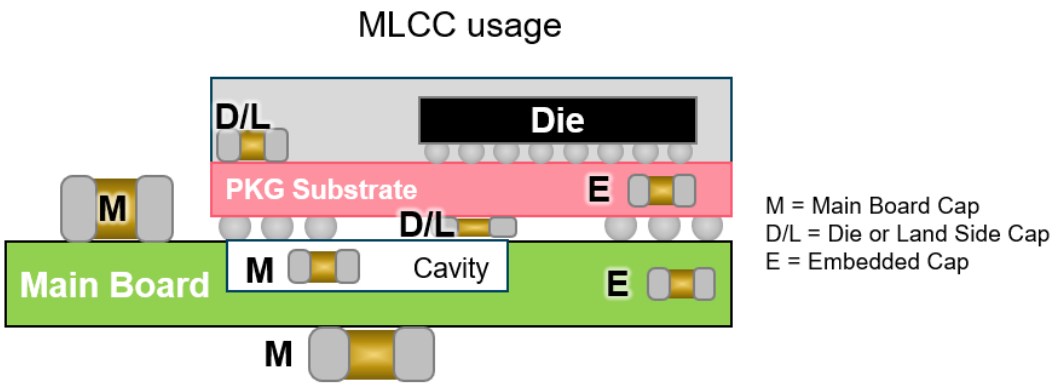


Fig. 2. While miniature MLCCs are shrinking space requirements on pc boards, the very smallest of these devices are being placed on IC substrates and even embedded within the pc boards and IC substrates.

In applications like these, reduced-height MLCCs exhibit notably improved electrical performance compared to standard-height but otherwise equivalent MLCCs because they reduce the inductance loop of the connected capacitor. This reduction improves the capacitor's ability to deliver high current slew rates with respect to time (di/dt). It also increases its self-resonant frequency (SRF), which allows the capacitor to operate across a wider frequency range before reaching its minimum equivalent series resistance (ESR) and having its response dominated by inductive reactance.

As previously mentioned, the consistent, reliable, and repeatable laydown, patterning, and stacking of astonishingly thin alternating ceramic and electrode layers is a key driver of MLCC miniaturization. It has dramatically reduced the portion of the overall MLCC cross-section that these crucial layers take up.

The combination of these process and material advances results in the ability to tightly control the electrode and termination dimensions. This, in turn, makes it feasible to create alternate electrode patterns that increase the device's series inductance while reducing its parallel inductance.

It has also resulted in the development of inductor/capacitor combinations, like 220-µm thick broadband LC-T configured filters, which are also known as three-terminal capacitors with capacitance values of 1 µF. Three-terminal capacitors (3Ts) exhibit exceptionally low inductance and broad frequency response.

For example, a 10% tolerance, 4.3-µF 3T might have an SRF of 20 MHz, an inductance in the 20-pH range, and ESR in the single-digit milliohm (mΩ) range. When 3T MLCCs are utilized in any of the three complex IC application examples pictured and described above (see Fig. 2), they enable inductance loop reductions of 20x or more when compared to standard-case MLCCs.

Miniature, Reduced-Height Alternatives To MLCCs

At present, MLCCs dominate in applications that allow for maximum thicknesses of 300 µm and 220 µm. The most common high runner capacitance values within this realm are 4.7 µF at 300 µm, 2.2 µF at 220 µm, and 470 nF at 150 µm.

Miniature, reduced-height MLCCs are the ideal technology for improving power quality on dc bias lines. Thin MLCCs offer large capacitance values with low ESR and ultralow inductance. Although there are alternatives to thin MLCCs, such as silicon capacitors and MOS capacitors, thin MLCCs have the added advantages of high voltage capabilities and higher di/dt current ratings.

Silicon capacitors are often considered for applications that allow for maximum capacitor thicknesses around 100 µm, as they can achieve thicknesses down to around 90 µm and be equipped with LGA, BGA, or custom configured terminations. However, silicon capacitors are limited to very low core level voltage ratings (<3 V), which is why they're not more common or discussed here any further.

If there's any flexibility in the 100-µm thickness requirement—for example, if the application will allow a device >100 µm but <130-µm thick—470-nF 01005 capacitors, which exhibit much higher voltages than silicon-based capacitors, can also be considered. Two other options include metal oxide semiconductor (MOS) capacitors and single-layer ceramic (SLC) capacitors.

MOS capacitors were initially designed for RF applications up to 20 GHz but are now widely used in embedded electronics. These devices have a thickness of 127 µm and are ideal in RF bias banks where they can be embedded in substrates or placed directly under high-frequency active devices. They also have breakdown voltages of up to 200 V, which enables their use in higher-voltage bias applications for emerging III-V semiconductors.

Single-layer ceramic (SLC) capacitors are available in a wide variety of sizes, configurations, thicknesses, and dielectrics (e.g., NP0, X7R, and X7S), rated for up to 100 V, and are ideal for applications such as dc blocking and pre-impedance matching internally to the active device's package. The range of SLC capacitor thicknesses is designed to provide engineers with options that are about the same thickness as the devices they are wire bonded to in order to minimize the inductance of lead wires.

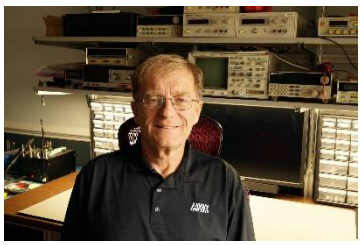
Conclusion

Recent improvements in MLCC material systems, manufacturing processes, and designs have led to the development of compact, low-profile, and increasingly efficient high-capacitance devices, like 3T MLCCs, that deliver improved performance in power delivery networks; are ideal for applications with high-density PCBs, challenging space and weight requirements, and complex ICs; and have great promise for miniature power conversion circuits.

References

1. "Low Inductance Capacitors For High-Speed Decoupling" by Robert Lu, KYOCERA AVX technical paper.
2. "Inductance Measurements for Multi-Terminal Devices" by Ben Smith, KYOCERA AVX technical paper.

About The Author



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For more on capacitor selection for power design, see the "Component" category and select "Capacitors."