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## Gate Driver Enables Scalable EV-Powertrain Designs

STMicroelectronics' STGAP4S galvanically isolated automotive gate driver for SiC MOSFETs and IGBTs gives flexibility to control inverters of different power ratings featuring programmable protections and rich diagnostics that allow ISO 26262 ASIL D qualification. With analog-to-digital converter (ADC) and flyback controller integrated on chip, the STGAP4S provides a highly featured and functional-safety qualified driver for scalable EV-powertrain designs.

The STGAP4S owes its flexibility to the output circuit that allows connecting the high-voltage power stage to an external MOSFET's push-pull buffer to scale the gate-current capability. This architecture lets engineers leverage the STGAP4S and its wide features to control inverters with different power ratings, up to high-power designs with multiple power switches in parallel. The driver can generate up to tens of amperes of gate-drive current with very small MOSFETs and handles a maximum operating voltage of 1200 V (see the figure).

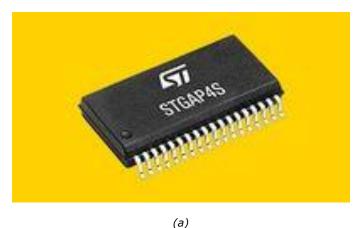
Among the driver's key features, its advanced diagnostics facilitate system-safety integrity up to ISO 26262 level D (ASIL-D) for safety-critical applications. The diagnostics include self-checks to verify the integrity of connections, the gate-drive voltages, and correct operation of internal circuitry such as the desaturation and overcurrent detection. The host system can read the diagnostic-status register through the IC's SPI port. In addition, two diagnostic pins provide hardware-detectable indications of fault status.

In addition to desaturation and overcurrent detection, protection features include active Miller clamping, undervoltage and overvoltage lockout, overtemperature detection. Configurable parameters include protection thresholds, deadtime, and deglitch filtering, which are programmed through the SPI.

The IC's fully protected flyback controller can be used to generate the supplies of the high-voltage section for the positive and negative gate-driving signals. This enables fast, efficient switching of SiC MOSFETs. The galvanic barrier provides 6.4 kV of isolation between the low-side circuitry and the high-side sections.

An evaluation board, the EVALSTGAP4S, includes two STGAP4S drivers to help designers complete evaluation of their features in a half-bridge application. The design lets users easily connect more boards together to evaluate more complex topologies such as a three-phase inverter.

The STGAP4S is in production now, in a SO-36W wide-body dual-inline package, priced from \$4.66 each for orders of 1000 units. For more information, see the <u>STGAP4S</u> page and the <u>EVALSTGAP4S</u> page.





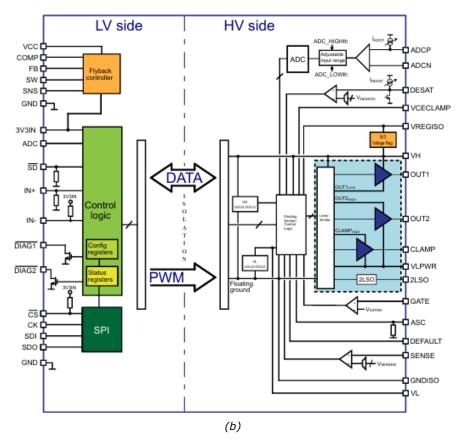


Figure. The STGAP4S is a galvanically isolated single gate driver for IGBTs and SiC MOSFETs with advanced protection, configuration and diagnostic features. The architecture of the STGAP4S isolates the channel gate driving from the control and the low voltage interface circuitry through true galvanic isolation. The output architecture is designed to allow the use of an external MOSFET push-pull stage giving flexibility in terms of current capability dimensioning and easing the use of several power switches in parallel. A package photo (a) and an internal block diagram (b) are shown here.