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Dickson Architecture And Novel Switching Techniques Enhance Charge Pump Benefits

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The charge pump or capacitor divider is increasing in popularity in high-efficiency power conversion, particularly for slim, low-profile, battery-powered applications. This article explores the use of multiple capacitor division ratios on the same IC device. It also introduces a feature that allows dynamic and seamless transitions between the ratios, depending on the external circuit environment. By considering various battery-powered architectures, we show how the charge pump offers significant advantages and how the ability to dynamically transition between ratios extends the system run-time.

This article focuses on specific technologies used in pSemi voltage regulators. As such, it analyzes operation of the Dickson charge pump architecture and the company's novel "adiabatic" or lossless switching of the charge pump. With this switching technique the charge redistribution is stored in a small inductor and recycled to the output. This improves efficiency and reduces electromagnetic interference (EMI) compared to conventional charge pump architectures.

Finally, this article explores how multiple divider ratios in the same IC device can be applied in real product examples. It describes how to dynamically transition between ratios to provide system-level benefits.

Introduction To Charge Pumps

A charge pump (CP) is a type of dc-dc converter that stores and transfers energy through switched capacitors (SCs), effectively increasing or lowering a dc voltage. It is an alternative to inductor-based converters and is commonly employed in high-conversion ratio applications that require great efficiency and low profiles. Most applications are space constrained and often power components are the largest, bulkiest ones in the system. With its smaller components, a charge pump can mitigate this problem.

From a lower-level perspective, charge pump circuits work on the fundamental principle that the voltage across a capacitor cannot change instantly. Charge pumps make use of this characteristic by manipulating the voltage across a capacitor with precisely timed switches.

There are several SC converter topologies in the literature; however, their benefits can differ based on the voltage range or power level in the applications. The Dickson charge pump is a common design that uses cascading stages to generate voltage dividers or multipliers. It is a handy and cost-effective circuit that employs capacitor stages and switching signals.

Assembling the circuit is simple but understanding how it works can be more difficult. The increased number of FET switches increases the complexity of the control and gate-drive circuitry. Furthermore, to debug and size components in your design, such as fly capacitors and switches, you must first understand how they work.

Dickson Architecture Description

Fig. 1 shows a simplified divide-by-n Dickson charge pump. As the division ratio of input voltage (V_{IN}) increases, the number of stages increases linearly, but the current through each stage decreases linearly. The Dickson charge pump exposes all switches to a maximum voltage of 2 × output voltage (V_{OUT}). This implies that when the division ratio increases, the number of stages must increase while the voltage rating of each switch remains constant.

This important property of the Dickson charge pump allows the gate charge losses to stay constant even when the division ratio is high. Multi-phase Dickson charge pumps offer additional benefits like enhanced efficiency, higher output power, and quicker output transitions by using multiple charge pump stages that can be operated in parallel, as shown in Fig. 2 for a divide-by-3 dual-phase Dickson charge pump.

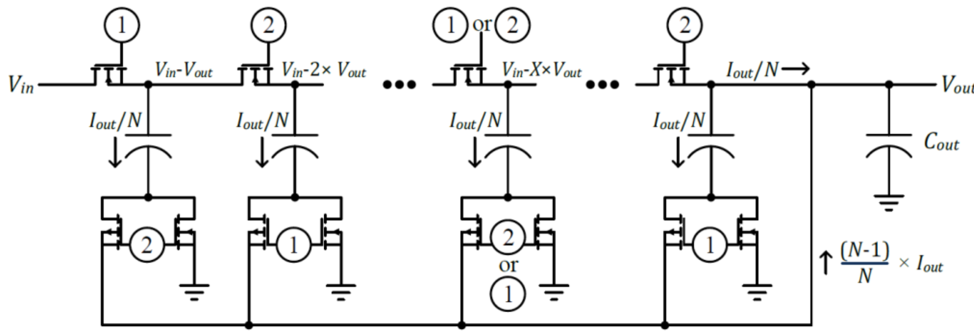


Fig. 1. Divide-by-N Dickson charge pump.

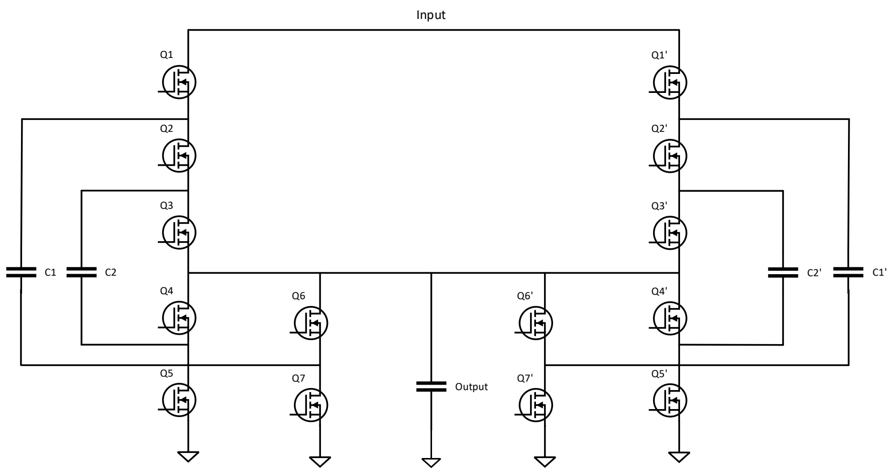
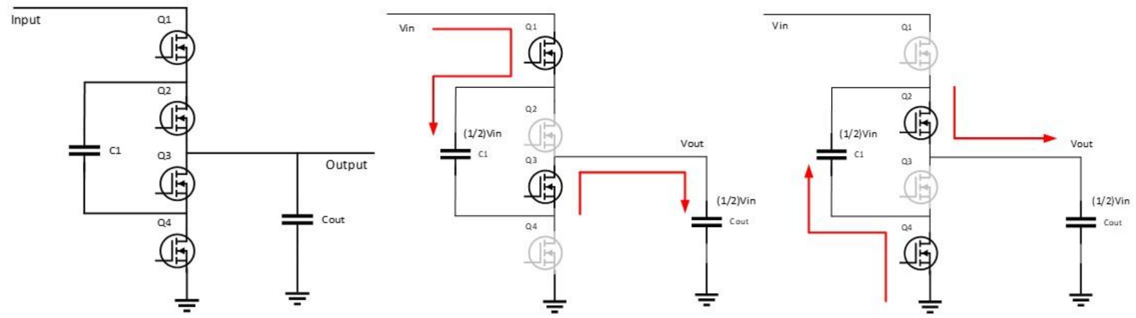


Fig. 2. Divide-by-3 dual-phase Dickson charge pump. The circled 1s and 2s indicate the order of gate drive signals—this will become clearer after reading the explanations for Figs. 3 and 4.

The Dickson charge pump places the burden of withstanding high voltages on the capacitors, not the switches. In contrast, a typical series-parallel charge pump (the most common architecture) drops the high voltage on the switches rather than on the capacitors. The gate-charge losses in this architecture increase with V_{IN} because the gate capacitance of the switches increases with the voltage rating. In addition, the series-parallel architecture design cannot be extended to a multi-phase configuration.

Fig. 3 shows a Dickson divide-by-2 charge pump with a single capacitor and four switches. This circuit works in two states:

- In state 1, Q1 and Q3 are closed, but Q2 and Q4 are open. In this state, the positive and negative terminals of C1 are connected to V_{IN} and V_{OUT}, respectively. The V_{IN} is reduced by the charge stored on C1 and it is balanced by the output capacitor (C_{OUT}).
- In state 2, Q1 and Q3 are open, but Q2 and Q4 are closed. The negative terminal of C1 is connected to ground, and the positive terminal is connected to C_{OUT}. Because the voltage across a capacitor cannot change instantly, it attempts to maintain an equivalent balanced voltage, where V_{OUT} is the divide-by-2 of V_{IN} if C1 and C_{OUT} are equal.

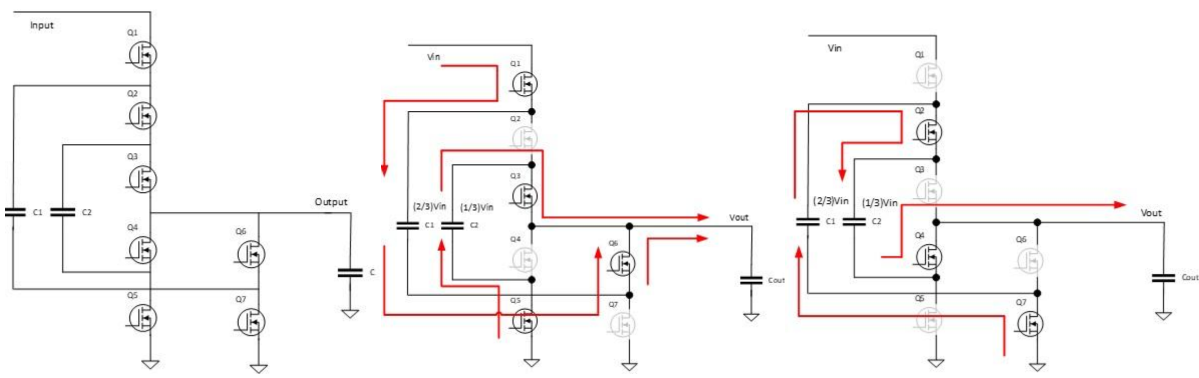


State 1. Vin is charging C1 State 2. C1 is discharging

(a) (b) (c)

Fig. 3. Divide-by-2 Dickson charge pump (a) and its switching states (b and c).

Fig. 4 shows the divide-by-3 charge pump and its states; each state can also be analyzed by using fundamental knowledge of a capacitor divider. As expected, the stages can be expanded by adding more fly capacitors (all of the floating capacitors being charged or discharged by the switches while storing and transferring energy, resulting in an intermediate voltage level) and switches to make a multiple divider charge pump, as shown in Fig. 1.



State1. Vin is charging C1; C2 is discharging

State2. C1 is discharging; C2 is charging

(a) (b) (c)

Fig. 4. Divide-by-3 Dickson charge pump (a) and its switching states (b and c).

Traditional CP Advantages And Disadvantages

One of the major advantages of a charge pump over a typical buck converter is its smaller size, eliminating the need for an inductor. Inductors occupy a lot of board space because their inductance value is directly proportional to the number of turns, and more turns require more space.

If precise regulation is not needed, charge pumps offer advantages such as simplicity, high efficiency, and the ability to buck and boost input voltage. The major distinction in charge pumps occurs in the current profile; there is no inductor driving current during transition, or a current path is not established until the switching has occurred. C_{OUT} supplies the load current during the transition. This eliminates switching commutation losses.

However, this statement assumes ideal capacitors and switches, both of which are not feasible in real-world applications. Some reasons for non-ideal behavior in charge pumps include MOSFET gate charge losses, I^2R losses and charge redistribution losses. Each of these challenges can lead to lower efficiencies in charge pumps, and the charge redistribution is especially responsible for the poor overall adoption of charge pumps today.

Consequently, traditional charge pumps are not competitive in efficiency because they incur redistribution losses while balancing fly capacitors through parasitic resistance, especially when the voltage gap between capacitors is large. Charge pumps also have an elevated level of output ripple and noise, and limited output current, making them inferior to other voltage regulators. Another constraint is that charge pumps can only be configured as multipliers or dividers.

The next section discusses a technique to mitigate charge redistribution losses—pSemi's novel adiabatic or lossless charge pump switching.

An Adiabatic Charge Pump

pSemi's novel adiabatic or lossless soft switching of the charge pump could be an excellent solution for achieving high conversion ratios with lower switching losses. With this style of switching, the charge redistribution is stored in a small inductor and recycled to the output. This improves efficiency and reduces EMI noise compared to traditional charge pump architecture.

The charge redistribution losses are caused by the voltage differences in the capacitors while charging and discharging the stored energy. In a charge pump, a capacitor is typically switched in parallel or in series with other capacitors resulting in charge redistribution loss. This redistribution loss is a function of capacitor size and switching frequency and is modeled as an extra series parasitic resistance in Fig. 5.

If C1 and C2 are identical capacitors, and C1 is charged to higher voltage than C2, the starting energy is twice the ending energy after the charge redistributes and balances. The lost energy is dropped across any parasitic components in the current loop. Because the charge is moving from high to low potential, power is lost. As more of the charge moves from C1 to C2, the voltage on C1 drops and the voltage on C2 rises. This reduces the voltage potential across which the charge needs to move and thus reduces energy loss. In other words, energy loss is reduced as the voltage potential between the two capacitors equalizes.

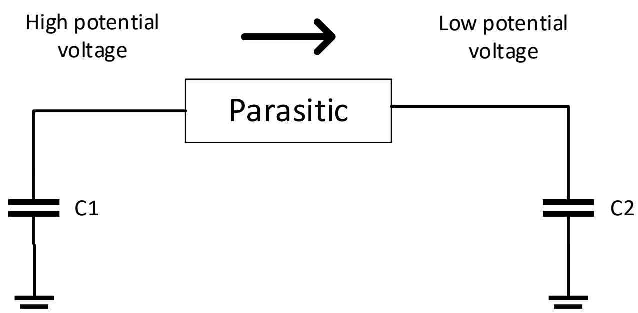


Fig. 5. Charge redistribution power loss.

If the parasitic resistance between C1 and C2 is a resistor, the current profile shows an exponential decay that creates a large RMS current. When the voltage across the resistor is large, the current through the resistor is also large, and the energy loss is at a maximum. As the voltage level decreases, so does that current.

The energy loss can be calculated with effective capacitance (C1 in series with C2 = 0.5 x C1) and the total energy loss is half that stored in C1 initially, before the charge is redistributed. The energy loss is independent of the resistor size and how it gets balanced by $\frac{1}{2}C\Delta V^2$.

Energy loss is an important insight when working with moving a fixed amount of charge, such as in a charge pump, because reducing the potential voltage between the capacitors reduces power loss. In a charge pump, using larger capacitances to minimize the voltage difference reduces charge redistribution losses.

pSemi has developed novel charge pump architectures that use a small, adiabatic output inductance. Adding an adiabatic inductor allows the current to resonate between capacitors and eliminates the charge redistribution losses in the fly capacitors. The simplified block diagram in Fig. 6 shows that the voltage drop occurs at the current source (I_{src}) and the energy is absorbed inside the current source like an inductor and recycled to the output load.

The act of charging and discharging capacitors with no charge redistribution losses is referred to as adiabatic or lossless operation.

In theory, the concept of an adiabatic charge pump is simple. But during the charging and discharging phases of an adiabatic operation the charge pump must ensure that the charge flows in and out of the fly capacitors, thus forcing any voltage difference between the capacitors to be dropped across the current source. A mismatch in the capacitance of parallel capacitors also results in a mismatch in the voltage between them while charging. Therefore, some form of stabilizing circuits might be required to ensure that the capacitors are balanced.

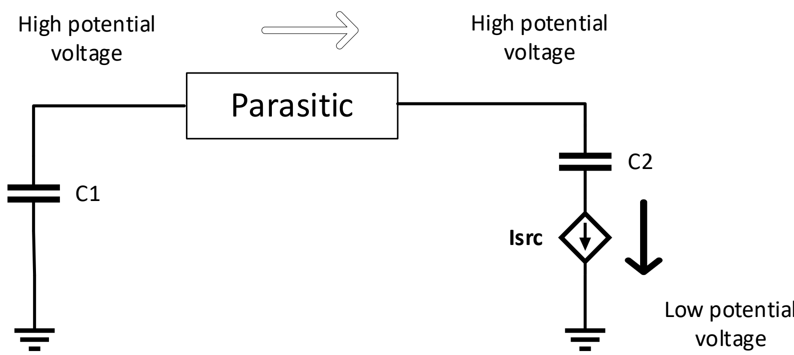


Fig. 6. Charge redistribution power loss with current source.

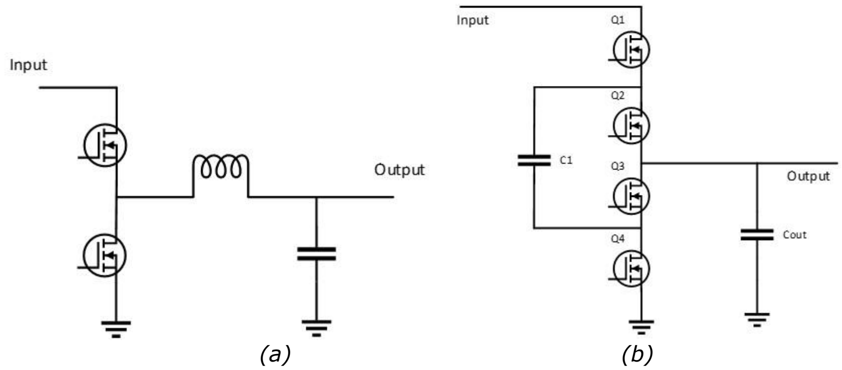
CPs With Adiabatic Switching Compared To A Buck Converter

The typical synchronous buck converter shown in Fig. 7(a) is widely used, but has significant drawbacks and limits. In the buck topology, the input voltage and ground at the switched node alternate between two levels. This means that the switch node waveform experiences a large voltage swing, requiring the use of a large output filter (output inductor and output capacitor) to deliver smooth dc voltage to the output load, particularly when the input and output voltage ratio is high.

With a low duty cycle on the high-side FET supplying all the average current, the current spike is a major issue, so decoupling capacitors must be placed in front of the FET. The larger the current spikes, the more decoupling capacitance is needed. At some point, controlling the conductive EMI becomes more problematic.

Voltage stress is further increased by leakage and parasitic inductances as the current reverses in the output inductor. The net result is that the designer must select higher-voltage FETs, reducing conversion efficiency. In standard buck or boost converters, the higher the conversion ratio, the worse the efficiency: The larger the voltage transitions, the more the EMI noise causes severe efficiency losses.

As previously stated, charge pumps have various advantages over standard buck converters. Fig. 7(b) shows a divide-by-2 Dickson charge pump, which merely uses fly capacitors and FET switches, to compare how its circuit differs from that of a buck converter.



7. Synchronous buck converter (a) and divided-by-2 Dickson charge pump (b).

pSemi's PE25203 and PE25213 charge pumps, which employ an optimized Dickson architecture and adiabatic switching, offer ultra-high efficiency solutions in a fixed area regardless of input-to-output ratio. These products achieve 97% to 99% power efficiency independent of the input-to-output ratio, resulting in a net system efficiency performance advantage. In the charge pump, capacitors do most of the work, and the inductor requirement is reduced. (The inductor used for adiabatic switching is much smaller than that needed by a buck converter.) Fundamentally, capacitors have more than 400 times the power density of inductors.

Because pSemi's charge pumps benefit from input voltage-independent losses, a higher stepdown or stepup ratio yields greater efficiency gain. At the same time, adiabatic charging allows the fly capacitors to function with higher voltage ripple, allowing the charge pumps to switch less frequently and increase efficiency, which has a positive impact on both gate charge losses and I^2R losses.

However, charge pumps, like transformers, are open-loop converters with no control loop, meaning they are merely voltage converters with no regulation, which is the fundamental disadvantage of most charge pumps. As a result, you can think of the charge pump as an intermediate bus in a two-stage system that uses a buck converter to regulate output voltage.

Multiple Ratios And How They Work

pSemi's charge pumps implement all the power switches and switch control to operate in either divide-by-2, divide-by-3, or divide-by-4 mode. As previously introduced, with Dickson architecture, the ratios are achieved precisely with non-overlapping switches in the same IC device. pSemi's charge pumps are based on the Dickson architecture, which can be modified to configure multiple division ratios, making them more efficient than the standard Dickson architecture.

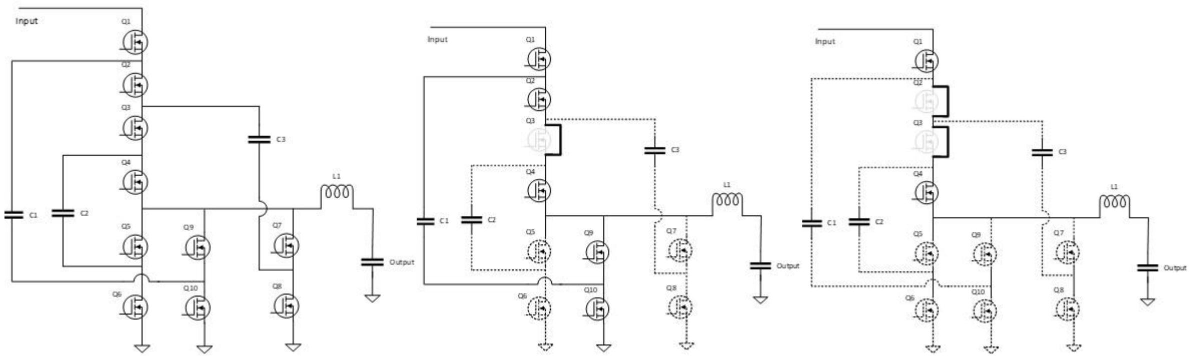
Fig. 8 shows how the multiple ratios can be switched to divide-by-2 or divide-by-3 with pSemi's configurable divide-by-4 Dickson charge pumps. Here, the fly capacitors must be well balanced, and effective capacitance values with dc voltage bias must also be considered for proper charge pump operation.

- To transition from divide-by-4 to divide-by-3, Q3 is shorted while C2 and C3 operate in parallel, with Q5 and Q7 switching together and Q6 and Q8 switching together.

- To transition from divide-by-3 to divide-by-2, Q2 is additionally shorted while C1, C2, and C3 work in parallel, with Q5, Q7, and Q9 switching together and Q6, Q8, and Q10 switching together.

Now you can have the previously described divide-by-3 and divide-by-2 Dickson charge pumps in state 1 and state 2, respectively, although the fly capacitors operate in parallel, and the switches work together as shown in Fig. 8.

As shown with the divide-by-4 architecture, changing the ratio requires reconfiguring the switch and capacitor connections. If not handled correctly, this could produce fluctuations in the output voltage and current. In a real implementation, it would be more complicated with a dual-phase scheme and stabilizing circuitry. Appropriately-sized fly capacitors and MOSFET switch drivers must be carefully selected to ensure fast, clean switching and that there is no difference in effective capacitor values.



State 1. Divide-by-3 CP *State 2. Divide-by-2 CP*

(a) *(b)* *(c)*

Fig. 8. Transitioning from divide-by-4 charge pump (a) to Dickson divide-by-3 (b) and divide-by-2 (c).

Seamless Dynamic Transitions Between Ratios

Achieving seamless dynamic transitions between different ratios is crucial for many battery applications but can be a challenge for charge pump architectures. To reduce instabilities such as transition time, voltage spikes and current surges, careful design is essential. pSemi's unique solution enables seamless transitions with some strategies.

pSemi’s charge pumps offer an auto-switch mode to change the divide-down ratio during operation to avoid a downstream undervoltage lockout (UVLO) event when there is a sudden input voltage drop at heavy system loading during low battery conditions.

The dynamic transitions between ratios must be smooth and glitch-free while minimizing disruption to the output voltage and system stability. When the output transitions, the device provides both the current to charge the output capacitor and the current to supply the downstream load. As a result, the rise and decline rates of the output voltage depend on the load and output capacitance.

If the output is not loaded, during the transition time, the charge pump switches to the lowest switch frequency setting and waits for the output to discharge gradually. To limit current surges, the soft start-stop method or current limit can be incorporated during reconfiguration.

The dynamic auto-switch mode is achieved by using an inverter comparator with hysteresis circuitry. The input voltage is sensed to vary the division ratio.

However, using a constant threshold can result in unwanted output transitions due to noise, signal fluctuation, or slow-moving signals. Setting the upper and lower hysteresis thresholds prevents unwanted output transitions. Sense resistors control provides two alternative voltage trigger points.

For example, by auto-switch mode trigger levels, the charge pump can seamlessly transition to divide-by-3 to 2 or divide-by-2 to 3, where V_{IN} is around 9 V in the case of a three-cell battery application to increase battery run-time. The threshold and hysteresis can be adjusted depending on the number of battery cells used.

In general, seamless dynamic transitions between charge pump ratios require a combination of careful switching sequences and capacitor management. The specific methods vary depending on the charge pump topology, transition speed, and overall system characteristics.

System Examples And Benefits

In many electronic systems, a charge pump can serve as a front-end converter to step up or step down voltages. Numerous benefits result when combining a charge-pump with a dc-dc converter and implementing an adiabatic charging system. Using an intermediate bus to step down from 2- to 4-cell batteries or charging batteries fast using the USB PD-EPR standard with minimal power dissipation are two example uses in mobile systems.

Core processors are moving towards fine geometry silicon with reduced voltage supply requirements and increased current. The charge pump output can supply a high efficiency voltage to the SoC, FPGA, and other peripherals in the power system for an intermediate bus application, lowering the size and inductor requirement for low-profile solutions.

For example, divide-by-2 for three-cell batteries typically allow existing core voltage to be used without resulting in the UVLO, as shown in Fig. 9. Seamless dynamic transition to divide-by-3 makes the system run-time longer, which is one of the benefits of multiple capacitor division ratios on the same IC device. The high efficiency reduces system loss by about 30%, improving system run-time, potentially leading to a reduction in battery size, system size, and weight, and enabling thin form-factor design.

Many systems derive low voltages from a much-higher multi-cell battery voltage. By using a charge pump as an intermediate bus, buck dc-dc converters in the system see an input voltage that is one-half to one-third that of the system input voltage, and therefore have much higher efficiency with a smaller conversion ratio.

Higher duty cycle or on-time in the buck converters means less inductance with a smaller inductor having a low DCR. At the same time, lower voltage-rated FETs have less parasitic capacitance, so they improve light load efficiency and increase the switching frequency, which allows for a smaller inductor. Overall, the system has a smaller size with lower system EMI and smaller input and output filters.

In contrast, with one-stage buck converters, increased inductance leads to poor transitional performance. You're also limited by switching frequency, so overall this entire solution suffers from the higher conversion ratio.

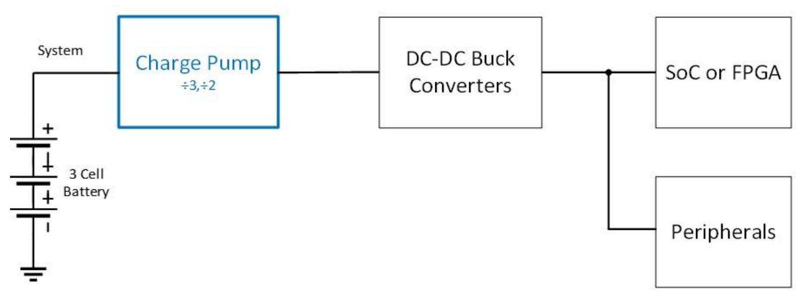


Fig. 9. Intermediate bus in the system.

Meanwhile, battery charging speeds are continually increasing. Thus, power dissipation and thermal issues are becoming an issue with high power in USB fast charging. Another application in a mobile system is to employ the charge pump as an auxiliary charging IC with USB PD-EPR input, capable of high-efficiency battery charging from a variable input PPS and AVS adapter, as shown in Fig. 10.

For example, the wireless charging (WLC) input voltage is increased to 18 V to lower current in the WLC coil while pushing the higher WLC power. With about 99% peak efficiency, high charging power can be delivered in constant-current mode, while trickle charging or constant-voltage charging is handled by the main charging IC. pSemi has developed optimized charge pump solutions for divide-by-2, divide-by-3, and divide-by-4 architectures based on the input voltage with varied voltage and current steps (PPS, AVS) on several types of USB PD-EPR adaptors and USB cables.

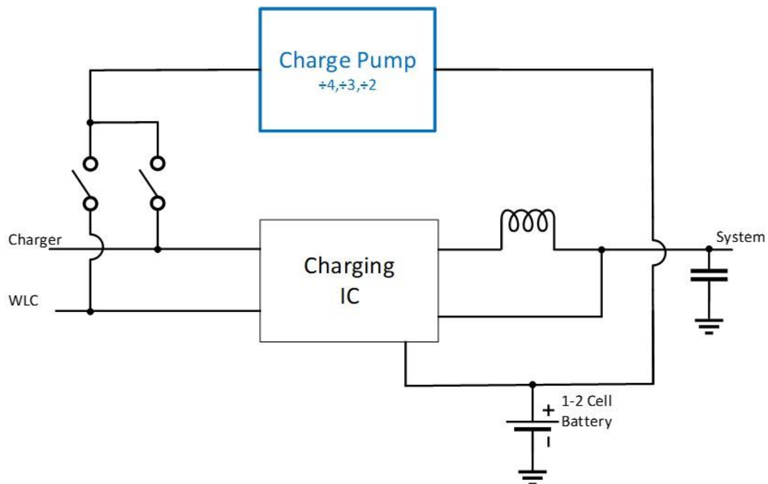


Fig. 10. USB PD/PPS/AVS battery charging.

Summary And Conclusion

Charge pumps have several advantages, including a high conversion ratio, great power efficiency, and low-profile battery-powered applications, but they also present several hurdles to establishing real-world operations. This article examined the Dickson charge pump architecture and how it functions using divide-by-2 circuit analysis, as this architecture overcomes some common CP limitations. The advantages and disadvantages of charge pumps versus a normal buck converter were discussed.

In addition to the Dickson architecture, other unique aspects of pSemi's charge pump designs contribute to their performance. The importance of pSemi's novel adiabatic soft-switching design in real-world product applications was explained. The uses of multiple divider ratios and flawless dynamic transitions in the same device were also briefly discussed.

Finally, two real-world system examples were cited to illustrate the benefits of using a charge pump.

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For further reading on designing dc-dc converters, see the How2Power Design Guide, locate the "Power Supply Function" category and select "DC-DC converters".