CS MANTECH Peers Into The Future Of Power Semiconductors

by David G. Morrison, Editor, How2Power.com

Wide-bandgap power semiconductors based on silicon carbide (SiC) and gallium nitride (GaN) materials are a major topic of discussion at the power electronics conferences and have been so for many years. The papers presented on these devices may address issues relating to device characterization and modeling, but more often focus on the details of their application in various power converter designs.

However, there are many additional layers of research on materials, device structures, and methods of device fabrication underlying the development of these WBG power semiconductors. Moreover, the universities and other research institutions that are doing this work are not only working to advance the state of the art in SiC- and GaN-based devices, but are also striving to develop the next generations of power devices based on new semiconductor materials.

Attending the recent edition of the International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH, held May 19-22, 2025 at the Hilton New Orleans Riverside) offered me an introduction to the design and fabrication of power devices based on materials such as aluminum nitride and gallium oxide. With even larger bandgaps than SiC and GaN, these new compound semiconductor materials hold the promise of even greater performance for power semiconductors.

This conference also presented advances in the design and fabrication of GaN power semiconductors, particularly the development of higher-voltage vertical GaN devices and lateral HEMTs. CS Mantech presented two sessions on power devices and those talks are the subject of this article.

However, the program was broader than power, and also featured sessions on other optoelectronics, lasers and RF devices based on compound semiconductors. Still other sessions addressed manufacturing challenges, substrates and materials, and packaging. With regard to materials, one session was devoted to gallium oxide. On the packaging front, the subject of heterogenous integration, which has been popular at many electronics conferences, had a dedicated session here.

Moving away from the purely technical, a series of presentations introduced attendees to the activities of the Microelectronic Commons—a U.S.-based national network of regional prototyping innovation "hubs". This organization is meant to reduce the U.S.'s reliance on foreign sources of microelectronics and protect the country from supply chain risks.

The Microelectronic Commons collectively addresses the following technology areas: 5G/6G technology, AI hardware, commercial lead-ahead technologies (CLAWs), electromagnetic warfare, secure edge computing/internet of things, and quantum technology. However, the hubs will focus on certain of these topics based on their regional strengths. For example, one of the hubs relevant to this conference and to the power electronics area is the Commercial Lead Ahead for Wide-bandgap Semiconductors (CLAWS) which is based at NC State. For more information, see the Microelectronic Commons website.

As at other conferences, plenary talks offered some higher-level discussions on what's happening in a particular area. For example, Huili Grace Xing's plenary, "AlN and Ga2O3: Materials of the Future or Reality," discussed the findings of her research group at Cornell over the past decade and the potential future of these two material systems that hold promise for power and other devices. Although the papers for most of the presentations cited in this article are available on the conference website, only the abstract is posted for Xing's plenary.

However, Xing points to a few earlier publications offering similar information on the work she discussed, "How to Unleash Power of Ga2O3?," Unleashing the promise of gallium oxide," "β-Gallium oxide power electronics "and "Next generation electronics on the ultrawide-bandgap aluminum nitride platform". For future reference, there's also a paper under review on "XHEMTs on Ultrawide Bandgap Single-Crystal AlN Substrates". These papers can provide further perspective on the work discussed below from the CS MANTECH Power Device sessions.

The following is a summary of the presentations in the two sessions on Power Devices. The papers for these talks are available on the conference website in the 2025 digests section. See Session 2A: Power Devices I and Session 3A: Power Devices II. The links for the papers will also be provided individually as each is discussed.

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Note that in addition to the extensive conference program, CS Mantech featured an exhibition with vendors offering a range of equipment, software, and services for compound semiconductor manufacturing. You'll find a listing of the 2025 exhibitors here.

Power Devices I

Paper 2A1: "Practical N-Type Doping in AlN for Power Electronics"

by C. E. Quiñones1, P. Bagheri1, D. Khachariya2, S. Rathkanthiwar1, R. Kirste2, P. Reddy2, S. Mita2, E. Kohn1, R. Collazo1, Z. Sitar1,2

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Presented by Ramon Collazo of North Carolina State University.

As noted in the paper by C. E. Quiñones and others, "Aluminum Nitride (AlN) is an attractive material for extreme environment capable kV-class power devices due to its ultra-wide bandgap, high breakdown field, high thermal conductivity, and temperature stability." In his presentation on this work, co-author Ramon Collazo elaborated on some of these benefits, noting a bandgap of approx. 6.1 eV for AlN (versus 3.4 eV for GaN), a breakdown field of >15 MV/cm (vs 3.3 MV/cm for GaN) and a thermal conductivity of 3.4 W/cm•K.

However, one of the challenges in implementing a power device based on this material is control of n-type doping. The challenge, said Collazo, is "managing point defects to extend the doping limits."

In his presentation, Collazo discussed the techniques available for managing point defects in nitrides and how his team applied these methods in Si-doped AlN to achieve sufficient levels of doping (mid-10^{17} cm^{-3}). He also covered details of device design to fabricate Schottky barrier diodes demonstrating state-of-the-art performance in AlN.

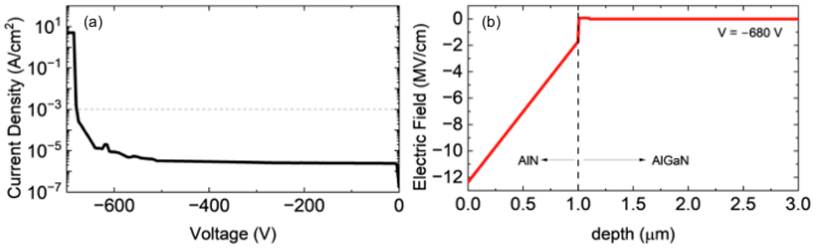

Fig. 4. (a) Reverse bias I-V of the fabricated AlN SBD showing a breakdown voltage at V = -680 V (b) Simulated electric field profile at the experimental breakdown voltage showing a maximum field electric field of 12.3 MV/cm.

(Courtesy of CS MANTECH)

As noted in the paper, this performance included "high current density (>3 kA/cm^2), low differential on-resistance (<1 mΩ•cm^2) and high breakdown voltage (680 V)." Collazo observed that this work "shows the practicality of AlN for power devices" though other challenges still remain such as the need to manage interfaces and ohmic concepts.

For more information, see paper 2A.1.

Paper 2A2: "Vertical GaN Trench MOSFETs with HfO2/Al2O3 Layered Gate Dielectric"

by E. Brusaterra1, E. Bahat Treidel1, P. Paul1, I. Ostermay1, F. Brunner1, and O. Hilt1

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Presented by Enrico Brusaterra of Ferdinand-Braun-Institut.

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Vertical GaN MOSFETs continue to be the subject of R&D because of several performance advantages they offer for power applications versus lateral GaN HEMTs. As the paper notes, these include a higher breakdown voltage and on-state current density for a given chip size, reduced thermal impedance and reduced specific on-state resistance". For these devices, the trench structure is being studied because it "owns the advantage of one epitaxial growth step, intrinsic normally-off nature and low gate currents" versus planar devices.

Brusaterra offers some additional reasons for focusing on trench. There the "lack of implantation and activation of Mg and lack of high-resolution processes, which are more time consuming and expensive. These two advantages are critical when comparing trench MOSFETs to other vertical architectures."

However, requirements for the gate oxide are more demanding than for planar structures. As the paper notes "it requires a robust gate dielectric to allow for channel inversion and for good transport properties close to the semiconductor dielectric interface[2]. Furthermore, the gate insulator has to be deposited on the etched sidewalls of the trench. A gate oxide deposited on such "etch-damaged" surfaces can lead to distortion of the space charge region preventing channel inversion which makes it harder to achieve the same performances as with planar gate devices."

Brusaterra adds, "Poor sidewall surface can also lead to early breakdown of the device due to point defects and electric field crowding, as well as increasing the threshold voltage instability during operation."

A number of gate dielectric materials are being investigated. Among them HfO2 is of interest because of its high dielectric constant and high band offset relative to GaN.

This work studied the use of a "gate dielectric consisting of a layered oxide of HfO_2 and Al_2O_3" and the devices produced using this gate dielectric were compared with previously produced vertical GaN trench MOSFETs using only Al_2O_3. As Brusaterra explains, the comparison against Al_2O_3 reflects its popularity in research rather than commercial use.

"Currently there are two main options: For production SiO_2 is preferred due to the higher throughput of LPCVD machines. For research Al_2O_3 is the standard since it can be deposited with ALD [atomic layer deposition] and [because] it's a well-known high k dielectric," says Brusaterra.

The paper discusses the design and fabrication of the MOSFETs using the novel layered dielectric, presents experimental results from these devices and compares these results with those using the Al_2O_3-only dielectric.

TABLE I
ELECTRICAL PARAMETERS OF THE TWO DIELECTRIC VARIATIONS UNDER INVESTIGATION

Dielectric	Breakdown Electric Field (MV/cm)	Relative Dielectric Constant ε_r (-)	Interface States Density (cm^{-2})
Al_2O_3	6.00	7.6	3.22×10^{12}
HfO_2 / Al_2O_3	6.52	12.8	4.19×10^{12}

(Courtesy of CS MANTECH)

As the paper summarizes, "The transistors incorporating the HO_2/Al_2O_3 layered gate dielectric exhibited up to three times increase in forward current, five times enhancement in gate breakdown voltage and significantly reduced threshold voltage shift induced by gate forward voltage stress, relative to devices with an Al_2O_3-only gate dielectric. Furthermore, the improved gate structure resulted in higher channel mobility (~11.1 cm^2/Vs

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[vs. 0.65 cm^2/Vs for Al_2O_3-only]) and a reduced on-state resistance (3.1 ± 0.6 mΩ·cm² [vs 10.4 ± 1.9 mΩ cm^2 for Al_2O_3-only]).” The reasons for the performance improvements are analyzed in the paper.

When asked about the implications of this work for future development of practical vertical GaN devices for power electronics design, Brusaterra observes that “devices with the new gate dielectric show much lower on-state resistance degradation during HV switching, which is a big problem for lateral GaN HEMT”.

For more information, see paper 2A.2.

Paper 2A3: “1700 V Breakdown Monolithic Bidirectional GaN/AlGaN MISHEMTs with a Thin Buffer Grown on SiC Substrate”

by Fouad Benkhelifa1, Stefano Leone1, Richard Reiner1, Michael Basler1, Heiko Czap1, Daniel Grieshaber1, Lutz Kirste1, Frank Bernhardt1, Stefan Moench1,2 and Ruediger Quay1,3

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Presented by Fouad Benkhelifa of the Fraunhofer Institute.

Discussing the evolution of power grid from centralized structure of today to distributed power sources in the future, Benkhelifa noted the need for bidirectional power converters to support them and high-voltage devices (perhaps with BV up to 2500 V) to implement these converters. While commercially available lateral GaN HEMTs have mainly been limited to 650-V breakdown voltages, Power Integrations’ commercialization of a GaN-on-sapphire device with a 1700-V breakdown voltage within an offline switcher IC suggests that lateral GaN HEMTs are suitable for higher-voltage applications.

Moreover, GaN is suitable to bidirectional power flow as noted in the paper, because of its “high-mobility lateral 2-dimensional gas (2DEG) current, and lack of a body diode, facilitating symmetric bidirectional current flow”. Moreover, “the implementation of GaN monolithic bidirectional switches will allow for higher power capabilities, more compact circuit topologies, and smaller, more efficient power conversion systems”.

In this work, the researchers fabricated “GaN-based discrete and monolithic bidirectional metal insulator semiconductor high electron mobility transistors (MISHEMTs). The transistors were fabricated on a thin (< 0.5 μm) GaN buffer grown on a highly isolated SiC substrate.” The structure of the bidirectional MISHEMT, which is a normally on device, is shown in the figure.

The bidirectional MISHEMT integrates two individual MISHEMTs with shared drift region and improved sheet resistance compared to two discrete devices, for bidirectional current flow and bidirectional blocking capability. The discrete, unidirectional MISHEMT served as a point of reference in evaluating the on-state resistance of the monolithic BDS. Both devices had a 1-mm gate length. In addition, a MISHEMT device with 147-mm gate width was constructed to test higher current capability.

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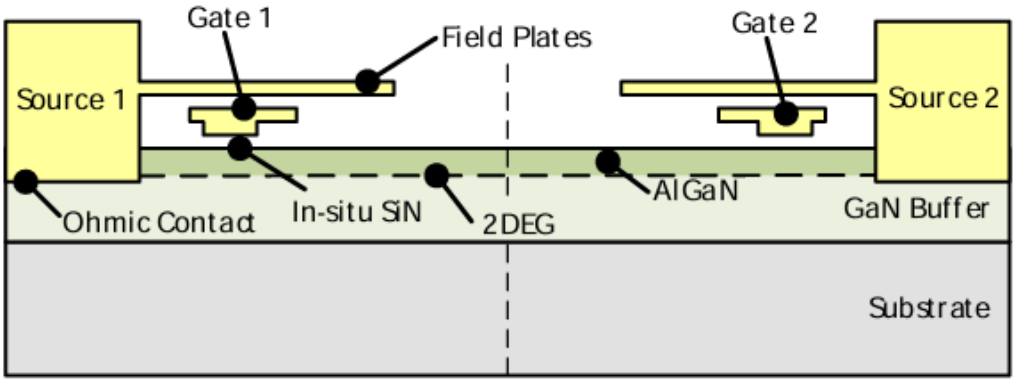

Fig. 1. Schematic cross-section view of the monolithic bidirectional GaN-based MISHEMT, with gate and source connected field plate

(Courtesy of CS MANTECH)

They then tested the dc characteristics of these devices including the high-voltage blocking and leakage current performance. Among the findings in this paper:

"The association of a thin (< 0.5 μm) GaN buffer and an isolated substrate is not a hurdle to get transistors achieving a high breakdown voltage and low leakage currents." As the paper states, when the buffer isolation of the epi-wafer was evaluated with ohmic contacts separated by different distances, it was determined that "The thin buffer is able to sustain an isolation voltage higher than 2800 V at a leakage current lower than 1 μA/mm, for a 25-μm separation structure."

For the monolithic bidirectional switch, "a bidirectional blocking voltage above 1700 V [was] achieved. The I_{DS} and I_G currents were lower than 50 nA/mm and 600 pA/mm, [respectively], before reaching physical destruction". Specific on resistance was 4.4 mΩ·cm^2 for the bidirectional MISHEMT versus 2.7 mΩ·cm^2 for the unidirectional MISHEMT. Furthermore, the bidirectional device had "a high Baliga figure of merit of 1.2 GW/cm^2."

Although the device in question was normally on, the authors suggested that similar results could be obtained with normally off devices, and while SiC was used as the isolating substrate here, other highly isolating substrates such as sapphire, AlN, and QST could also be used [see my summary on the imec paper for more on GaN devices using QST].

While the switching performance of the experimental devices has yet to be tested, the authors concluded "This work will enable us to pave the way [in] developing high voltage classes discrete, bidirectional and monolithic integrated power ICs devices, grown on highly isolating X-substrates and based on thin buffers for cost reduction."

For more information, see paper 2A.3. In addition to the work discussed in this paper, in April, the Fraunhofer Institute announced a bidirectional 1200-V GaN switch with integrated free-wheeling diodes. For more on this device, see the announcement or the paper presented at the recent PCIM conference.

Paper 2A4: "The Effect of Operating Temperature on the On-State Performance of Quasi-Vertical Gallium Nitride MOSFETs"

by Jon Evans1, Finn Monaghan1, Rob Harper2, Andrew Withey3, Camille Colombier4, Matt Elwin1, Mike Jennings1

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Presented by Jon Evans of Swansea University.

In introducing this talk, Jon Evans noted the main motivation for building vertical GaN power transistors—"to make breakdown voltage independent of chip area." Vertical GaN MOSFETs also have the advantage of being normally off devices and therefore relatively easy to drive. However, there are obstacles to manufacturing vertical GaN devices, which account for their rarity in the marketplace.

As Evans observed, there's a limited supply of GaN substrates (making them expensive), difficulties growing epitaxy on non-GaN substrates, and thermal management issues as GaN is less thermally conductive than silicon carbide.

This paper addresses all three issues by investigating the performance of quasi-vertical GaN MOSFETs built on SiC substrates. After describing the structure of the devices being studied and how they were fabricated, the paper discusses the changes in transfer characteristics of the devices over temperature, relating this to non-monotonic shifts in threshold voltage, transconductance and on-resistance, and the causes of these shifts in terms of device characteristics are discussed. A series resistances model was used to study the contributions of different structural components to the temperature dependence of $R_{DS(ON)}$.

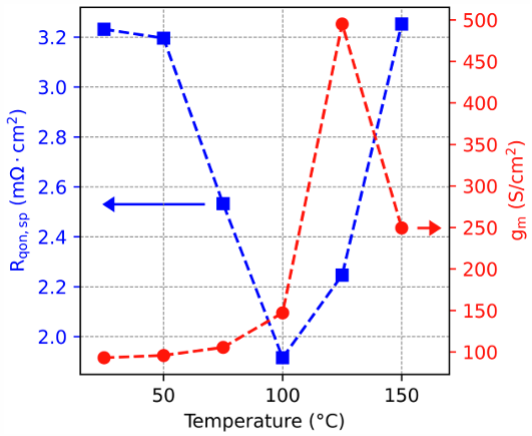

Fig. 3. Specific quasi-on-resistance and trans-conductance (both extracted at the point of maximum dI_d/dV_{gs}) shown as a function of temperature.

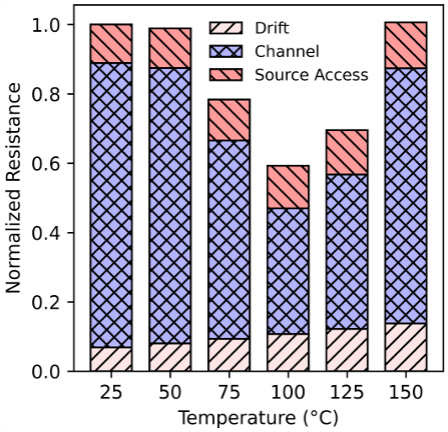

Fig. 5. Estimated resistance components for the drift layer, channel and source access regions, normalized to total on-resistance at 25°C.

(Courtesy of CS MANTECH)

As Evans noted, "channel resistance dominates across the temperature range". In the conclusion, the paper explains that "trapping behavior at or close to the MOS interface [was] likely responsible for the significant shifts in both threshold voltage and transconductance". The paper adds that "slow turn-on in the subthreshold region also indicates mitigation of interface traps is required to improve performance."

As Evans observed, optimization of materials and the gate module will be needed to address this issue.

For more information, see paper 2A.4.

Papers From Power Devices II

Paper 3A1: "Wide Bandgap Power Switches (GaN HEMT and SiC Power MOSFETs) for Hard and Soft-Switching Applications, a Long-Term Perspective"

by D. Risbud1, M. Zuniga1

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Presented by Marco Zuniga of Renesas Electronics.

While most of the power device talks presented at this conference focused on device design and fabrication, and overcoming challenges in creating power devices in new WBG materials (such as gallium oxide) or still developing device types (such as vertical GaN MOSFETs), this paper, which was presented by Marco Zuniga,

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takes a different approach. It reviews the current state of the art in commercially available GaN HEMTs (d-mode and e-mode) and SiC MOSFETs, and discusses their application in power circuits.

For experienced power supply designers or application engineers in the power semiconductor industry, much of this material will be familiar as these devices have been on the market for years, so details of their operation and where and how they are used are fairly well known. However, since CS MANTECH focuses on device design and fabrication, many of the researchers who present here are not power supply circuit experts, and likely found very useful perspective on device usage and market trends in this talk.

On the other hand, this talk also highlighted some of the areas where lateral GaN power devices are beginning to challenge SiC MOSFETs such as with 650-V devices in totem-pole PFC boost circuits, and even at 900-V device ratings. As the paper notes, "Renesas has demonstrated its 900-V SuperGaN capabilities outperform an equivalent 900-V SiC MOSFET in a 6.6-kW CLLLC converter."

Among the paper's conclusions, the statement to the effect that there will be continued competition at 650 V and that SiC will continue to dominate at 1200 V seems to have some industry consensus. But as Zuniga observed, "While SiC dominates at 1200 V today, GaN HEMTs [at this voltage] have been demonstrated and may be able to compete [with SiC MOSFETs] in certain applications in the future." "Advances in epi architectures and multi 2DEG devices will lead to further convergence."

Overall, the speaker offered a fairly balanced approach in discussing the GaN versus SiC device options. "At 650 V you can use either of them—whichever works best at the system level." And while the paper and the talk shined a light on GaN becoming more competitive in the applications where SiC currently leads, Zuniga observed that "both WBG technologies are advancing toward higher breakdown voltage and lower specific on-resistance."

Nevertheless, Renesas recently announced its decision to get out of the SiC device business and focus all its efforts on GaN, building on the portfolio it has obtained through the acquisition of Transphorm. So, to the extent this talk focused on GaN's ability to challenge SiC, it seemed to be very much in line with the company's product strategy.

For more information, see paper 3A.1.

Paper 3A2: "Normally-Off N-Polar GaN/AlN Transistors with p-NiO Gate Stacks"

by C. Zhang1, Y. Yin1, P. Huang1, I. Furuhashi2, M. Pristovsek2, M. Kuball1, M. D. Smith1,

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Presented by Chengzhi Zhang of the University of Bristol.

Commercially available, enhancement-mode GaN power devices are typically lateral HEMT designs that employ a p-type gate stack to deplete the 2DEG under the gate. This turns a normally on depletion-mode transistor into a normally off enhancement device—like the silicon power MOSFETs that power supply designers are accustomed to using.

Furthermore, conventional GaN power HEMTs typically use a III-polar crystal orientation, which as the paper notes refers to the fact that "AlxGa1-xN/GaN heterostructures [are] grown along the (0001) axis ('III-polar'). The 2DEG arises at the interface due to band offsets and piezoelectric and spontaneous polarization associated with the inversion asymmetry along the c-axis in wurtzite phases of III-nitride."

But there is an alternative crystal orientation that offers potential benefits in power devices. As the paper notes "a 2DEG can be generated in *N polar structures* grown along the (000-1) axis in GaN/AlxGa1 xN structures such that the AlxGa1-xN acts as a back-barrier located below the GaN channel. This enables better control of the 2DEG channel due to improved carrier confinement, in addition to simpler Ohmic contact formation to the 2DEG due to the absence of a surface AlxGa1-xN top barrier layer."

The impact of these differences between III-polar and the N-polar crystal orientations, which are still in the research stage, becomes more apparent in terms of device-level benefits as the paper proceeds. This paper investigates the use of a p-NiO gate structure in an N-Polar GaN/AlN lateral HEMT.

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As the paper states toward the end of its introduction "p-NiO has attracted attention as a potential substitute for p-GaN in HEMT gate stacks, offering several advantages including a simpler and low-temperature synthesis process, a higher hole concentration, and a work function comparable to that of p GaN [4]. These characteristics make p-NiO a promising candidate for improving threshold voltage control and enhancing device performance in III-nitride HEMTs, setting a pathway to future commercializing of the new technology."

This article describes the design and fabrication of an n-polar GaN/AlN HEMT with a p-NiO gate stack as well as two alternative n-polar device structures—a MOS-gated HEMTs and AlN trench MOSFETs as a means of evaluating the utility of the proposed approach with the p-NiO gate stack and also the benefits of the N-polar GaN/AlN material in general for building power devices. All three devices are fabricated on a sapphire substrate.

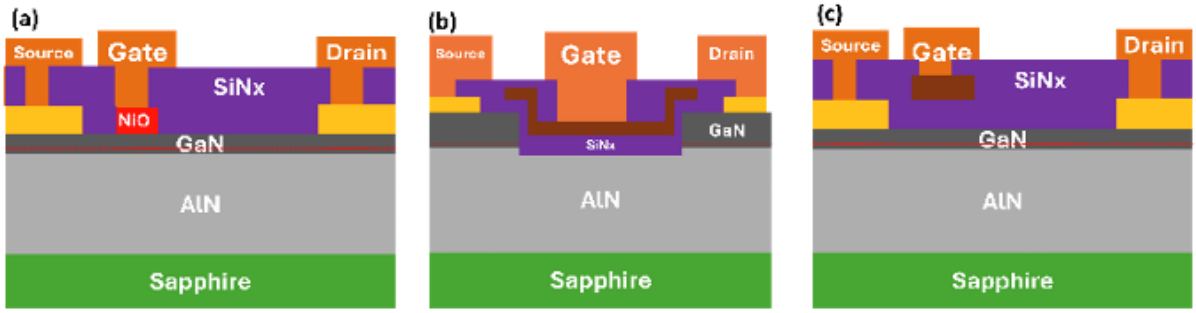

Fig. 1. Cross-section schematic of co-fabricated (a) p-NiO gated HEMT (b) Trench MOSFET and (c) MOS-HEMT.

(Courtesy of CS MANTECH)

Among its conclusions, the paper says "p NiO [gate stack] offers a promising route for fabricating normally-off N polar devices to take advantage of the strong carrier confinement compared to III-polar structures". This implies the potential for building GaN HEMTs with higher breakdown voltages and lower leakage currents than the currently available III-polar devices.

For more information, see paper 3A.2.

Paper 3A3: "Vertical GaN-on-Tungsten High Voltage pn-Diodes"

by E. Bahat Treidel1*, E. Brusaterra1, L. Deriks2, S. Danylyuk2, E. Brandl3, J. Bravin3, F. Brunner1 and O. Hilt1

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Presented by E. Bahat Treidel of Ferdinand-Braun-Institut.

Vertical GaN structures for diodes are desirable for similar reasons they are valued for GaN power transistors. Breakdown voltage and chip area can be decoupled and higher device ratings can be obtained for a given die footprint, which suggests lower cost.

However, as with vertical GaN transistors, the "natural" approach of building devices on GaN substrates is a barrier because of the small size and limited availability of GaN substrates. While the required thick GaN epitaxy can be grown on foreign substrates like silicon or sapphire to create vertical structures, the lattice and CTE mismatches between GaN and the foreign substrate materials are problematic.

This paper explores an alternative of growing GaN on sapphire and then transferring the GaN devices to a tungsten substrate, which offers lower thermal impedance. After GaN is grown on sapphire and the device structures are formed, the GaN membrane devices are detached from the sapphire using laser lift off and then bonded to a tungsten wafer. The goal is to produce a GaN diode that is fully vertical in structure and cost competitive.

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Co-author Enrico Brusaterra, adds the caveat that this "CS MANTECH paper alone does not properly address the issue of growing thick epitaxy on sapphire, which is a problem for vertical devices." But he points to a talk which his group gave at last year's conference, which addressed this subject in depth. See the paper "Wafer Bow Tuning with Stealth Laser Patterning for Vertical High Voltage Devices with Thick GaN Epitaxy on Sapphire Substrates".

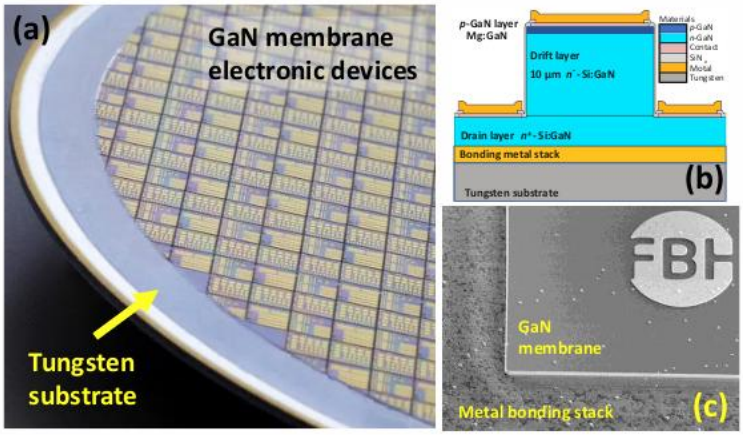

Fig. 1. (a) GaN membrane on a tungsten wafer at the final stage of processing. (b) Schematic cross-section of a GaN membrane *pn*-diode. (c) SEM micrograph of the front side of a GaN membrane bonded to a tungsten wafer.

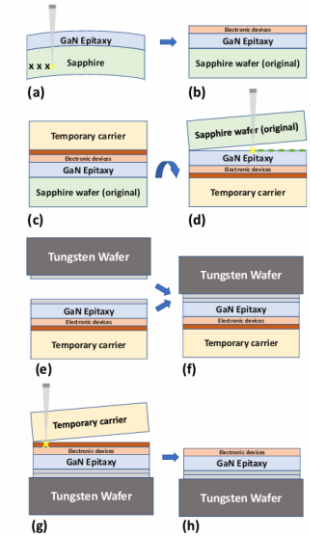

Fig. 2. Wafer's backend process flow; (a) epitaxial wafer bow reduction [5] (b) frontend electronic devices manufacturing (c) temporary DSP sapphire carrier bonding (d) GaN epitaxy membrane separation from the sapphire substrate by laser lift-off (e) GaN back side N-face ohmic contacts and bonding metal deposition (f) GaN membrane and tungsten wafer metal bonding (g) temporary carrier removal (h) final GaN membrane on tungsten substrate.

(Courtesy of CS MANTECH)

But returning to the work presented at the 2025 conference, this paper describes the many process steps required to fabricate these GaN-on-tungsten pn-diodes and then presents the measured performance for the diodes both before they are removed from the sapphire (at which point they are considered "quasi vertical" structures) and after they are mounted to the tungsten substrates (at which point they are "fully vertical" structures). Performance is also compared against existing, state-of-the-art GaN on silicon (fully vertical) and GaN on sapphire (quasi vertical).

Results were promising as the on-resistance of the pn diodes was reduced notably after the transfer to tungsten (from 3.39 ± 0.23 mΩ cm^2 to 1.71 ± 0.12 mΩ·cm^2), while the blocking voltage was only degraded slightly (from a median value of 1015 ± 47 V to 988 ± 57 V). The paper concludes that the high process yields and relative ease of the GaN membrane transfer suggest that this approach can be the basis for building low-cost vertical GaN pn diodes for power applications.

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When asked about the implications of this work for power electronics applications, Brusaterra explains, "We still have not tested the feasibility of packaging and system integration of tungsten chips. The different thermal dissipation requirements when compared to lateral GaN or native vertical GaN devices or even SiC devices may lead to different system solutions. More work is required, especially in collaboration with system designers."

For more information, see paper 3A.3.

Paper 3A4: High Voltage Design Strategies for Gallium Oxide Power Devices

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Presented by Nicholas Lyn Edwards of Swansea University.

With its high bandgap voltage (~4.6 V), suitability for n-type doping, and its potential for making high-quality native substrates affordable, gallium oxide holds great promise for high-voltage power semiconductors. However, as with GaN, p-type doping is a challenge, which in turn makes development of an enhancement-mode transistor challenging.

In response, researchers investigating this material as a next-generation material system are looking at alternative device structures such as the β-Ga_2O_3 FinFET described in this paper. The β refers to the beta phase of this material, chosen for its thermodynamic stability.

In this paper, the authors model the proposed β-Ga_2O_3 FiNFET, and run drift-diffusion simulations to evaluate the impact of different device parameters such as dimensions of internal structures, various material parameters, choice of dielectric materials, and others on threshold voltage with an eye to determining what's required for enhancement-mode operation.

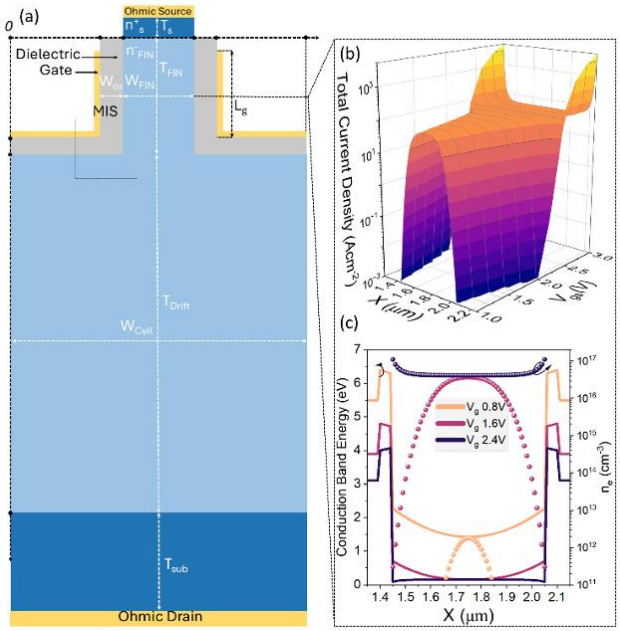

Fig. 2. (a) Shows a schematic of the simulated β-Ga_2O_3 FinFET. (b) Cutline of total current density across a 200 nm W_{FIN} increasing gate bias. (c) Conduction band energy and electron concentration across the fin during various stages of its turn-on operation at V_{ds} 5V.

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Additional simulations were run to evaluate parameters influencing failures due to drain induced barrier lowering (DIBL), with the goal of mitigating such failures. Still other simulations were performed to determine the parameters affecting breakdown voltage. Devices parameters needed to achieve a breakdown voltage of 5 kV were determined.

Since this work is preliminary to fabricating the proposed FinFET, a first step taken here was an etch development study conducted such that a "process was developed to achieve trench etching suitable for the fabrication of Ga_2O_3 FinFET devices."

For more information, see paper 3A.4.

Paper 3A.5: 1000-Hour HTRB Test on 1200 V Lateral HEMTs with Engineered p-GaN Gate

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Presented by Sujit Kumar of imec.

Commercially available lateral GaN HEMTs have made inroads at 650 V and lower voltages with enhancement-mode devices satisfying application requirements for normally off devices. At higher voltages such as 900 V and 1200 V, whether e-mode or d-mode, there have only been a limited number of devices available. One vendor has notably succeeded in incorporating a 1200-V d-mode GaN-on-sapphire power switch in its offline switcher ICs (Also see my above summary of "1700 V Breakdown Monolithic Bidirectional GaN/AlGaN MISHEMTs with a Thin Buffer Grown on SiC Substrate," for additional comments on this development from Power Integrations.)

However, for those seeking a high-voltage standalone GaN transistor that might be used, for instance, in a power converter application connecting to an 800-V bus in electric vehicles, there are only a few devices available from specialty GaN suppliers and nothing in the catalogs of the mainline power semiconductor companies. With most of the GaN devices on the market, GaN epitaxy is grown on silicon substrates, which enables them to be cost competitive with silicon MOSFETs.

Although silicon is readily available and cheap, as Sujit Kumar notes in his talk, it's a challenge to grow thick GaN layers on silicon, which is a requirement for achieving high BVs in lateral HEMTs. This paper investigates the development of a 1200-V lateral GaN HEMT fabricated on 8-inch QST substrates, which are "engineered" substrates made by Qromis.

Because these substrates, which are based on polycrystalline aluminum nitride (poly-AlN), have CTE matched to GaN, and the AlN and AlGaN materials used in buffer layers, QST substrates enable thick GaN layers to be grown on them. The QST substrates and the processes required to grow thick GaN layers on them are said to be less expensive those of the alternative substrates (silicon, SOI, sapphire, SiC and GaN). And as Kumar notes, the QST substrates are scalable to 300 mm, offering a path to lower cost devices.

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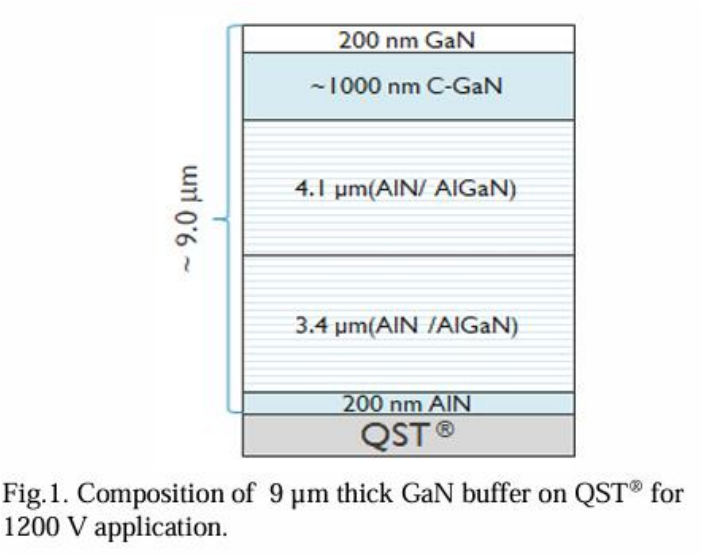

Fig.1. Composition of 9 µm thick GaN buffer on QST® for 1200 V application.

(Courtesy of CS MANTECH)

As this paper says, the architecture for this 1200-V p-GaN gate HEMT and details of how it is fabricated were given in a previous paper. This new paper advances that work, describing the doping of the p-GaN layer "by adding Si doping at the Schottky interface to improve the gate reliability and forward gate leakage [8] and re-optimizing the Mg doping profile to obtain the desired threshold voltage (V_{th}) of 2.5 V and a low $R_{on,sp}$ of 6.1 mΩ-cm^2 at 25°C."

It then presents the results of 1000-hour high temperature reverse bias (HTRB) testing to assess device reliability. The tests were conducted with two devices having two different effective gate widths. "This is one of the first demonstrations of 1000-hour HTRB test on 1200-V lateral HEMTs in the literature" says Kumar.

Among the results, the authors found no change in electrical parameters such as drain and gate leakage, and threshold voltage as a result of the 1000-hour HTRB test. However, there was a slight change in dynamic on-resistance for the DUT with the larger gate width (or field plate) and it also had a slightly lower pass rate than the device with the narrower gate width. Overall, the paper concludes, "the 9-µm thick GaN buffer show good electrical properties, and fabricated transistors show hard breakdown of ~ 1800 V."

When asked about additional work required to develop high-voltage GaN HEMTs on QST, Kumar explains the "next step is to develop technology on 300-mm QST substrates, which imec is working on."

For more information, see paper 3A.5. For background on the substrates discussed here, see "QST Platform Enables Scalable GaN Manufacturing".

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