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The Path To Radiation Hardened SiC MOSFETs And Schottkies For Space Flight

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This article will attempt to walk through the evolution of silicon carbide (SiC) power devices toward rad hard applications. The path will lead through a brief introduction to the devices, susceptibility to various radiation events, testing, work updates and a few notions on what we can do to fly SiC in space in the near and distant future with references to fundamental supporting works. This includes discussion of developments presented at the recent IEEE Nuclear & Space Radiation Effects Conference (NSREC 2025), which was held July 14-18 in Nashville.

Preamble

My lexicon is a little different than most. I've worked in sales and marketing at the vendor as the technical voice of reason. I've led with engineering excellence making inroads with top clients that monetized well into the positive on any metric. My roots are in design and R & D. I've built vertical market segments, designed the circuits, the ICs and the devices, and developed a lot of the applications. In the rad-hard (RH) world I've done much testing, validation, qualification and TID, ELDRS, SEE, proton and neutron testing in close work with the designers.

My stance regarding rad-hard silicon carbide devices is a humble one. I'm not selling a company, a solution or a component. I have no SAP dashboard to appease, no book to make. I'm not developing a business or chasing book to bill. I've done all of these roles in industrial, automotive and space products for over two decades. But alas, I've resigned those roles to join a sensational team focused on building great stuff, meeting and exceeding mission requirements and providing proper mission assurance and due diligence. I side with CV Ferro's view on reinvention. (See "The War On FAEs (Part 4)".[1])

Due to Intersil/Renesas' kindness, I was able to attend the IEEE Nuclear & Space Radiation Effects Conference (NSREC) this year in Nashville. I've attended several times before, usually giving a poster. That support enabled the latter portion of this work. The former is required to build understanding of the path to space flight adoption of SiC devices and rad hardness.

Early SiC Devices

The first SiC device launch that drew my attention was the SiC Schottky at APEC in Dallas in 2002. The parts were automotive qualified at that point.

It came at a good time. We were struggling with higher power CCM-boost-derived PFC circuits and the hard reverse recovery on the (then silicon) diode. We had to add a lot of parts to grab the I_{rr} peak, tank up E_{rr} and pump it back to the output on the next cycle. A "part-sy" solution, with a lot of parasitic interactions.

In the course of this work we learned a lot. The best lesson was that if you slew di/dt too fast during t_a in a hyper-abrupt ultrafast PN Si diode, the device fails catastrophically. The interpretation of this failure mechanism was that the depletion region can only modulate so fast due to the highly nonlinear junction capacitance and required charge.

Hyper-abrupt epitaxial designs often had a step in the capacitance vs. voltage curve due to the abrupt change in doping. When we force too fast of a di/dt, the depletion region can only short. We believed the short to occur in a small local region, perhaps near an impurity and then quickly spread to catastrophic failure. If dQ/dt is current, then the local current in this region exceeded the current density limits of the device and the short ensued. We couldn't call it punch through because the depletion region never had time to span cathode to anode and become a short.

This problem was so prolific in large PFC circuits that Unitrode designed a dual boost PFC circuit where a small pilot converter pulled the reverse recovery energy out of the main freewheel diode and zero voltage switched the main MOSFET. This was the UC3855 and it can be seen here in this datasheet.[2]

At this time, the Si diode designers were learning how to implant recombination regions in the back side of the die, control the E-field better in the EPI and make the capacitance vs. blocking voltage curve more linear. "Q-speed", "Stealth" and several other brandings came from these efforts.

Then came the SiC Schottky. A high-voltage Schottky barrier diode. It's a majority carrier device. It commutates during t_a. V_f is a little higher than the tall epitaxial Si PN diodes, with a positive tempco (the tall EPI Si diodes often had that too, bulk EPI resistance dominated the traditional negative V_f vs. temperature trend). See Fig. 1.

Yeah Baby! The reverse-recovery energy drops to nearly zero. Groovy! But then came the material nuances like dislocation defect densities, micropiping, breakdown voltage drift, limits on chip size, and lower I_{fsm} vs. I_f average in view of Si. (See reference 3.)

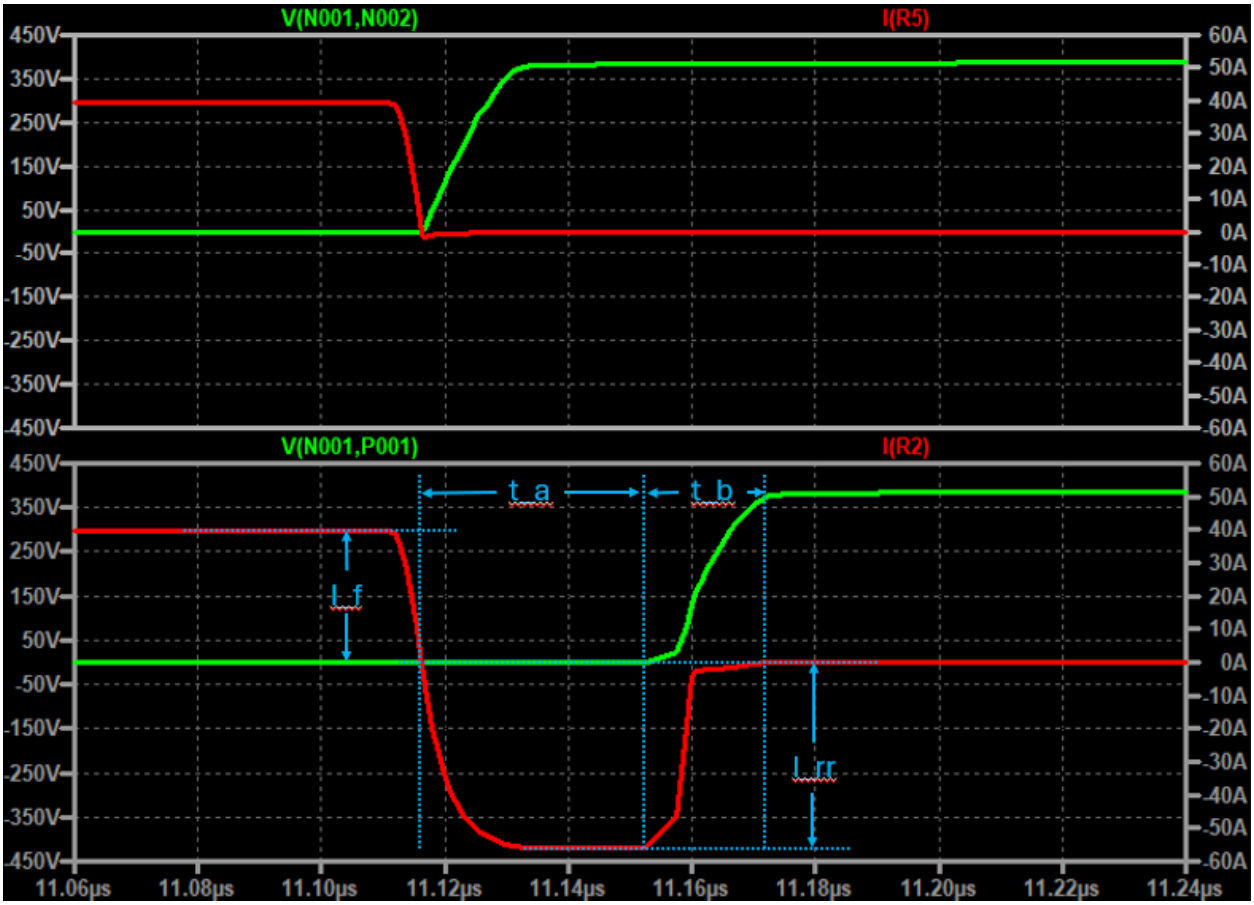

Fig. 1. Reverse-recovery waveforms. I_f = 40 A, V_{block} = 400 V. Red trace is diode current, green trace is diode voltage. Top waveforms are SiC Schottky, bottom waveforms are hyper-abrupt fast recovery Si epitaxial PN diode. SiC Schottky commutates during t_a, Si diode commutates during t_b. For epi diode, t_a ≈ 40 ns, t_b ≈ 20 ns, I_{rr} peak ≈ -55 A. SiC I_{rr} and t_a are negligible with respect to Si Epi diode.

Enter The SiC MOSFET

SiC created a lot of turmoil. Cascodes, JFETs, BJTs, and n-channel MOSFETs. When the dust settled the n-channel MOSFETs hung on with the JFETs also having much utility.

Great Scott! What a hit! The bulk $R_{DS(ON)}$ of SiC was 1% to 5% that of Si (woo hoo!). SiC can handle 10x the E-field of Si. Wow! SiC has nearly 10x higher thermal conductivity, and intrinsic temperatures well beyond what most packaging and die attach operations can handle. Awesome.

But this material was not without drawbacks. The intrinsic body diode had a high V_f and the faster commutation speeds of the devices often excited parasitic oscillations that couldn't be seen with slower Si devices.

Shortly after the SiC and gallium nitride (GaN) startup and acquisition bubble ran its course, practical solutions began popping up. The inverter comprised of field stop (FS) trench IGBTs in a module was upgraded to SiC power MOSFETs and soft-recovery Si FREDs to have lower conduction loss than the high V_f intrinsic body diode in the SiC MOSFETs.

The SiC power module began to proliferate in higher end, high reliability applications that were willing to pay for the extra efficiency, weight reduction, and space claim reduction. The big kickstart came with more electric aircraft (MEA) initiatives and funding. These were good times, but the new modules were not without problems. Faster devices in traditional 2D substrate module designs gave rise to lots of oscillations. (See reference 4).

The really good RF designers will speak of 3D substrates and having to go vertical to minimize parasitic inductance and stray capacitance. They will prove the notion with HFSS simulations and technology shifts. It's a secret, but RF and power electronics at these speeds are one and the same. Fast switching with WBG power switches is a microwave problem that resides most everywhere *but* 50 ohms. If we are to truly exploit SiC switching speeds and other WBG device merits at larger scales in a module, a two-dimensional substrate is prohibitive. (See reference 5.)

The next problem that must be addressed is driving the SiC MOSFETs. Maximally low dynamic and static driver output impedances are needed, and a negative gate voltage is required at fast switching speeds to hold the device off during fast commutation and charge coupling into C_{iss} from C_{rss} of the device. It would seem fast and direct to drive the fast die with the fastest possible solution. The fastest way that I'm aware of to drive a gate capacitance is with a current source. However the output impedance of the current source is ideally infinite, thereby it must be clamped to be deterministic. (See reference 6).

Early Rad-Hard Consideration In SiC Devices

While the MEA learning curve was happening, cosmic neutron susceptibility of semiconductor devices came into focus. Failures were observed in traction drives in trains at high altitudes and developmental aircraft. These anomalies made the industry wonder if SiC would be any more or less immune to these events. For a reasonable review of radiation interactions in semiconductors, see "The Power Supply Designer's Guide To Radiation Effects In Power Semiconductors".[7]

Neutron displacement testing revealed that SiC MOSFETs were *rock solid* over practical neutron fluences in the 1×10^8 to 1×10^{11} particles/cm^2 range. Ordinary enhancement-mode, n-channel Si MOSFETS would show a downward threshold voltage shift at the end of neutron testing and higher drain leakage in the off state. The threshold voltage shift of SiC was negligible in comparison with Si, as was the leakage increase!

Total ionizing dose testing revealed that SiC threshold voltage drift was minimal, the leakage currents remained approximately the same, $R_{DS(ON)}$ did not degrade over fluence and the intrinsic body diode was unscathed.

However, heavy ion testing showed a glass jaw. Top engineers from NASA Glenn have publicly identified SEE as a clear impediment to the adoption of SiC MOSFETs and Schottkies for space flight. In particular, single event gate rupture (SEGR) was a huge problem in the SiC MOSFET. The MOSFET cross section shown in Fig. 2 will see an SEGR failure at the bottoms of the trench, in the drift region.

The same high E-field that makes the device perform better than Si is a demerit when a heavy ion passes through the gate oxide and the area under it when the device is in the off condition. The gate is at negative voltage, the drain is at high positive voltage, the E-field between them is high, with a sharp gradient. An ionizing path can easily damage that structure.

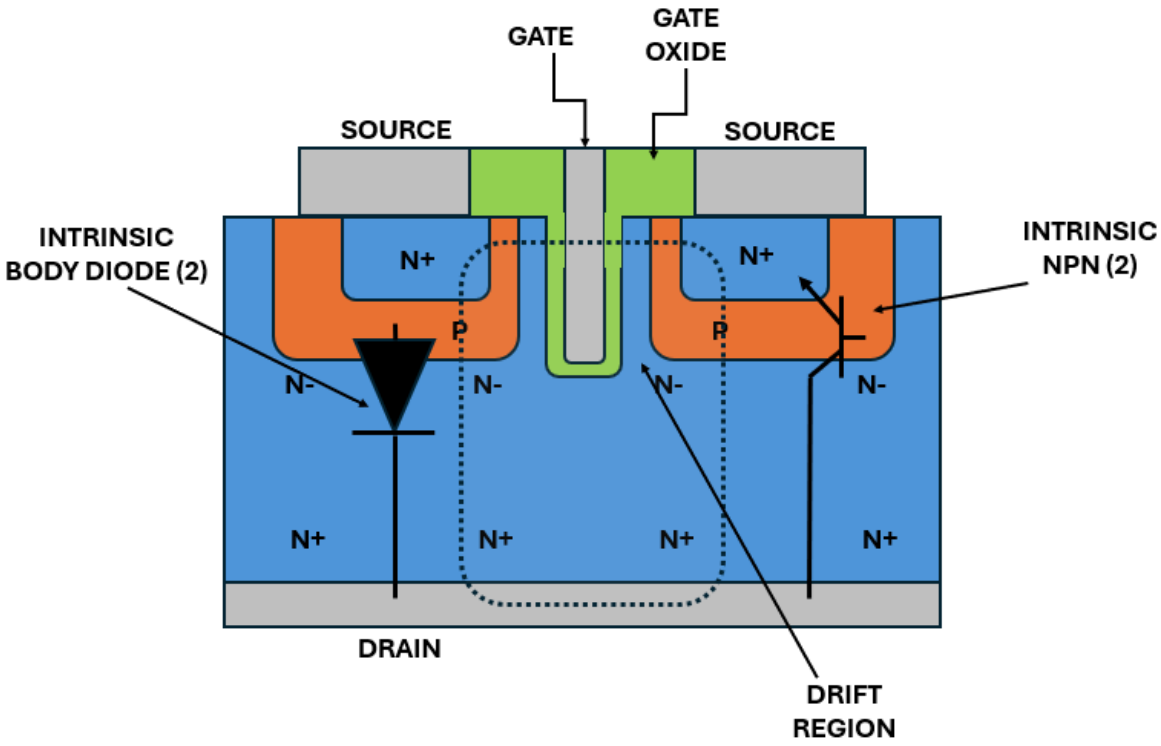

Fig. 2. Vertical MOSFET cross section (trench). Note the intrinsic body diode between the lower p-well and the drain and the intrinsic NPN with its BE junction shorted by the top-side metalization. The depletion region for the intrinsic NPN is adjacent to the MOSFET channel drift region.

The simple fix is to make the gate oxide thicker, but that requires a little consideration. Thicker oxide raises threshold voltage, increases $\pm V_{gs}$ max, lowers C_{iss} and offers a larger space for hole trapping. That's a bad tradeoff.

Hole trapping shifts V_{th} quickly. Once it drops low enough there's no more off state. This is exacerbated at high temp by the normal downward V_{th} shift. Smaller C_{iss} will also make the composite power switch more susceptible to C*dv/dt turn-on during fast commutation. The C_{rss}/C_{iss} voltage divider will offer a higher voltage to the gate and the impedance trying to hold it off.

To make the gate oxide thinner drops the threshold voltage, drops $\pm V_{gs}$ max, raises C_{iss}, raises the E-field in the vertical channel, and offers a thinner space for hole trapping. Clearly there is a sweetspot.

Update: Modern Radiation Effects In SiC MOSFETs And Schottkies

Die Geometry

As for device geometries, if we are to exploit the lowest bulk $R_{DS(ON)}$ of the SiC devices, a stripe structure is the optimal path. HEXFETs, rings, and other structures don't take full advantage of the substrate real estate *and* they often add sharp points and corners which cause E-field related problems in rad testing.

The stripe structure offers great gain structure. With W/A that large, transconductance is substantive. Desat is a (very) distant problem, however Spirito effect will likely be a concern on slow transitions or in linear mode. But SiC has much better thermal conductivity, therefore the hotspots have much better heat removal than Si.

The stripe structure also comes with some nuances. The gate runners are often thin metalized paths. The resistance of the gate runner from one end to the other is in the tens of ohms range. The cells nearest the gate pad turn on first, the ones at the end turn on nanoseconds later. When commutation speeds approach or exceed this delay line timing, the composite MOSFET may be unstable.

TID, Neutron, ELDRS

In modern SiC MOSFET and Schottky designs, gamma and neutron (displacement) radiation performance is solid. The leakage doesn't degrade, charge trapping is minimal and threshold voltage shift is small.

SEGR

The modern solution to SEGR is to redesign the gate structure for a threshold of around 4 V, and a means to inject electrons into the hole traps to offset the threshold shift. SEGR is largely remedied on these principles. But V_{gs} on must be driven high, often around 15 V to 18 V, and due to the C_{rss} size and nonlinearity, V_{gs} is usually driven to -5 V in the off state to avoid Cdv/dt turn on problems.

SEB

The remaining issues are SEB and drain leakage as per reference 8. SEB failure occurs when a heavy ion comes in and passes through the topside n well and p well, somewhere below the top-side source metalization that shorts the BE junction in the intrinsic NPN. The BE junction shorting impedance at this distance is nonzero and the NPN turns on. At this point gate-drive command means nothing and the SiC MOSFET is on. This failure is catastrophic.

Drain leakage also increases with heavy ion fluence and the effects are worse at high V_{ds} blocking voltages. Higher voltages attract more charged particles. (See reference 9.) But the increase in leakage is far less than the WBG alternative lateral p-gate GaN devices. The results of this work lean toward simply derating 1200-V SiC devices to something less than 500 V for space flight.

Savage (reference 10) introduces the notion of off-axis testing and notes SEGR response in Si MOSFETs. In most testing, the beam is normal to the die. This work introduces a "roll" angle, which is to say that the beam angle is rotated off normal, in parallel to the direction of the stripes in the structure. This action was shown to have negligible effects on SEGR performance of the die other than moving the Bragg stopping distance.

The "tilt" angle was also introduced. The tilt angle rotates the beam off normal perpendicular to the stripes in the device structure. At a high enough tilt angle, the heavy ions can pass through more than one stripe structure, provided that the Bragg stopping distance is sufficient. This was found to have detrimental effects on SEGR.

This work was pushed forward into RH SiC device design, but not without issue. Common sense would dictate that at a tilt angle well off of normal, which is to say nearly parallel to the surface of the die, the heavy ions will pass through several trenches and intrinsic NPN structures. This dramatically raises the chance of SEB. To add more space between the stripes is to reduce bulk $R_{DS(ON)}$ of the channel and hence net device value.

Protons cause similar SEB and drain leakage current although the mechanism is secondary. The incident proton collides with a Si or C nucleus and produces secondary particles that travel toward the drain. These particles can cause SEB by turning on the intrinsic NPN as well as elevated drain leakage. See reference 11.

An intensive, focused TCAD modeling paper using ECORCE shows simulated results that agree with these observations. See reference 12.

Further, Niskanen and team have shown that SEB and drain leakage counter each other over temperature. At high temp, drain leakage tends to "anneal out" or minimize, while SEB becomes more susceptible. This fits well with basic models. We know V_{be} of the NPN transistor to drop with increasing temp—that alone makes the part more susceptible to NPN turn-on at high temp. See reference 13.

A distant comparison to a lateral SiC RF MESFET shows some similarities to the above observations, indicated that the particular stripe, epitaxial structure is not at fault, rather the material has some susceptibilities. See reference 14.

The Path To Make SiC Rad Hard

Simple, Fast Solution

There is a very simple solution that is being played with SiC MOSFETs and Schottkies in LEO satellites on class D and C space missions that are shorter in duration. Derate V_{ds} of the part (V_{ka} for Schottky). To derate V_{ds} is

to control the E-field in the off state. Lower volts, lower volts per meter, lower E-field. Immunity to SEGR and SEB goes up dramatically.

Accepted derating at present state of the art is to take a 1200-V automotive-qualified SiC MOSFET and fly it as though it is a 250-V device. There are no MIL PRF 19500 slash sheets for this "meatball" derating, but if the mission is perhaps a LEO internet satellite that lasts two years, this sort of derating will suffice.

In applications like this, derated automotive parts will often be used throughout the platform and payload. I'm not aware of a space power converter relying on avalanche voltage or energy. The voltage derating shouldn't leave any voids. It's a fast path to flight but the path is lacking assurance, space and rad qualification and flight heritage.

Moderate Solution—The Rad-Hard-By-Design SiC MOSFET

But what about the big, long-haul missions like Artemis? Those will require more than meatball V_{ds} derating. Baseline requirements will be a device that is on the QPL, RLAT testing, a MIL PRF 19500 slash sheet and a lot of flight heritage. Those things won't come easy. Any good radiation-hard designer will tell you that there is no such thing as rad hard by luck. The bad designers won't be around long enough to counter the statement.

If the solution were available today in form, it would take two years to get it through complete qual with an accompanying MIL PRF 19500 slash sheet at the DLA. But SiC MOSFETs and Schottkies need to be exploited in long-haul space missions. SiC will also offer ratings well beyond that of silicon.

For example, if the dc bus to a massive Hall thruster array is 1 kV to keep copper weight down, 2200 V or 3300 V SiC power switches will likely be needed. Si has nothing like that now in rad-hard, or automotive-grade MOSFETs for that matter.

Resolve SEB Issue

The radiation-hardened SiC MOSFET recipe must resolve the SEB issue. The good news is that TCAD device simulation models are starting to converge well to measured device performance and can help with this effort minimizing shuttle lots and related processing lags. Based on my experience and what's been reported in the literature, I suggest the following steps:

- Change the doping profiles a bit in the epi design and take some gain away from the intrinsic NPN by not doping the source n-well junction as heavily. The p-body isn't usually heavily doped, but the topside n-well is. I believe this would also require decreasing the doping in the backside of the die (drain) to keep the charges balanced. The composite effort would surely demerit $R_{DS(ON)}$, but some $R_{DS(ON)}$ could be traded for improved SEB immunity.

- Change the depth of the p- and n-well to keep them a little closer to the source metalization that shorts the n- and p-well on the top side. Again, this comes with similar channel and $R_{DS(ON)}$ impact. The gate can't modulate as much of the channel cross section, $R_{DS(ON)}$ will go up.

- Use superjunction technology with carefully controlled E-field. Liu and team referenced using "buffer regions" in the epi design to improve SEB performance in vertical Si MOSFETs. These buffer regions were additional EPI layers, before the superjunction technology came into play. Liu and team also correlated avalanche voltage to SEB performance. (See reference 15.) Avalanche can be easily measured and sorted in production testing at dc. The parts with higher avalanche voltage are more immune to SEB.

  From an alternate stance, if we reflect on the old device physics book(s), they will show the width of the depletion region at reverse bias as:

$$W_D = \sqrt[2]{\left(\frac{2\varepsilon_{SiC}}{q}\right)\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_b)}$$

where

$$W_D = width\ of\ depletion\ region\ (m)$$

$$\varepsilon_{SiC} = permittivity\ of\ SiC\ material (F/m)$$

$$q = charge\ of\ one\ electron\ (Coulombs)$$

$$N_A = acceptor\ doping\ level\ \left(\frac{particles}{m^3}\right)$$

$$N_D = donor\ doping\ level\ \left(\frac{particles}{m^3}\right)$$

$$V_0 = blocking\ voltage\ (V)$$

$$V_B = intrinsic\ barrier\ voltage\ (V)$$

The notion is that a higher acceptor doping level (in the p-well) will make for a narrower depletion region. The critical field in the narrower depletion region happens at a lower voltage. We can measure that! It's V_{bds}! The BE junction of the intrinsic NPN is on the top side, the drift region of the intrinsic body diode spans the same p-well to the drain termination. The breakdown voltage measurement looks through the drain into the source.

If the p-well in the source has excessive doping (that is, lots of gain in the intrinsic NPN), then breakdown occurs at a lower voltage in the body-diode depletion region. Higher drain-source breakdown voltage for a given process proportions to higher SEB immunity.

- Exploit superjunction features to offer a lower shorting resistance in the buried BE junction that is further from the topside metal short.

- Criss cross heavy, low-resistance gate metalization in multiple layers. Commutation speeds are approaching the delay line timing of the gate runners from one side of the die to the other. At this point the device may be unstable. Delay line timing must be reduced to support faster commutation timing. If gate metalization were to "criss cross" with second-layer metalization over the primary layer running perpendicular to the stripes, the internal cell-to-cell delays would drop. Compared to the substrate, metal layers are cheap and easy. There's no reason this can't be done.

- Restructure the device cell geometries and give up a little $R_{DS(ON)}$ for symmetrical, central gate distribution. Let the geometries have radiused corners and minimal E-field gradient. This will make the SiC power switch look more like an RF power transistor. But the RF designers knew stuff too, and their devices perform well in SEE testing. A symmetrical structure would get all of the gate signals to all of the cells at about the same time. This makes for a more stable device in general. But the bulk $R_{DS(ON)}$ will be much higher than that of a stripe die layout.

Change The Device

Walking around NSREC 2025 I ran into a few GaN authorities including Jim Brandt and Bel Lazar. Jim gave a great poster on the angle of incidence in the heavy-ion beam having varying impact on SEE performance in RH GaN.[16] In these discussions, it was clear that the rad-hard lateral p-gate GaN devices are doing well. Why not build a similar structure in SiC?

It's a new game with new nuances, but if we could build a p-gate structure, with no gate oxide, the primary hole trapping mechanism vanishes, as does the intrinsic NPN. This notion comes with material science challenges. GaN, 2deg and AlGaN have been engineered to work well together. SiC has not gone down this path.

There are SiC JFETs out there designed for normally on E-fuse applications. Perhaps that technology could be spun?

Disruptive Technology

The disruptive solution is to change the structure. Samuel Anderson at ICEMOS has demonstrated a dazzling means to this end. As he states "I put the wide bandgap material where it is needed". That statement on its

own is ambiguous and inviting. How does he get that to work? Is it yet another four-terminal cascode like switched emitter or GaN HEMT-over-Si MOSFET?

No, it isn't. Sam has taken a unique stance on vertical MOSFET design. The fundamental notion is that of a "taller superjunction MOSFET" where the epi layer is grown very tall in a novel process beyond that of standard superjunction technologies. This allows the gate to modulate more of the channel and further reduce $R_{DS(ON)}$ in the Si. This can be accomplished *with negligible C_{rss} or C_{oss} addition in a vertical structure.*

This is a brilliant idea that furthers the utility of Si MOSFETs. The processing and material science of this solution varies. It is well guarded and positively brilliant. More information on IceMOS devices can be found in reference 17.

IceMOS added an astonishing addition to this tall epitaxial silicon MOSFET. Sam put the wide-bandgap material where it was needed. Not in the gate, source or upper part of the channel that is sensitive to SEGR, SEB and other heavy ion events, but rather in the drain.[18]

I can only describe this solution as magic. The implementation is comprised of brilliant material science and manufacturing techniques. Sam's solution is to augment the drain of the tall Epi Si superjunction MOSFET with SiC material. In this modality, the SiC material only blocks drain voltage. The high E-field is applied from the Si/SiC drain interface to the termination on the bottom of the SiC augmentation. The SEB and SEGR problems of stripefet SiC MOSFETs are no longer in play.

But this isn't perfect. The game is to provide lowest $R_{DS(ON)}$ and highest V_{ds} in smallest package. The structure of the very tall EPI Si MOSFET can be designed and terminated to withstand higher LET and or higher Bragg distances, but it will still require a stripe technology to terminate the gates, and no designer in their right mind would put the gate termination in the middle of the die to unify the delay distribution.

This is because bond over active is a bad idea. The stress from terminating the bond wire would change the performance of the active die area under it. We can't have an island in the middle of our die—it gives up too much $R_{DS(ON)}$. So the gates will likely remain terminated off in a corner and the same gate runner delay problem will march forward.

The IceMOS Si-on-SiC power MOSFET is expected to do well in neutron, gamma, heavy ion, proton and prompt dose testing. Hopefully, there will be no traps or issues in the Si/SiC interface.

A Few Words On SiC Schottkies

There hasn't been as much fuss about power diodes because it's not an issue as yet in the RH power design community. However, the issues are coming. Manufacturers of RH diodes have been shuffling fabs and processes. Many of the old RH Si technologies were produced on small wafers that just don't lend themselves to modern mega fab processing techniques. How does one mount a 2-inch wafer on a 10-inch vacuum chuck for dicing? The untiring dashboard droid only takes this to mean that the old fabs are too expensive and must be shut down.

I've now seen several instances where the "new diodes" from the "new fab" bearing the same part number and DLA slash sheet as the old diode fail in circuit, 100% of the time, where the old diodes worked great. We've found that E_{rr}, Q_{rr}, I_{rr} went up dramatically with the fab transfer. Switching loss in our application is now 5x higher with the new parts and they run away and fail 100%. The dashboard at the landfill might monetize that as a success, but neither the vendor or the client are doing well with it.

SiC has a future here as well. A SiC Schottky commutates during t_a. There are no large switching losses to consider, no recombination mechanisms to design. The one fault with a SiC Schottky is that if there is a surge and the Schottky is forward biased hard enough to make V_f of the Schottky structure large enough to bias the guard ring, there is then a PN junction on in parallel with the Schottky structure and reverse recovery mechanisms apply. But in SiC this is much faster than Si and the energy levels are lower for the same data sheet voltage and current ratings in view of Si PN junction ultrafast, soft reverse recovery parts.

The main failure mechanism in a SiC Schottky diode again relates to E-field and heavy ion interactions. I've not seen instability in TID, ELDRS or neutron data, but SEB is a problem with heavy ions. The same solution for MOSFETs holds true for Schottkies, back off on the E-field and SEB problems can be mitigated. Perhaps some of the tricks used to make the SiC MOSFET rad hard could be applied to the SiC Schottky diode.

We can't discuss rad-hard SiC MOSFETs and Schottkies without mentioning the distant cousin, that of GaN. The p-gate, Schottky gate, lateral GaN power MOSFET is doing well in space applications. EPC has an outstanding grasp on the fundamentals, susceptibilities and mitigation. The EPC team has slash sheets with the DLA and fully qualified parts used in many missions.

But the lateral structure is not without issue or limitation. I don't see a lateral MOSFET having the ability to block voltages much higher than 1 kV in the next decade. The main nuance is the leakage current in the off state. The distance between the "typical" column in the datasheet and the "max" column is tens of dB. Off state leakage current can be high.

Discussions around the matter show that there is a temp dependency related to some charge trapping. At low temp, there isn't enough energy to trap charge, at high temp there is enough energy to kick out the trapped charge. The "worst temp" for leakage current was in the 40°C to 80°C junction temperature range.

I've not seen much work with the cascoded structure for space applications. I can imagine that the GaN HEMT is fairly immune to neutron, TID, SEE, ELDRS and proton. The weak point is likely the Si MOSFET on the bottom, but if is truly set up such that the HEMT blocks the voltage and the Si MOSFET blocks the current, the composite device should do well in SEE. The bottom FET isn't blocking high voltage, the upper HEMT does that. The only thing left on the bottom MOSFET is a current density problem and SEB.

Conclusions

When the team at JPL built Voyager 1 and Voyager 2, every circuit started out with "that's impossible". Nearly 50 years later, the systems are still working. Why? Were there SPICE models back then? Were they lucky? Was there an SAP dashboard?

No. The dedicated folks got together, tried to visualize every possible circumstance, every possible interaction, and everything that could go wrong. Then they overdesigned everything on best practice and gave their best assurance that the bird would hang on. Nearly 50 years later, it's still going.

By comparison, the NiCd batteries in my Makita 6012DWK cordless drill lasted maybe six months each in the late 80s and early 90s. The NiCd batteries in Voyager are still doing fine, nearly 50 years later.

In light of this, building an RH SiC MOSFET and Schottky is a lesser challenge, but it's still a grind. Design, test, qual, documentation, iterations. This is certainly not a 5-nm FINFET on a parent structure with 2 billion others running at 0.6 V. But without the power, if V_{cc} = 0, those FINFETs don't have much utility. This leaves the burden on us. We deliver that power! We have to make the devices and power converters that make that supply voltage.

Historically, we have to take pause and think back. When Mike Catrambone's dad started Omnirel in Leominster in 1985, the company made space and other high-reliability modules, assemblies and semiconductors. Some 25 years later, after the acquisition, IR HiRel had a wonderful business building and selling rad-hard MOSFETs. Folks like Milt Boden, Max Zafrani, Jim Brandt, Mike Thompson, Saeed Shafiyan-Rad, Jerry Dube and yours truly made wonderful contributions to those efforts leading to several generations of rad-hard MOSFETs and related parts. In that time, many other designers of zeal have said "We'll have rad hard MOSFETs in two months, it's only three terminals, what could be so difficult?" to deliver *nothing* 10 years later.

Rad-hard design is not an easy process. It's an extremely fine-tuned, wholly immersive subset of the semiconductor world that requires a lot of work and fundamental understanding. The path to a rad-hard SiC product family of MOSFETs and Schottkies will be a tough one, but it's not impossible. From a business standpoint, I believe most any principal or end user would greatly appreciate having alternative MOSFETs and diodes on their BOM in view of the ongoing vendor issues.

I thank you kindly and may your electrons continue to flow as you intended.

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About The Author

Paul Schimel currently serves as a staff engineer for Northrup Grumman in the power group. He has over 29 years of theoretical and hands-on experience in power electronics, spanning military, aerospace, automotive and industrial markets. Paul's work regularly includes rad-hard adjudication and testing, dc-dc converter design, device-level analysis, root cause analysis, failure analysis, EMI mitigation, PCB layout, control loop compensation, inverter design, transformer design, rotating machine design, bench-level measurement and validation techniques and system-level analysis/comprehension.

He has designed dc-dc converters from milliwatts to megavolt-amps, inverters to 5,000 HP. He is a licensed professional engineer (PE) and holds two FCC licenses (First Class Radiotelephone and extra class amateur). In addition, Paul holds several patents on power electronics matters.

For more on rad-hard power devices, see How2Power's Space Power section.