ISSUE: September 2025

Leveraging Special Dead-Time Control Modes To Optimize GaN-Based Buck Converter Designs

by James R. Staley, Analog Devices, Durham, N.C.

Synchronous converters operate by alternately toggling a control switch and synchronous switch device (usually a FET) on and off. The timing of this operation matters. If the delay (known as dead time) between turning one switch off and the other on is longer than necessary, efficiency suffers. If the delay is not long enough, a condition known as shoot-through can occur where massive amounts of current flow through the switch pair. This dramatically hurts efficiency and can damage components. While these considerations have been well understood for many years by power supply designers designing with silicon power MOSFETs, the dynamics change somewhat with the introduction of gallium nitride (GaN) FETs into synchronous converters.

In replacing silicon MOSFETs, GaN FETs offer higher energy density, faster switching, and lower losses due to their dramatically lower gate capacitance (C_g). GaN FETs, however, have very tight V_{GS} limits and do not have a body diode. Because of this, the reverse-conduction losses are much higher with longer dead times if the gate slew rate is lowered to avoid gate ringing.

But they are still just as subject to the deleterious effects of shoot-through. To take full advantage of these devices, dead time must therefore be optimized. This article explores the switching dynamics at play when GaN FETs are used for the power stage in synchronous buck converters and how specialized dead-time adjustment modes in two buck controllers—the LTC7891 and LTC7890—can be used to optimize dead time based on design goals for efficiency and reliability. Along the way, we'll discuss measurement techniques for making switch-node measurements as these become more challenging in the face of GaN's fast slew rates.

Switching Operation Considerations

Consider the typical application in Fig. 1. This is a 15-V to 36-V input, 12-V/15-A output stepdown converter featuring the LTC7891 synchronous stepdown controller.[1] It is designed specifically for driving GaN devices, and we will examine how to accurately measure dead time and overshoot while optimizing the gate resistor using this application circuit.

The switching network for the buck converter with smart near-zero dead time is comprised of the controller that drives control switch Q1 top gate (TG) and a synchronous switch Q2 bottom gate (BG). The top gate is driven with separate pull-up/pull-down resistors (TGUP, TGDN) and the bottom gate is driven with separate pull-up/pull-down resistors (BGUP, BGDN). Switching currents during each switch cycle are averaged with the output filter network L1 and C_{OUT} to produce a regulated output voltage.

An ideal converter would have lossless switches that turn on and off instantly in perfect unison. However, while GaN FETs are capable of being turned on and off more quickly than other technologies due to their low capacitance, there are delays between the controller commanding a switch on, and that switch reaching a fully on state. The same holds true for turning the switch off.

Because of this delay, there are transition losses that become an important part of the total losses of switching operation. These losses translate into switch heat, which hurts efficiency and ultimately imposes thermal limits of operation for the FET. But how does one practically work with these limits imposed by nonideal switches?

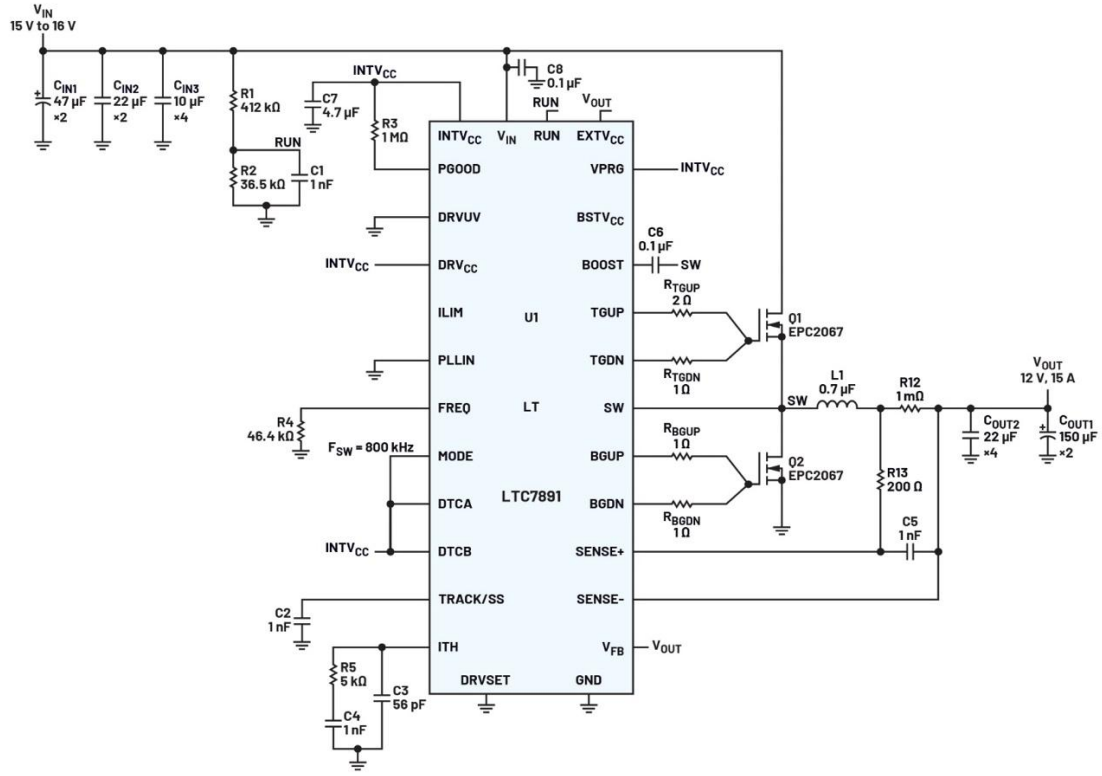

Fig. 1. An 800-kHz, 15-V to 36-V V_{IN}, 12-V V_{OUT} buck regulator providing up to 15-A output.

If both switches are fully on—even for a fraction of a second—low $R_{DS(ON)}$ means a short circuit from V_{IN} to GND, and catastrophic switch failure is the result. If both switches are partially on, high drain currents cause instantaneous high-temperature rises that stress the switches and reduce their lifetime. This condition is known as shoot-through (Fig. 2).

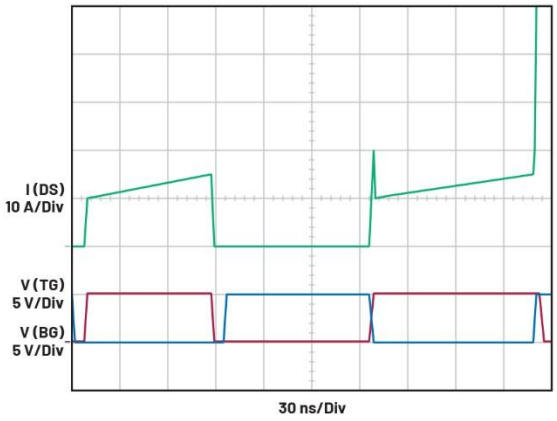

Fig. 2. Shoot-through caused by insufficient dead time,

The initial switching has roughly 8 ns of dead time and the switch current has a normal di/dt associated with switching to input current, then ramping as the inductor charges. The next transition has symmetric rising and falling edges, allowing both transistors to be partially on and resulting in a sharp spike of drain current that is still below $I_{(DS)MAX}$. The final transition allows 2 ns of on-time overlap and the drain current spikes well beyond the rated FET drain current.

To avoid this, controllers turn one switch off and then delay the turn-on of the other, which is a period known as dead time. This prevents shoot-through only if the programmed dead time is sufficient to allow the transition from completely on and off (Fig. 2). But what happens if this time is too long?

MOSFETs have a parasitic body diode that will clamp the switch node and prevent reverse breakdown while the FET is still off. This temporary $V_F \times I_{DS}$ power loss eats into efficiency the longer it takes for the FET to turn fully on and replace the (typically 0.8 V to 1.0 V) $V_F \times I_{DS}$ power loss product with the $I_{DS}^2 \times R_{DS(ON)}$ loss, which is much lower.

GaN FETs, on the other hand, do not have this body diode structure. They will clamp under reverse voltage at a much higher potential, with 2 V typical for the lateral transistor structure. This means that excessively high power losses will be incurred for even moderate dead times, making it essential for GaN FET controllers to minimize dead time.

To overcome this, MOSFET-based designs often place a Schottky diode across the synchronous switch in parallel with the MOSFET to reduce the forward voltage drop during dead time. The diode's junction capacitance, however, quickly dominates as a source of loss in the higher switching frequency applications GaN is ideal for. The tradeoffs associated with these considerations are shown in Table 1.

Table 1. Losses from 48 V to 12 V at 500-kHz switching frequency and 20-ns dead time.

	BSZ097N10NS5 MOSFET	EPC2218 GaN FET	PMEG100T030 Schottky
V_F (V)	0.9	1.5	0.7
I_D (A)	20	20	20
Reverse conduction loss (W)	0.36	0.60	0.28
Q_{RR} (nC)	60.0	0.0	9.5
Reverse recovery loss (W)	1.44	0.00	0.23

GaN-based designs are now seemingly between a proverbial rock and a hard place. Shoot-through from dead-time failure and the switches instantly evaporate; too much dead time and they could de-solder themselves right off the board. How does one determine the right balance between efficient conversion and an adequate safety margin?

Perhaps the easiest way to solve this dilemma is to choose a converter that offers smart near-zero dead times or adaptive dead time features baked into the silicon. The LTC7890[2] and LTC7891 stepdown controllers are dual-/single-buck designs that are purpose built to drive GaN FETs with pin selectable smart near-zero, adaptive, and precision resistor adjustable dead time control options. The architecture cleverly measures the actual V_{GS} and V_{SW} levels to intelligently control timing to achieve both precision and safety for any device being driven. It does this by making rapid adjustments to control a precise amount of dead time.

Instead of the traditional open-loop gate drive, the programmed dead time is adjusted on-the-fly to guarantee turn-on and turn-off occurs when the controller needs, rather than when the gate signal along with parasitic gate resistance and capacitances dictate. This minimizes the reverse conduction losses and capitalizes on the near-zero reverse recovery loss inherent to GaN. A complete guide to these modes of operation is shown in Table 2.

All that is left for the user is to verify that the programmed mode and timing are implemented correctly. However, the verification process presents challenges the designer must first overcome.

Table 2. DTC mode configuration.

Dead time control (DTC) MODE	DTCA	DTCB	Dead time (ns)
Smart Near-Zero DTC	$INTV_{CC}$		0 (typ)
Adaptive DTC	GND		20 (typ)
R_{SET} DTC	10 Ω to 200 kΩ	10 Ω to 200 kΩ	7 to 60

Measurement And Layout Considerations

Measuring the dead-time and overshoot waveforms requires careful attention to probing techniques and implementation. GaN FETs have very stringent V_{GS} constraints relative to MOSFETs—typically 5 V with +6 V to –4 V absolute max. Strong gate drive with parasitic reactive elements leads to ringing, and even brief excursions can damage GaN devices.

The GaN gate presents a lower capacitance to the drive pin than MOSFETs, which is what makes them compelling for use at higher frequencies. However, probes themselves present parasitic reactance elements that can distort the waveform and give incorrect information about what the gate sees unprobed. Holding a probe with the hand using minimal hardware can be an invitation for disaster should the hand slip. Using the traditional alligator clip lead is out of the question.

Classically, custom pigtail application probing techniques have been recommended for good scope measurements, provided the return path is properly chosen for top gate and switch nodes (Fig. 3). This still leaves the floating top gate with a problematic approach for probing. One solution is to use a connector such as the MMCX style, or header pins that will adapt to MMCX probe tips. While the bottom gate can be ground referenced, the topside gate is referenced to switch, so some form of isolated probe must be used.

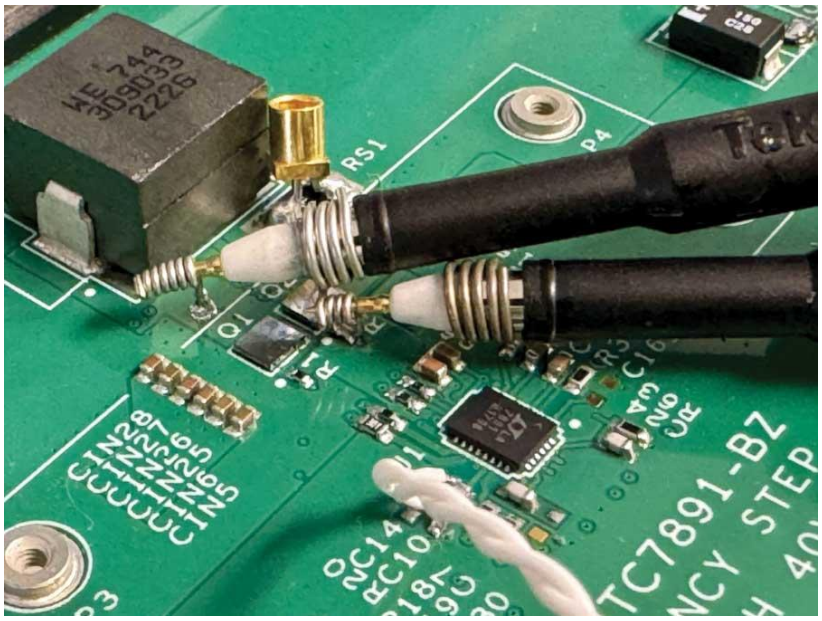

Fig. 3. Good probing technique on bottom gate and switch to minimize ringing artifacts.

Optical probes, such as the Tektronix TIVP or newer TICP, which features less drift, can provide this isolation for the top gate measurement and utilize the MMCX connector. Fig. 4 shows a typical LTC7891 dead-time measurement setup in progress with the MMCX connector directly under the FET gate pin coupled to a 1-GHz optical probe.

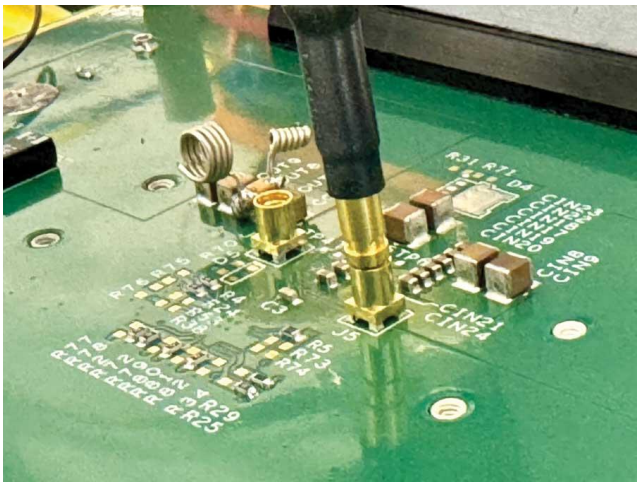

Fig. 4. Tektronix TIVP100 optical probe connected to the top gate via an MMCX connector.

The connectors themselves are a case study in compromise. Surface-mount MMCX connector placement can take up physical board space. This is a concern where very tight layouts for power density are an issue. If the connector is placed (optimally) directly across the gate and source pins of the FET without introducing additional gate trace, it may spread the layout more than desired. On the other hand, placing the connector out of the way of the layout introduces additional trace inductance and resistance that can degrade measurement accuracy.

Another alternative is the use of hole-through headers that can be populated only for measurement and then left off for the final build, but this entails using an adapter that increases parasitic elements slightly, along with creating annulus space openings on all layers in the pad stack. With the optimum balance of tradeoffs and careful attention to layout, a minimal amount of overshoot and ringing due to the probe parasitic elements can be achieved (Fig. 5).

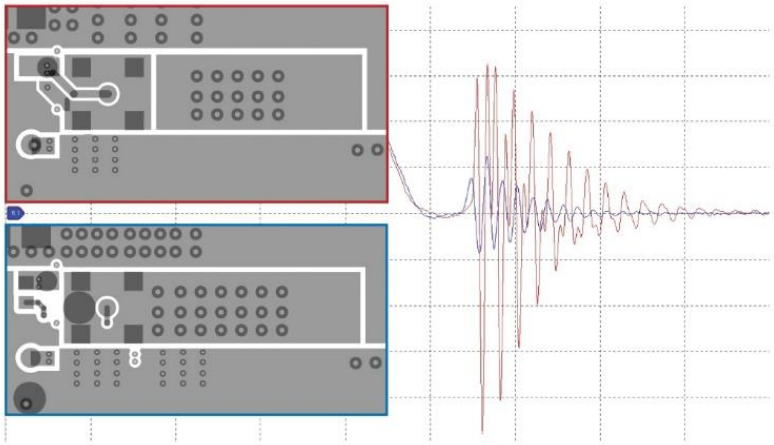

Fig. 5. Top gate turn-off waveforms showing the effect of parasitic elements in probe connection. Red: non-Kelvin connected; Blue: Kelvin connected MMCX connector. 20 ns/div, 2 V/div using the Tektronix TIVH 1-GHz optical probe.

The red outlined original layout had the MMCX connector solidly connected to the switch node and gate node connected with via and inner trace to the gate pad of the GaN FET. The red trace showed ringing exceeding +6.4 V/−9.1 V. Using the same 2.2-Ω pull-up/1.0-Ω pull-down gate resistance but modifying the blue outlined layout to separate the MMCX body from the switch node and Kelvin connect it instead, the blue trace shows +2.4 V/−1.8 V of ringing at the top gate turn-off. The key takeaway here is that even minor adjustments to the layout can have great impact on the measured overshoot figure, which is a key parameter for tuning out overshoot and ensuring that the GaN FETs are not being overdriven.

Once the measurement technique is validated, the process of verifying dead time can begin. The first step is always to ensure that whatever type of probe being used to measure the top waveform is de-skewed with respect to the bottom signal using a common signal source. Dead time is relative, so the skew of one channel with respect to the other does not matter so long as a common signal shows up without any horizontal offset.

This also allows for ensuring that any gain error and offset (common issues with optical probes) are corrected for, or at least known for, post-measurement adjustment later. Optical probes should be allowed to thermally stabilize before collecting data that is used to make decisions. It is often useful to record any gain and offset settings.

A baseline measurement at the lowest possible stress voltage and current (lower V_{IN} for buck, higher V_{IN} for boost) should be taken before pushing the limits of power on the design once the setup is completed. Gate overshoot scales as a function of input voltage and output current, so if the design is marginal, it's best to discover and correct for this before stressing any limits.

If the oscilloscope used for testing has reference cursors, it is helpful to place these at the upper and lower limits of the GaN V_G data sheet spec as a visual cue for tolerable ranges. Use the switch node waveform to trigger and overlay top and bottom gate waveforms to get the optimal picture of dead time. Ideally a differential or optical probe is used to measure top gate waveforms. If the measurement must be made with respect to ground, it is often helpful to use scope trace math functions (if available) to subtract switch node from top gate node inputs to have a virtual ground-based trace for analysis.

Proper techniques for laying out, probing, and collecting data outlined here should provide system designers with a good degree of confidence in the robustness of GaN-based designs implemented with the LTC7890 and LTC7891 stepdown controllers. Once a prototype has been set up to accurately measure the switching waveforms on the bench, the designer can choose a configuration and then optimize the gate-drive signals.

Taming The Gate Connection

To snub the peak overshoot, increase the value of the gate pull-up resistor. If the gate is slow rising and has no overshoot, this will not damage the FET, but the controller will delay turn-on or turn-off to maintain the programmed dead time, which causes increased transition losses associated with excessive gate resistance. To correct for this, decrease the gate pull-up resistor.

See Fig. 6 to understand the impact that gate resistance has on the waveform. The left set of waveforms shows gate measurements with pure PCB trace—effectively 0 Ω of pull-up and pull-down resistance on the top and bottom gates (TG and BG traces). The right set of waveforms shows 10 Ω of both the pull-up and pull-down resistance for both the top and bottom gates.

Recalling that ideal switching involves instantaneous transitions, a fast-rising waveform with a small amount of overshoot within limits over the entire input voltage and output current range is preferable to an excessively damped gate waveform. The gate falling waveform overshoot is similarly adjusted by increasing or decreasing the gate pull-down resistor.

The center set of waveforms shows a decent compromise between the overshoot associated with 0 Ω, and the excessive delays to eliminate all over/undershoot of 10 Ω. A key advantage to split pull-up/pull-down lines is the ability to tailor each resistance. Note that 2 Ω of pull-up resistance in the center trace of Fig. 6 sufficiently damps the overshoot, but as little as 1 Ω of pull-down resistance in Fig. 7 is needed to correct the undershoot shown in the top traces of both the top and bottom gates.

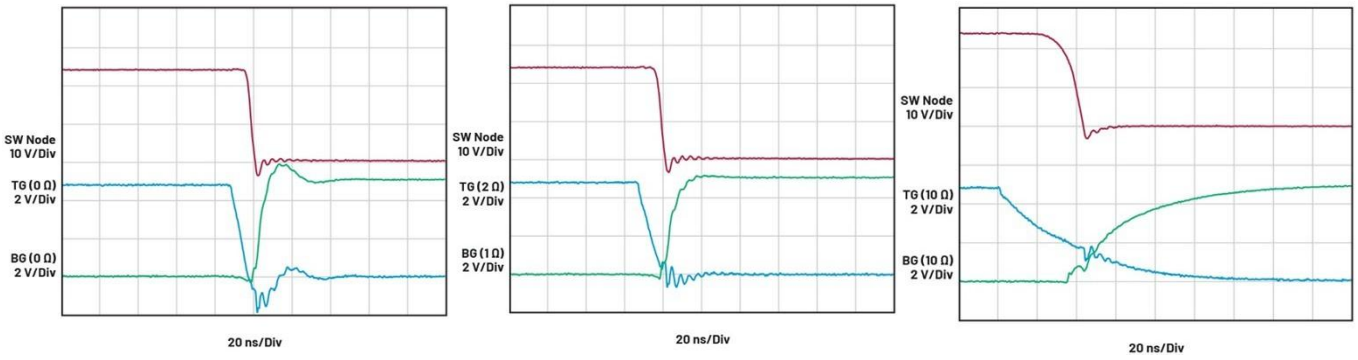

Fig. 6. The effect of series resistance on gate slew (SW rising) TG: top gate; BG: bottom gate. The left set of waveforms shows results with the PCB trace for gate connection (0 Ω). The middle set of waveforms shows optimized gate resistance. The waveforms on the right show all gates with 10 Ω in series with gate drive pins. The most critical value for the SW node rising is $R_{TGPULL-UP}$.

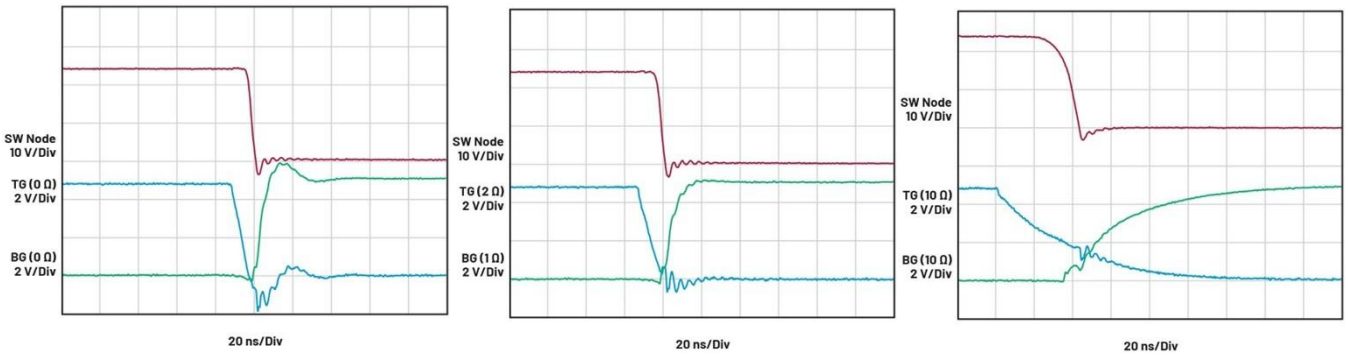

Fig. 7. The effect of series resistance on gate slew (SW falling) TG: top gate; BG: bottom gate. The left waveforms show the PCB trace for gate connection (0 Ω). The middle waveforms show the optimized gate resistance. The right waveforms show all gates with 10 Ω in series with gate drive pins. The most critical value for the SW node falling is $R_{TGPULL-DOWN}$.

Poor layout or overly conservative damping with gate resistance comes at a price. The longer the transition takes—even with near-zero dead time guaranteed from a threshold point of view—the more transition losses will eat into the efficiency budget. This is confirmed by thermal analysis using the FLIR imaging unit.

This is illustrated very dramatically in Fig. 8, which shows a near 40°C temperature rise between 0-Ω and 10- Ω resistors measured in the previous figures. This represents a loss in the available power budget before allowable thermal stress on the FETs is exceeded.

Another concern to look for with the bottom gate is phantom turn-on, which will appear to be a swell in the ringing that begins to approach threshold voltages of the bottom FET; having both FETs on is never a good thing! The LTC7890[2] and LTC7891[1] have low impedance gate drivers that help prevent this, but bottom gate pull-down resistance should be optimized with this in mind. This process of optimizing gate-drive levels ensures that the FETs will be safely switched under all conditions using smart near-zero dead time, but how should other modes or dead times be verified?

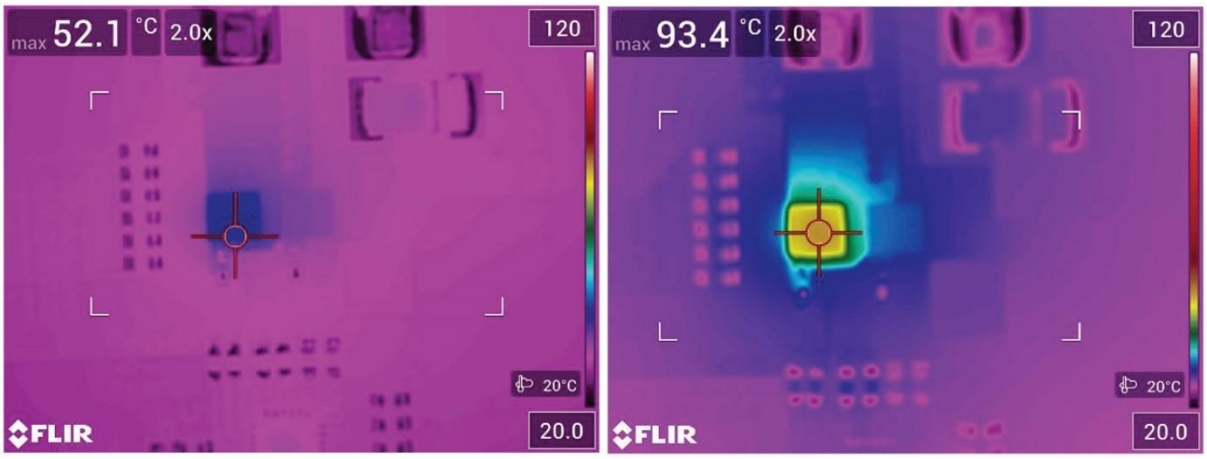

Fig. 8. Thermal capture of transition losses due to gate resistance. The left image is taken at 24-V V_{IN} and 12-V V_{OUT} at 10 A using PCB trace resistance on all gate traces, resulting in a peak temperature of 52.1°C on the top FET. The right image shows identical conditions with 10 Ω of resistance on all gate traces. The top FET increases to 93.4°C with no additional power at the output.

Choosing The Dead-Time Delay

In some cases, a designer may choose or be mandated to use a set amount of dead time. The LTC7890 and LTC7891 have three modes of dead-time control, summarized in Table 3. Smart near-zero dead time servos the appropriate gate to ensure no destructive levels of energy remain with such tight timing.

Adaptive gate-to-gate dead time uses Kelvin-sensed thresholds present at the gates themselves to servo timing to a default of 20-ns dead time. R_{SET} programmable dead time uses the same internal logic but allows a trimmed precision offset of the 20-ns value from 7 ns to 60 ns.

Note that if either adaptive or R_{SET} DTC is used, it will be necessary to set trigger thresholds at 1 V using the gate signals to verify the timing is functioning as programmed.

Table 3. DTC mode configuration.

Dead time control (DTC) mode	DTCA	DTCB	Dead time (ns)
Smart near-zero DTC	$INTV_{CC}$		0 (typ)
Adaptive DTC	GND		20 (typ)
R_{SET} DTC	10 Ω to 200 kΩ	10 Ω to 200 kΩ	7 to 60

Choosing a dead time is an exercise in tradeoffs. For the lowest losses possible, use the smart near-zero dead time and rely on the intelligent detection and servo architecture for the highest possible power density applications with the highest efficiency. Armed with the knowledge of how to set up and verify the dead time is minimized to near zero with proper measurements, this is generally the best option.

Fig. 9 shows this near-zero dead time in action with optimized gate resistance. There is no visible reverse conduction time, and no parallel Schottky diode is used at additional penalty to protect the GaN FET. This results in maximum efficiency and minimal thermal stress.

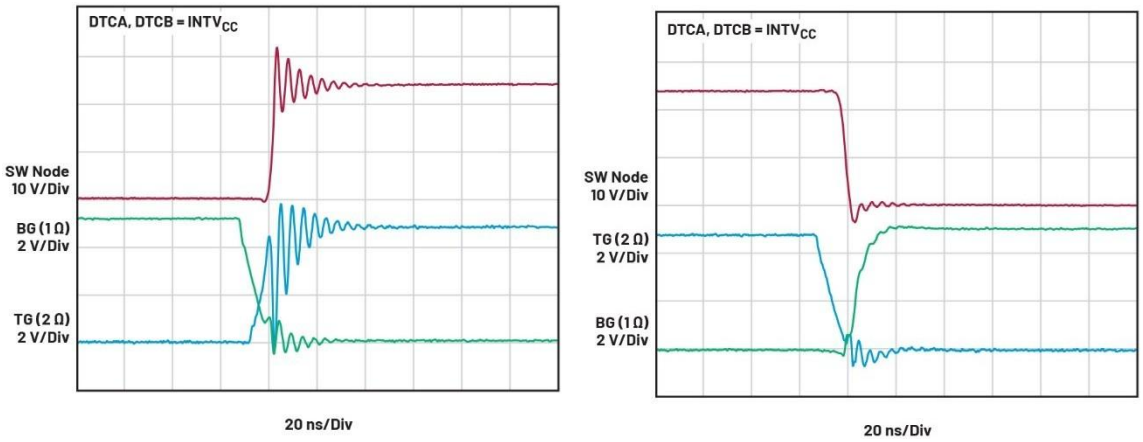

Fig. 9. Smart near-zero dead time control transitions using optimized gate resistance. Note there is no visible reverse conduction region showing on switch node with this mode enabled to actively control dead time.

If, however, design mandates dictate some finite amount of dead time beyond this, the adaptive modes will allow any value to be dialed in for perceived comfort margin at the expense of power lost to heat in the GaN FETs, as shown in Fig. 10. This may be due to conservative management engineering mandates or driven by reluctance to stray too far from guidance derived from MOSFET-based designs, but the LTC7890 and LTC7891 allow the user all options to suit their needs.

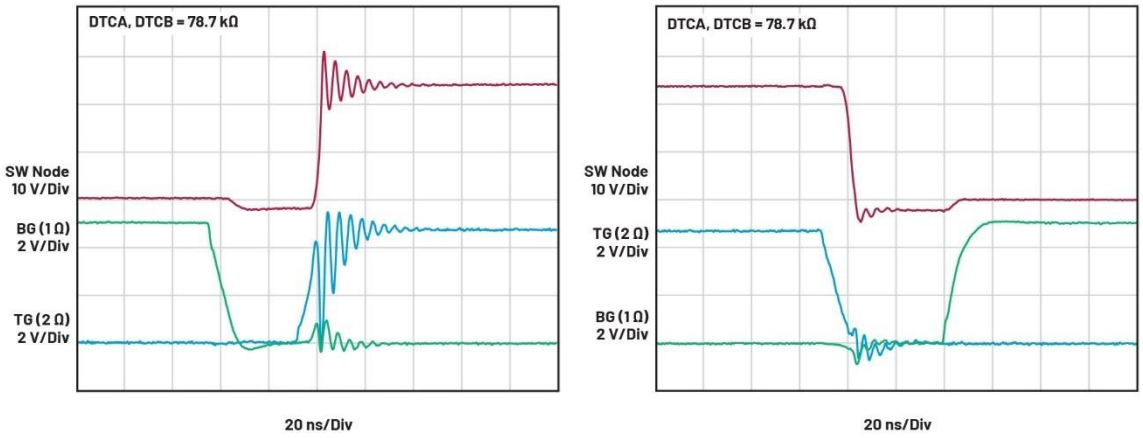

Fig. 10. 35-ns dead time R_{SET} mode transitions using optimized gate resistance. The dead time is precisely controlled but the reverse conduction periods reflected in the switching waveforms are clearly visible at 2 V, resulting in considerable losses.

As dead times increase, it is especially important to record efficiency and peak hot spot temperatures of the FETs with thermal imaging devices at the corner conditions to retain thermal margin for planned ambient operating conditions. Like the gate resistance, dead time has a direct and pronounced effect on peak thermal stress on the FETs. The peak temperature of the top FET for the 12-V V_{OUT}, 10-A condition being tested here is 56.3°C using the optimized gate resistances. This represents a 3°C temperature rise from the 0-Ω PCB trace, but is reasonable considering there is no overvoltage stress to damage the FETs during transients.

However, when the R_{SET} mode is used to increase the dead time to the 35 ns typically found in controllers without smart near-zero or adaptive controls, this jumps over 10°C to 66.5°C for the same power developed at the output—and it's seen on both FETs (Fig. 11).

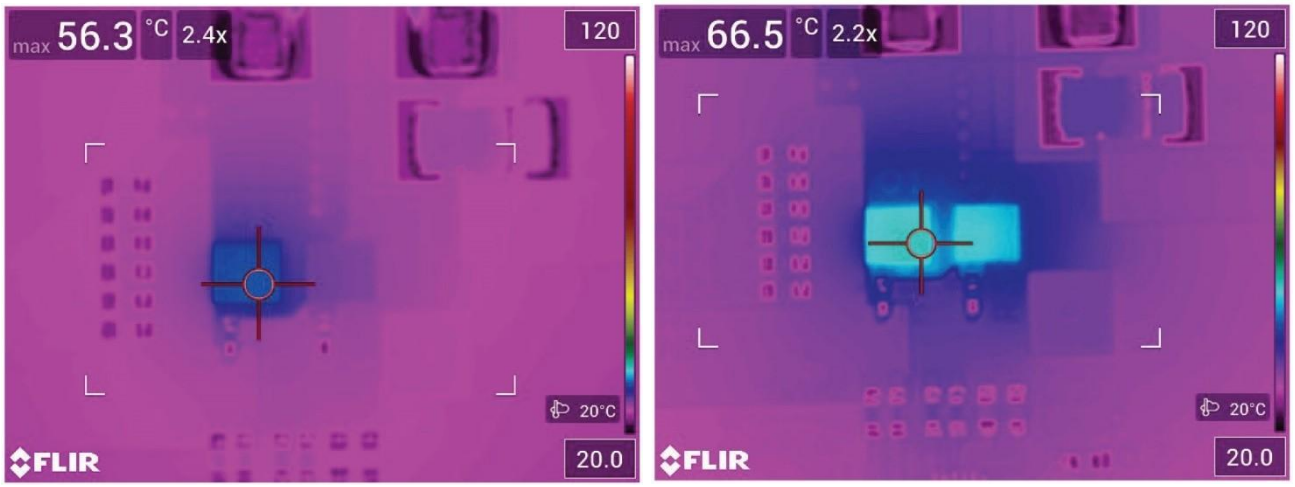

Fig. 11. Thermal capture of transition losses due to dead time modes. The left image is taken at 24-V V_{IN} and 12-V V_{OUT} at 10 A using smart near-zero dead time mode and optimized gate resistance, resulting in a peak temperature of 56.3°C on the top FET. The right image shows identical conditions with 35-ns (typical) dead time configured in R_{SET} mode. Both FETs increase in temperature to 66.5°C with no additional power delivered at the output.

It becomes apparent that the price for being conservative in this regard is an efficiency and thermal penalty that eats into the power budget. That same amount of thermal loss could have been used for an additional several dozen watts of output power delivery if the smart near-zero functionality had been utilized. Food for thought when deciding if tradition, rather than empirical data, is to be prioritized when determining dead time margin for comfort.

When using the controllers discussed here, follow this development process by starting with a sound layout using evaluation reference designs provided by Analog Devices. Continue with solid bench measurement techniques to measure and validate the design. This ultimately results in a reliable design circuit for the final product. The data collected during this process, following the procedures and techniques described, will be accurate and trustworthy.

Armed with a solid understanding of what the tradeoffs are and how to balance them, better decisions about which modes of operation, what external component values to use—and, more importantly, why those decisions are being made—will ultimately shorten design cycle times, reduce costly iterations, and prevent much frustration by the system designer.

Conclusion

GaN technology is rapidly developing as leaders in the wide-bandgap technology continue to improve the $C_G \times R_{DS(ON)}$ figure of merit with each generation of device offerings. While the device size, capacitance, and on-resistance change with each new iteration, the right approach to reliable measurement and verification of operation remains the same.

There is simply no acceptable substitute for bench verification of prototype operation to ensure that a design is solid and has sufficient safety margin at the corner conditions of operation. Designs that follow data sheet guidelines, layouts that closely follow evaluation board placement and routing, and measurements taken with the guidance offered here will offer the best chances of a first-pass success with no re-spin necessary.

References

1. LTC7891 product page.
2. LTC7890 product page.

About The Author

James R. Staley has over 25 years of semiconductor industry experience. He is currently a senior product applications engineering manager for Analog Devices in the Data Center and Energy business unit. He has held positions with applications engineering, sales applications engineering, and systems engineering groups at Linear Technology and Analog Devices. James and his family reside in the Raleigh, North Carolina area. He graduated Eta Kappa Nu from North Carolina State University with a B.S.E.E. concentration in nanotechnology.

For more on dead-time related discussions, see How2Power's Design Guide, and do a key word search on "deadtime" and "dead time". Also, locate the "Popular Topics" category and select "Silicon Carbide and Gallium Nitride".