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Commentary

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Optimizing Power Density In Power Converters: The Role Of Top-Side-Cooled Packages

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Power electronics are evolving rapidly, with new materials and packaging technologies driving efficiency gains and enabling higher power densities. A key enabler of this transformation is the integration of advanced packaging technologies like Infineon's top-side-cooled (TSC) Q-DPAK packages (Fig. 1).

These packages, which separate the thermal and electrical paths, significantly enhance the performance of power converters. While silicon MOSFETs like CoolMOS and CoolSiC have traditionally dominated power conversion applications, the benefits of top-side cooling are now being realized across silicon (Si) and silicon carbide (SiC) based devices, offering higher efficiency, faster switching speeds, and the ability to operate at elevated temperatures.

This article explains the thermal and electrical advantages offered by MOSFET packages with top-side cooling using Infineon's Q-DPAK as an example where these benefits are maximized. It then discusses how to optimize the PCB layout and configuration of the switching cells when using TSC packages for optimal converter performance. Results of testing a full-bridge eval board with TSC SiC MOSFETs are presented to validate the recommended techniques for optimizing the board layout.

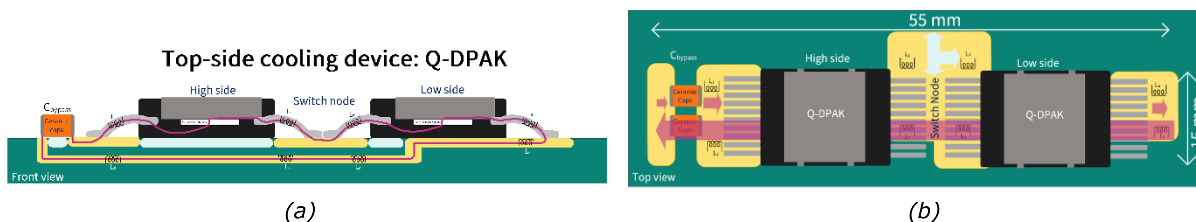

Fig. 1. Power loop design: top-side-cooling device viewed from the side (a) and the top (b).

The Role Of Package Design In Power Converter Optimization

Package design is a critical factor in the overall performance of power converters (Fig. 2). For both Si and SiC MOSFETs, the efficiency of the power conversion process is directly influenced by the packaging choice. Traditional bottom-side-cooled (BSC) packages have a cooling pad beneath the power device, typically requiring additional thermal vias and PCB modifications to achieve the necessary thermal performance. However, this design can be limiting, as the cooling path is constrained by mechanical stack-up, which increases the complexity of thermal management.

While the thermal stack is similarly built up in a traditional through-hole (THT) TO-247 package, the electrical performance in such configurations does not match that of top-side-cooled (TSC) packages. Although both approaches share a similar thermal pathway, the TO-247 package tends to exhibit higher parasitic inductance due to the way current flows through the package and the associated PCB layout. The increased parasitics in these configurations can adversely affect switching speed and efficiency.

In contrast, TSC packages allow for more optimized current paths and significantly lower parasitic effects, improving both thermal dissipation and electrical performance. The higher parasitic inductance in TO-247 packages typically limits their use in high-frequency applications, where fast switching speeds and low losses are crucial (Fig. 3).

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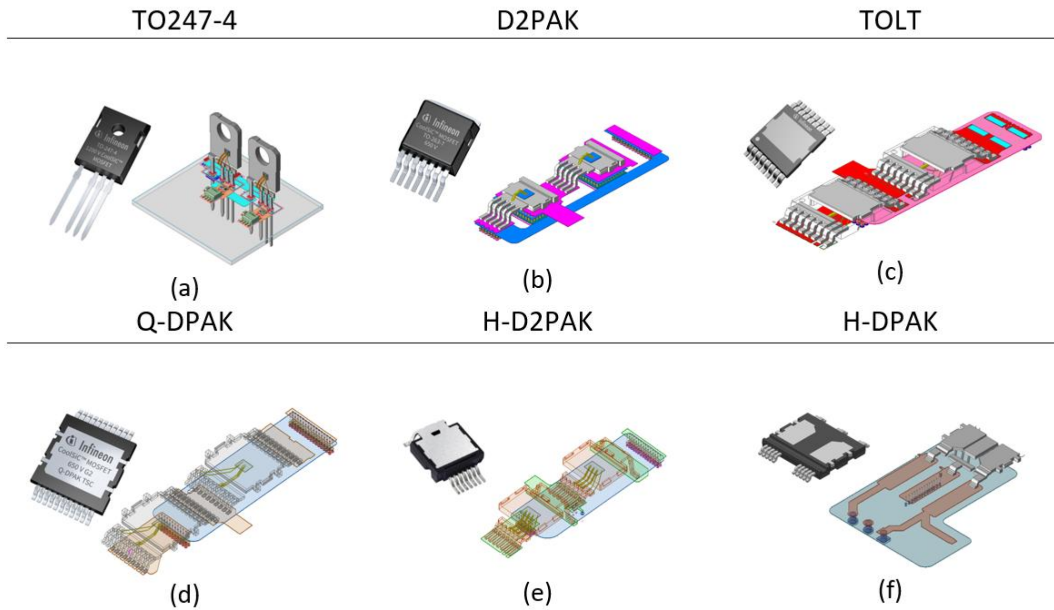
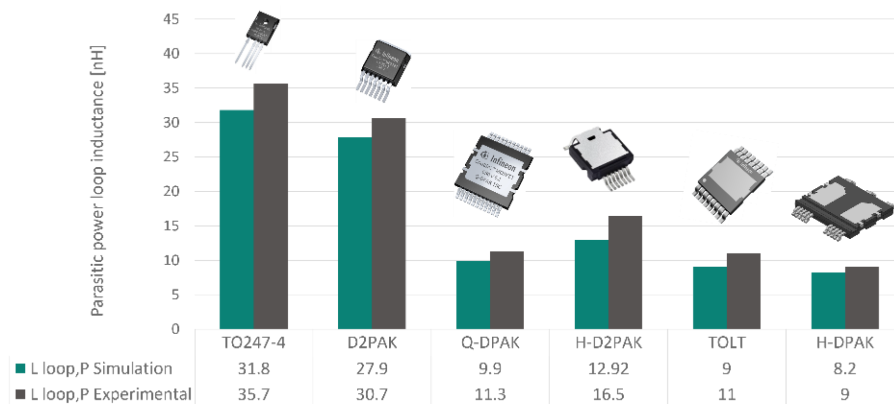


Fig. 2. Different power loop designs by package: TO247-4 (a), D2PAK (b), TOLT (c), Q-DPAK (d), H-D2PAK (e), and H-DPAK (f).



	TO247-4	D2PAK	Q-DPAK	H-D2PAK	TOLT	H-DPAK
L loop,P Simulation	31.8	27.9	9.9	12.92	9	8.2
L loop,P Experimental	35.7	30.7	11.3	16.5	11	9

Fig. 3. Comparison of the power loop inductance values for different power packages.

TSC packages like the Q-DPAK offer a clear advantage by enabling direct attachment to heatsinks or liquid cooling systems on the top of the package. This design decouples the thermal path from the electrical path, making it easier to dissipate heat efficiently while reducing thermal resistance. With TSC, the power device and gate driver can be positioned on the same side of the PCB so long as the gate driver is not thicker than the device itself. Although, it’s recommended that the gate driver be placed on the opposite side of the board. Given that if offers these options for component placement, TSC provides greater design flexibility and system-level integration than bottom-side cooling.

Thermal Stack Considerations

A significant difference between top-side and bottom-side cooling lies in the impact on the thermal stack. Heat is dissipated through the PCB with bottom-side cooling, and the cooling pad is located beneath the package. This setup can lead to challenges in terms of thermal efficiency and additional PCB space requirements for the cooling vias. Moreover, the cooling efficiency is compromised by the need to manage heat dissipation across the PCB, which can risk other components on the board getting hotter due to heat buildup around the device.

In contrast, top-side cooling allows the cooling system to be directly mounted to the device, improving thermal dissipation and simplifying the overall thermal stack design. The cooling system can be integrated at the top of the package, allowing for more direct and efficient heat transfer. This enables designers to create a more

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compact thermal stack, reducing the need for complex thermal vias and increasing the system's overall thermal performance (Fig. 4).

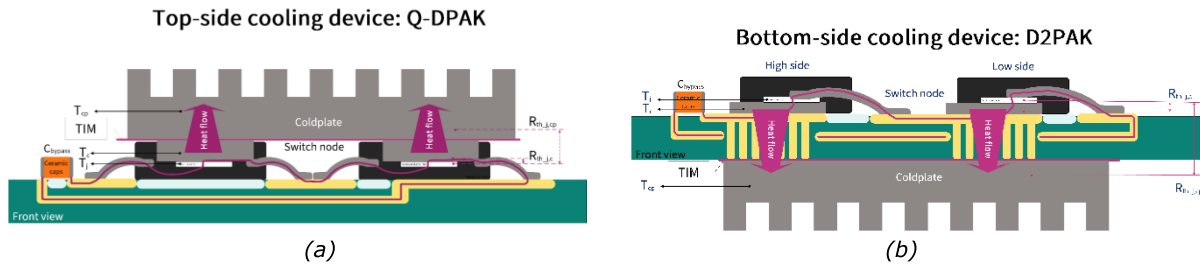

Fig. 4. Thermal concept for top-side cooling (a) and bottom-side cooling (b) devices.

Moreover, top-side cooling opens up the possibility for a 3D design, as the cooling path is separated from the power loop. This decoupling is particularly beneficial for high density designs, where efficient use of the PCB area is crucial. The result is a more reliable power converter with better heat management, enabling higher power density and better performance under load.

Minimizing Parasitic Inductance

One of the primary challenges in optimizing power converters is minimizing parasitic inductance and capacitance, especially in high-frequency switching applications. These parasitic elements can significantly impact the switching behavior of power devices, reducing switching speeds and increasing losses. To achieve the best performance in power conversion systems, optimizing both the PCB layout and the configuration of the switching cells (SW-Cells) used in the converter is essential.

The SW-Cell design defines the placement of power devices, gate drivers, and other components on the PCB. It is critical to design these cells with careful consideration of the current paths, loop areas, and the overall layout to reduce parasitic inductance. Reducing inductance enables faster switching times, which enhances system efficiency by reducing losses.

The power loop is optimized for top-side-cooled packages by positioning the decoupling capacitors close to the power devices. This configuration minimizes the inductive loop area, resulting in lower parasitic inductance and improved switching speed. On the other hand, bottom-side cooling systems often struggle to achieve the same level of optimization due to the need for additional vias and thermal management considerations, which can increase parasitic inductance and reduce efficiency.

Switching Cell (SW-Cell) Designs: Tailoring Layouts For Specific Applications

Efficient power conversion depends on the choice of SW-Cell design, which determines how power devices and associated components are arranged on the PCB (Fig. 5).

The *I-Loop SW-Cell* is the standard design, where the MOSFETs are placed on the bottom of the PCB, and the other components are placed on the top side. While this configuration works well for many applications, it does not offer the lowest parasitic inductance, particularly in high-frequency systems.

The *area-optimized I-Loop SW-Cell* places the gate driver input stage opposite the MOSFETs, optimizing available PCB space. This layout reduces parasitic inductance while maintaining high switching performance, making it ideal for applications where power density and compact design are critical.

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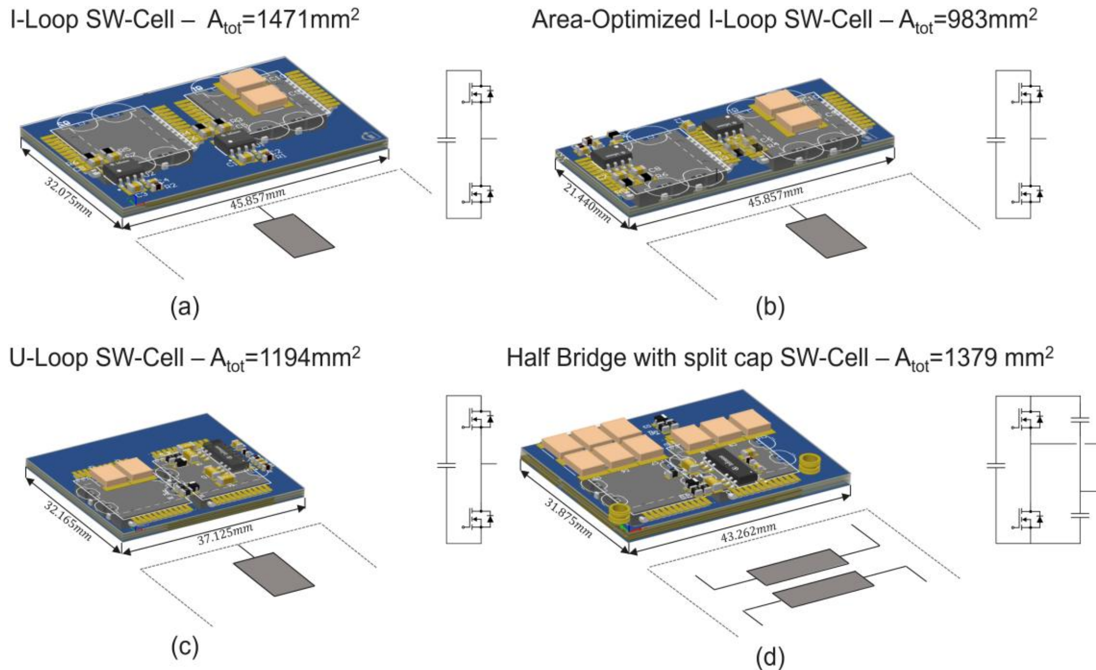

Fig. 5. Proposed power-dense half-bridge switching cells based on Q-DPAK TSC: I-loop SW-Cell (a), area-optimized I-Loop SW-Cell (b), U-loop SW-Cell (c) and half-bridge with split cap SW-Cell (d).

The *U-Loop SW-Cell* separates the switching node from the dc+ and dc- terminals by placing them on opposite sides of the PCB. While this design is suitable for space-constrained applications, it leads to higher parasitic inductance due to a lesser optimization of the current path routing, which can slow switching performance in high-frequency designs.

Finally, the *split-cap half-bridge SW-Cell* is optimized for ZVS topologies, such as LLC converters. This design splits the resonant capacitors between the dc+ and dc- terminals, improving commutation efficiency and reducing switching losses. However, it requires careful layout and a higher component count, making it more complex than other designs.

System-Level Design And Thermal Management

The performance of a power converter depends not only on the electrical layout but also on how well the thermal and mechanical designs are integrated into the system. Thermal management is crucial for ensuring that the power devices operate within safe temperature ranges and to avoid thermal runaway.

For top-side-cooled packages like the Q-DPAK, thermal management is simplified by enabling direct attachment of heatsinks or cooling plates to the top of the package. This setup minimizes thermal resistance, improves heat dissipation, and reduces the need for complex thermal vias, such as inline copper PCBs, typically required in bottom-side-cooled packages. This enhanced thermal performance helps the power converter operate at higher power densities without compromising reliability.

Mechanical design is also crucial, particularly in systems with high-density components. A well-designed PCB layout can help minimize mechanical stress, which is essential for maintaining the board's structural integrity and ensuring the power converter's long-term performance.

Validating Design Optimization

To validate the effectiveness of these design strategies, a full-bridge evaluation board was built using Infineon's CoolMOS and CoolSiC MOSFETs housed in Q-DPAK TSC packages. The board featured a four-layer PCB optimized for power plane design, vertical current loop routing, and magnetic field compensation (Fig. 6). The layout from the switching cell follows the concept of the *I-Loop SW-Cell* standard design (Fig. 5a).

System-level testing confirmed that the optimized layout reduced power loop inductance to approximately 7 nH, matching simulation predictions of 6.9 nH obtained using Ansys 3D FEM multi-physics. This result demonstrates

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that simulation-driven design techniques can be successfully applied in real-world power converters, enabling faster switching and reduced losses.

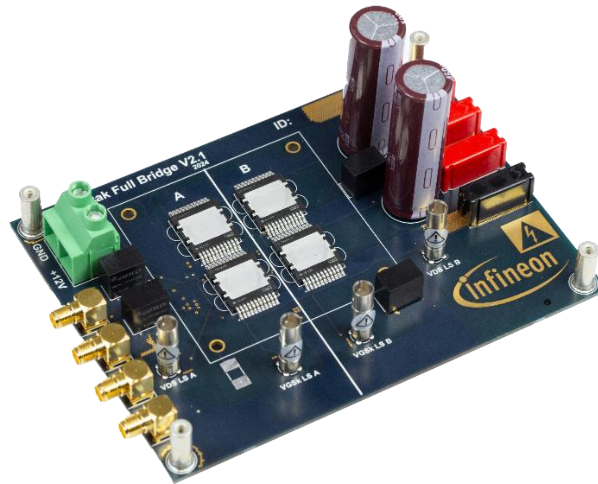

Fig. 6. Q-DPAK full-bridge board.

The gate drive placement was optimized to minimize parasitic capacitance and ensure signal integrity, further improving switching performance. These results validate the importance of optimizing the electrical layout and thermal management in SiC-based power converters.

Conclusion

Infineon's top-side-cooled Q-DPAK packages offer a compelling solution for optimizing power density and system efficiency in both CoolMOS- and CoolSiC-based power converters. By decoupling the thermal and electrical paths, TSC packages reduce parasitic inductance, enhance thermal performance, and enable more efficient power conversion.

Optimizing PCB layouts, SW-Cell designs, and thermal management strategies is critical for unlocking the full potential of SiC and silicon MOSFETs in high-power applications. With the right design choices, power converters can achieve higher efficiency, faster switching speeds, and greater reliability, setting the stage for the next generation of power electronics.

About The Author

Josef Wildauer is a principal engineer with Infineon where he leads the development of new technologies, leveraging his strong background in physics to drive innovation. Currently, Josef's main emphasis is on the development of new SiC MOSFET technologies, specifically tailored for the automotive industry. In this role, he has been responsible for designing and implementing cutting-edge solutions, including the development of new automotive concepts and the optimization of SiC MOSFET performance. Josef has a master of science (MSc) degree in applied physics from the University of Innsbruck, where his studies focused on molecular physics.

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