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Deploying Primary-Side Current Sensors For PSU Output Current Limiting—Protecting Against Low Impedance Overloads

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Current limiting in a switch-mode power supply protects PSU components and the powered load from damage by preventing excessive current during load surges, overloads, or short-circuit conditions. It allows the user to use cheaper, more energy-efficient, lower-power PSUs (see the reference) to energize spikey loads and support peak loading conditions with passive components (buffer caps) and load control. Key advantages of current limiting include preventing overheating and fire hazards, as well as PSU auto-recovery when an overload or faulty condition is removed.

Constant current and current foldback are popular methods of current limiting that may be implemented with current sensing on either the secondary side or primary side of the power supply. The latter has advantages such as reduced losses and improved reliability. For example, current transformers (CTs) used to implement primary-side current-mode control can also provide the sense signal for primary-side current limiting.

However, filtering of the CT signal to remove the spike generated by hard switching—needed for accuracy of current-mode control—can undermine current limiting when the load is shorted by a very low impedance presented by a failed component or a PCB defect. This problem of sensor accuracy occurs regardless of the sensor type used for primary-side current sensing.

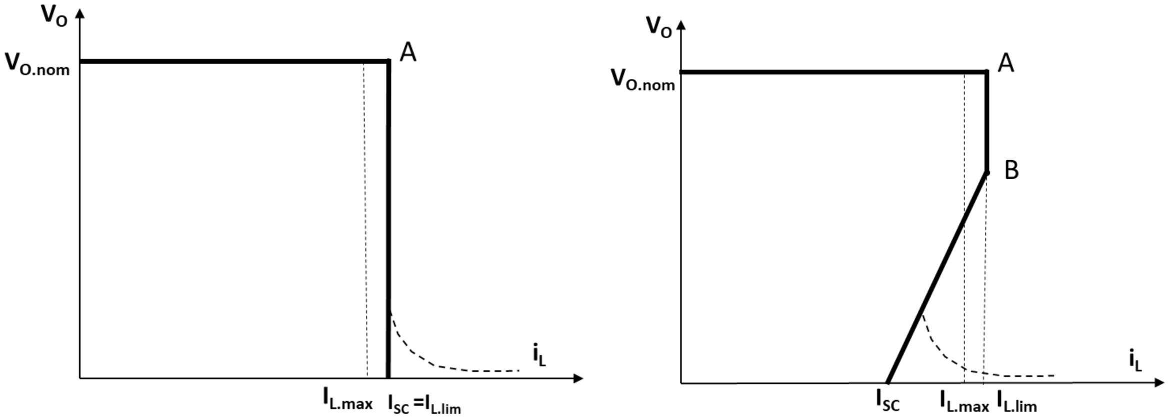
In this article, this sensor error at very low impedance load is explained, and we analyze the short circuit current increase and its sensitivities to the magnitude of the overload and CT sensor time constant. Based on this analysis some guidance is given on selection of the CT sensor filter capacitor value, rating of the power components for the two forms of current limiting, and on activation of the PSU latch-off feature.

Constant-Current Limiting Vs. Current Foldback

There are two most common implementations of PSU overcurrent protection: constant current limit and current foldback. They operate similarly when the load current reaches the preset limit ($I_{L.lim}$ in Fig. 1), which is set higher than the PSU maximum continuous rating ($I_{L.max}$). In the first (fixed current limit) implementation, once the PSU load current reaches the preset limit, and the load impedance keeps dropping, the PSU V-A load line falls vertically, reflecting the output voltage reduction while keeping the load current unchanged (Fig. 1a). Because this operation mode is associated with relatively high-power dissipation ($I_{L.lim} > I_{L.max}$), it can be used within preset limited time intervals.

In the current foldback case, unlike the fixed current limit, the load current gets reduced, usually below the PSU maximum rating $I_{L.max}$, once the load impedance and the output voltage drop below a certain preset level (point B in Fig. 1b). Such a control mechanism is used to reduce thermal stress on components when the overloading condition lasts a long time.

The load lines shown in Fig. 1 can be generated by comparing a sensed current signal with a fixed or variable reference and controlling the PWM duty ratio based on the resulting error signal. Although the fixed current limiting and current foldback techniques are straightforward to implement with secondary-side sensing, monitoring the output current typically causes additional power loss in a current-sense resistor, which is particularly apparent in high-current applications.

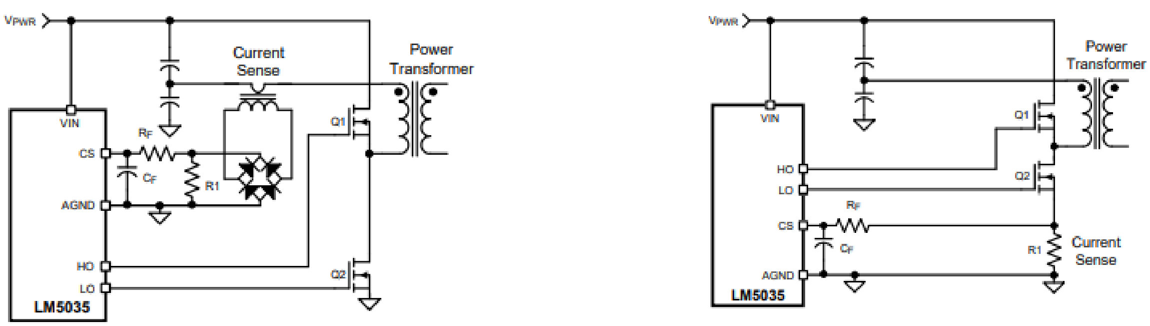


(a) (b)

Fig. 1. Output V-A load lines with fixed current limit (a) and current foldback (b). Dashed lines illustrate the potential increase in output current when the current is sensed on the primary side and the short-circuit impedance reaches ultra-low levels.

Sensing the load current on the primary side has noticeable advantages over load-current sensing. In that case, there is no need to accommodate a resistive sensor in a high-current path on the secondary side. In many cases, primary-side sensing can be provided by existing components used for other converter control functions.

For example, current-mode control often uses current transformers (CTs) as sensors to monitor the inductor current, which is then fed into a feedback loop to regulate the switching power supply. Primary-side CTs are also used to provide signals supporting symmetrical transformer core operation in push-pull topologies, protection from primary shoot-throughs caused by control glitches, etc. Typical examples of placements of primary-side current sensors are given in Fig. 2, which depicts the half-bridge LM5035 PWM controller application guidelines.



(a) (b)

Fig. 2. Primary-side current sensing options in a half-bridge topology utilizing a current transformer (a) and a sense resistor (b)

Thus, using primary-side current sensing offers the advantages of high reliability, higher efficiency, and lower heat generation compared to resistive sensors placed in high-current secondary-side networks.

Challenges With Primary-Side Current Sensing

The implementation of fixed current limiting and current foldback techniques, which employ sensing the PSU load current on the primary side for PSU protection purposes, presents some challenges. In most hard-switching converter topologies, the active component current contains a spike reflecting the output rectifier recovery and parasitic capacitor charging processes. This spike needs to be filtered out to prevent an inaccuracy in the current magnitude detection (that is, the magnitude of the output current).

This filtering (shown in Fig. 2 networks), in turn, can affect the PSU reliability in a short-circuit condition when the impedance of the short drops to very low levels. This condition is characteristic of the PSUs supplying power to dc-dc regulators whose faulty active components may have a resistance of a few milliohms. Let's take a closer look at this phenomenon.

A typical primary-side active component current waveform produced by a current transformer sensor is shown in Fig. 3 with a blue-colored trace. The smoothed waveform in which the spike is filtered with a capacitor placed in parallel with a CT terminating resistor is presented on the same diagram in green.

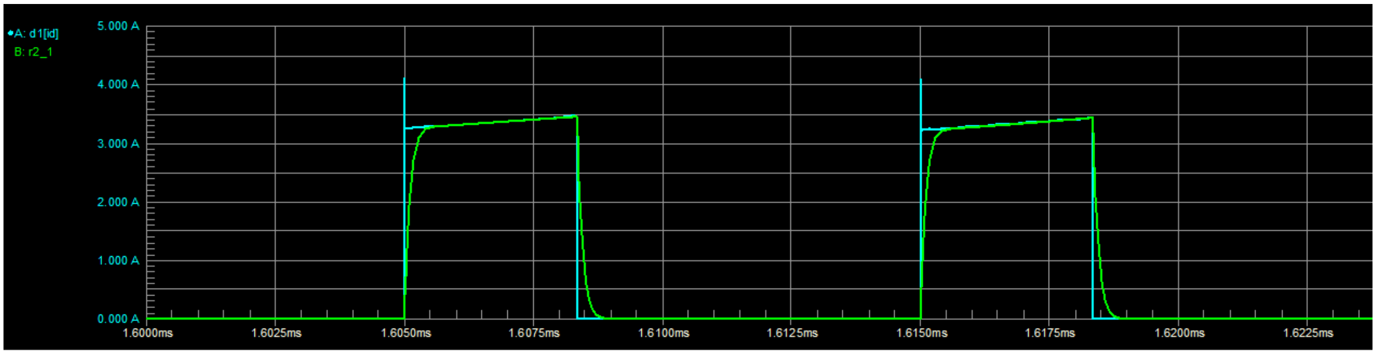


Fig. 3. Typical active component current waveforms generated on the primary side. Actual with a spike (blue) and the smoothed with the spike filtered with a cap placed in parallel with a CT terminating resistor.

In the current limit mode, once the load impedance drops below a certain level and the load current reaches a predetermined threshold ($I_{L.lim}$ in Fig. 1), the PWM reduces the duty ratio of the generated pulses, lowering the output voltage and maintaining the primary-side current magnitude and the load current unchanged.

The PSU reliably operates in this mode unless the load represents a very low impedance short. Such a short-circuit condition is characteristic of the loads containing dc-dc converters. The failed-into-short active component in such a converter can have an impedance of just a few milliohms, which requires decreasing the duty ratio to a small percentage of the nominal. At such impedance levels, the sensor operating point can fall into the ramp region of the filtered green-color waveform in Fig. 3, which can directly affect detection accuracy and the actual current magnitude.

This case is illustrated in the diagrams shown in Fig. 4. At low-impedance shorts, while the sensed peak level remains fixed (blue trace in Fig. 4), the actual current magnitude may noticeably exceed the projected level (red trace) and overstress the PSU active components. To ensure the PSU's reliable operation in this condition, this increase in the current magnitude needs to be evaluated.

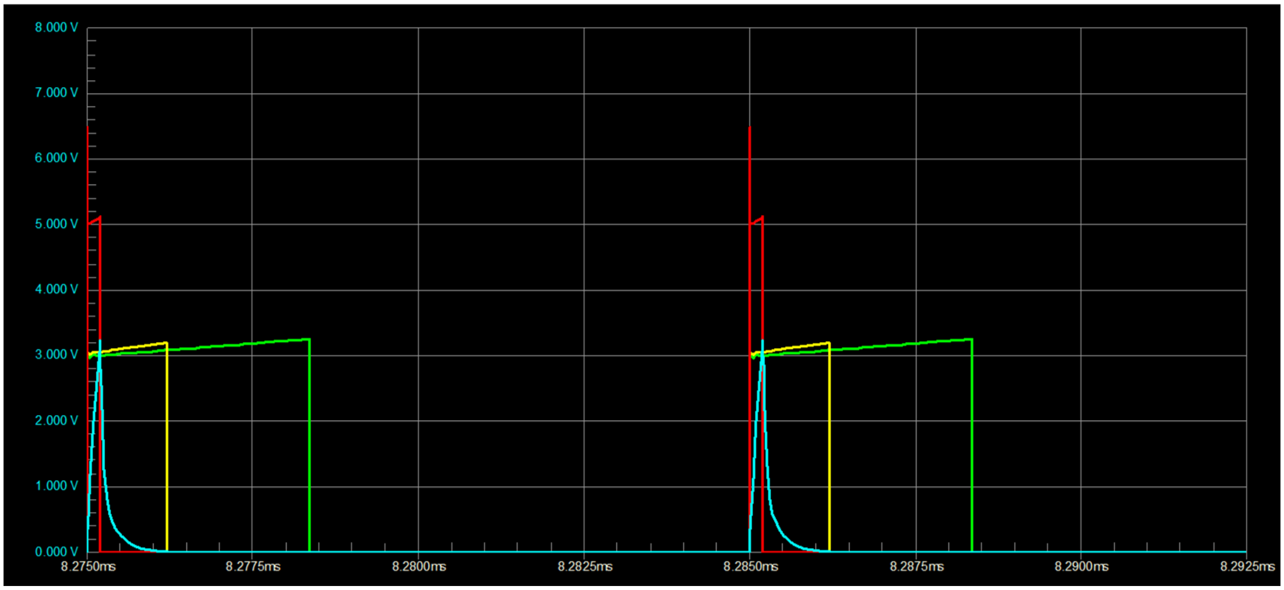


Fig. 4 In the current limit mode, when the load impedance drops from $R_L = V_o/I_{L.lim}$ to approximately $R_L = V_o/3I_{L.lim}$, the peak loading condition causes the operating duty to reduce while keeping the sensed and actual current magnitudes unchanged (green and yellow waveforms). When the load impedance drops to much lower levels corresponding to an ultra-low impedance short, while the sensed peak level remains unchanged (blue trace), the actual current magnitude (red trace) can exceed the planned level and overstress the PSU active components.

Actual Current Magnitude Increase

When the primary active component current magnitude is sensed with a current transformer, having a terminating resistor R, the current spike associated with the output rectifier recovery and parasitic capacitance charging processes mentioned above is usually smoothed with a filtering capacitor.

To quantify the magnitude increase, let’s neglect the parasitic spike impact and assume for clarity that the current signal has a rectangular shape and that the sensor output waveform shape depends on the current pulse magnitude and RC time constant, where C is the filtering cap value.

In that case, when the operating duty enters the rising slope region, producing the same detected signal level requires a higher actual current pulse magnitude. This phenomenon is illustrated in more detail in Fig. 5.

In this diagram, the CT sensor output pulse magnitude corresponding to $I_{L.lim}$ is designated as $I_{M.lim}$, and the pulse magnitude under a low-impedance short circuit condition is designated as $I_{M1.lim}$. These levels correspond to the primary current magnitudes referred to the secondary CT winding.

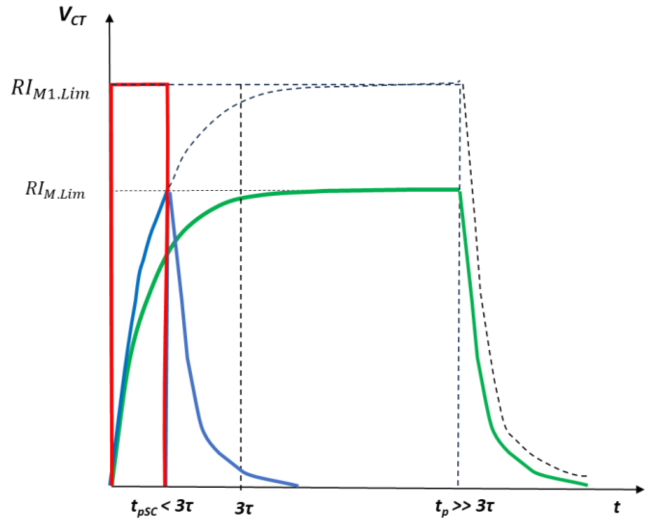


Fig. 5. When under short circuit conditions, the load impedance reaches very low levels, and the pulse duration t_{pSC} becomes lower than 3τ (τ = RC), the operating duty enters the rising slope region of the CT sensor pulse (blue trace), and keeping the same sensed signal magnitude $RI_{M.Lim}$ results in a higher actual current pulse magnitude $I_{M1.Lim}$ (red trace). The green trace represents the safe condition where the CT sensor accurately senses the current magnitude.

Assuming that the primary-side pulse magnitude needs to be always kept at $I_{M.Lim}$ we can write the following equation representing the relationship between the "regular" current limit condition ($t_p \gg 3RC$—green trace in Fig. 4 or point A in Fig. 1) and the low-impedance short-circuit condition $t_{pSC} < 3RC$):

$$RI_{M1.Lim}\left(1 - e^{-t_{pSC}/\tau}\right) = RI_{M.Lim}$$

The current magnitude in the low-impedance short circuit condition can be obtained from this equation as follows:

$$I_{M1.Lim} = I_{M.Lim}/\left(1 - e^{-t_{pSC}/\tau}\right)$$

As can be seen from this expression, the shorter the pulse duration t_{pSC} the higher actual current magnitude $I_{M1.Lim}$. To determine what pulse duration under short circuit will be set by the control loop and at what impedances the process of the actual current magnitude increase can take place, we can consider that in the current limit mode, the output voltage is, on one hand, proportional to the current magnitude and the load impedance, and, on the other hand, to the pulse duration at the PSU output filter input:

$$\frac{I_{M1.Lim}R_{SC}}{I_{M.Lim}R_{nom}} = \frac{t_{pSC}}{t_{p.nom}}$$

where R_{nom}, $t_{p.nom}$ and R_{SC}, t_{pSC} are nominal load impedance and pulse duration in point A (Fig. 1) and load impedance and pulse duration under short-circuit conditions, respectively. Substituting into this equation the expression for the current magnitude under the low impedance short circuit condition and after using normalized values, we get

$$\frac{D_{SC}}{D_{nom}} = \widehat{D_{SC}} = \frac{\widehat{R_{SC}}}{1 - e^{-\widehat{D_{SC}}/\hat{\tau}}} \qquad (1)$$

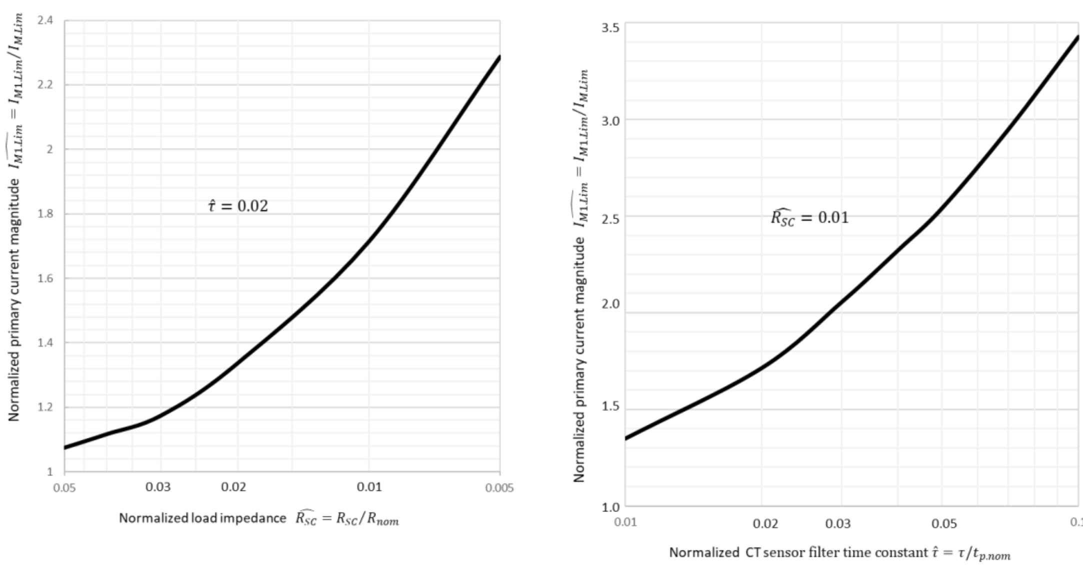
where $\widehat{D_{SC}} = D_{SC}/D_{nom}$ is the short-circuit operating duty normalized over the nominal, $\hat{\tau} = \tau/t_{p.nom}$ is the normalized RC time constant, and $\widehat{R_{SC}} = R_{SC}/R_{nom}$ is the short-circuit impedance normalized over the nominal (point A in Fig. 1).

Rewriting the equation for $I_{M1.Lim}$ for the normalized values yields

$$\widehat{I_{M1.Lim}} = \frac{1}{1-e^{-\widehat{D_{SC}}/\hat{\tau}}} \qquad (2)$$

By solving the transcendental equation (1) for $\widehat{D_{SC}}$ with a numerical method, we can determine the $\widehat{D_{SC}}$ level as a function of the short circuit impedance $\widehat{R_{SC}}$ and the current sensor time constant $\hat{\tau}$. Substituting the computed $\widehat{D_{SC}}$ values into (2) yields the actual current limit as a function of these two variables.

The results of these computations are presented graphically in Fig. 6a and b for several typical parameter values. $\widehat{R_{SC}}$ values on the X-axis in the diagram in Fig. 6a are given in reverse order for a more visual illustration of the primary current increase at low short circuit impedances. The graphs demonstrate significant (up to 3 times) actual current increases over the projected level. This phenomenon is also illustrated by the dashed tracks in PSU output V-A load lines in Fig. 1.



(a) (b)

Fig. 6. Current magnitude vs. short circuit impedance (a) and current sensor time constant (b).

Safe PSU Operation At Low Short Circuit Impedances

The plot in Fig. 6a demonstrates that the actual current limit can significantly exceed the projected value when short-circuit impedances are at low levels and represent a small percentage of the nominal load value. For example, if a 12-V, 20-A (240-W) PSU having peak power of 360 W current limit is set at 30 A (i.e. R_{nom} = 400 mΩ) at R_{SC} = 4 mΩ ($\widehat{R_{SC}} = 0.01$), the current limit exceeds the projected level by more than 70%, i.e., by more than 20 A. Such an increase in current magnitudes can overstress PSU active components and cause excessive heat dissipation in the output circuitry if this condition persists for a thermally significant time.

Another factor affecting the current limit is the CT sensor time constant, which, in practice, influences the selection of the CT sensor filter capacitor value. If the CT sensor filter time constant $\hat{\tau}$ is changed from 0.02 to

0.03, the current limit increase in the above example will exceed 100% (Fig. 6b). To avoid PSU damage, the rise in current limit in low-impedance short-circuit conditions needs to be addressed at the design stage.

If the low-impedance short-circuit condition is possible in the PSU's real operating environment, the following measures can be taken to prevent PSU active components from overstressing. Evaluation of potential limit increase using the method described above offers the opportunity to avoid over-filtering the sensor signal by selecting the minimum possible CT sensor cap value. If, with the given R_{SC} and computed τ values, the exceeding of the projected current limit level is still possible, active components' maximum ratings need to be selected to accommodate the calculated increase.

In the fixed current limit case, the PSU's instantaneous turn-off feature must always be activated to prevent active components from overheating in the continuous short-circuit condition or when a peak loading condition lasts for a thermally significant time interval. This can be achieved by activating the UV protection: when the PSU is in current limit mode, and the output voltage drops below a certain level, e.g., 30% of the nominal, the PSU latches off.

In the current foldback case, instantaneous turn-off (latch-off) does not need to be used (i.e. it adds no value) if the foldback limit reduction exceeds the computed current limit increase. However, the latch-off feature does need to be activated in the foldback case if the current limit reduction cannot outbalance the actual current increase. With this control mechanism, the PSU operating point will move from point B in Fig. 1 to the origin of the coordinate system, avoiding a potentially unsafe area.

The latch-off in both cases can be justified by the fact that, in practice, a continuous short-circuit condition and low supply voltage level don't allow the load to operate properly anyway, and PSU shutdown will not create any additional degradation to system operation.

Reference

"Energy-Based Efficiency Metric Helps To Optimize Server Power Delivery For Dynamic Workloads" by Viktor Vogman, How2Power Today, October 2018.

About The Author

Viktor Vogman is currently retired from Power Conversion Consulting where he applied his skills as an analog design engineer specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

For more on power protection in power supply design, see How2Power's Design Guide, locate the "Design area" category and select "Power Protection".