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Stabilizing The Loops Of A Three-Phase Vienna Rectifier—Part 1

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The three-phase Vienna rectifier was patented by Prof. Johann Kolar in December 1993, as he explained in the keynote session[1] he gave at the Applied Power Electronics Conference (APEC) in 2018. In its simplest unidirectional implementation, the rectifier requires a three-phase diode bridge associated with three bidirectional switches, nowadays commonly realized with two back-to-back power SiC transistors for example.

The control of these components can be done in different ways like full hysteretic control, sinusoidal pulse-width modulation (SPWM) or space vector modulation (SVM). In a typical application featuring *dq0* control, there are three loops to stabilize. However, the methods that are currently used to design the compensation for these loops have their drawbacks.

Some programs use an auto-tuning engine to tweak compensator parameters automatically—but this is a form of trial and error. At least one program, PLECS, can generate the small-signal response of the entire converter, but this requires a license for the tool. While designers could potentially perform a small-signal analysis on a Vienna rectifier design, for most the process is too complicated.

To address this situation, I have found an averaged model consisting of six PWM switch models that can deliver the ac responses we need to stabilize the converter in a reasonably straightforward and fast way. In this first part of the article, we will explore a strategy using this average model to compensate the control loops of a Vienna rectifier with analog circuits. Then in the upcoming second part, we'll update this method for a converter operating with digital compensators.

Here in part 1 we will start with the T-type converter, which is a good vehicle to explain the operation of the Vienna rectifier by reducing it to a single-phase implementation. As we will see, we can develop an average model of the single-phase T-type converter based on Vorpérian's switch model and then extend it to three phases to model the Vienna rectifier. Having this average model will allow us to more easily obtain the response of the Vienna rectifier using LTspice.

While this study will not explain control theory in depth, we'll briefly review the concept behind the Clark transformation, which is the basis for *dq0* control. Then we'll demonstrate how the six-PWM-switch average model can be used to obtain the ac responses and compensate the three loops of the Vienna rectifier operating under *dq0* control.

Single-Phase T-Type Boost Converter

Fig. 1 shows a three-level boost converter operated with a bidirectional switch. The configuration is called a T-type converter and the output voltage V_{bus} splits between the two output capacitors C_1 and C_2. For a 265-V rms input voltage, this converter will regulate at 800 V dc, offering the ability to stack two converters individually supplied by the 400-V rails as shown below. This approach lets the designer choose 650-V breakdown voltage types for all transistors, while 1200-V BV_{DSS} types should have been selected with a classical two-level converter featuring an 800-V single-bus voltage.

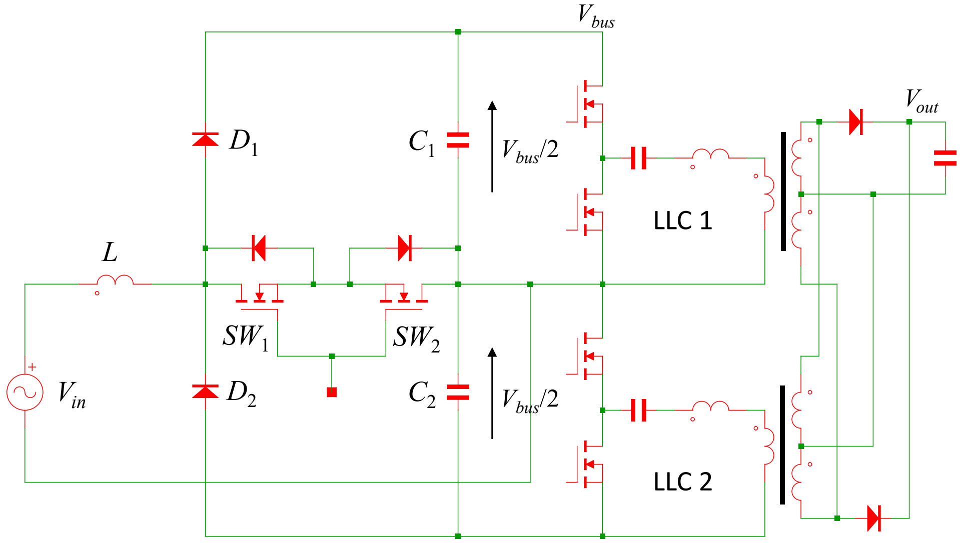

Fig. 1. A three-level converter is perfect for stacking converters and reducing the voltage stress on the semiconductors. Here, two LLC converters are paralleled and supplied by two different primary voltages. But other converter types may also be used here for performing dc-dc conversion and adding isolation.

In this configuration, switches SW_1 and SW_2, are wired back-to-back to offer bidirectionality: when both are turned on, the current can flow in either direction. For instance, when V_{in} is positive, switches SW_1/SW_2 are biased and the input voltage appears across the inductor L. The current rises with a slope given by

$$S_{on} \approx \frac{V_{in}}{L} \qquad (1)$$

When the switches open, the inductive current keeps circulating in the same direction but now finds a path or *freewheels* in diode D_1. The voltage across the inductor reverses, reducing the current with a slope defined by

$$S_{off} \approx \frac{V_{in} - 0.5V_{out}}{L} \qquad (2)$$

The current now circulates in capacitor C_1 and the load. During this event, the two switches block $V_{bus}/2$ or 400 V if the bus voltage is 800 V. When the input polarity changes, the sequence repeats itself as illustrated in Fig. 2. D_2 is now involved in the freewheel action, while the current feeds capacitor C_2 and the load.

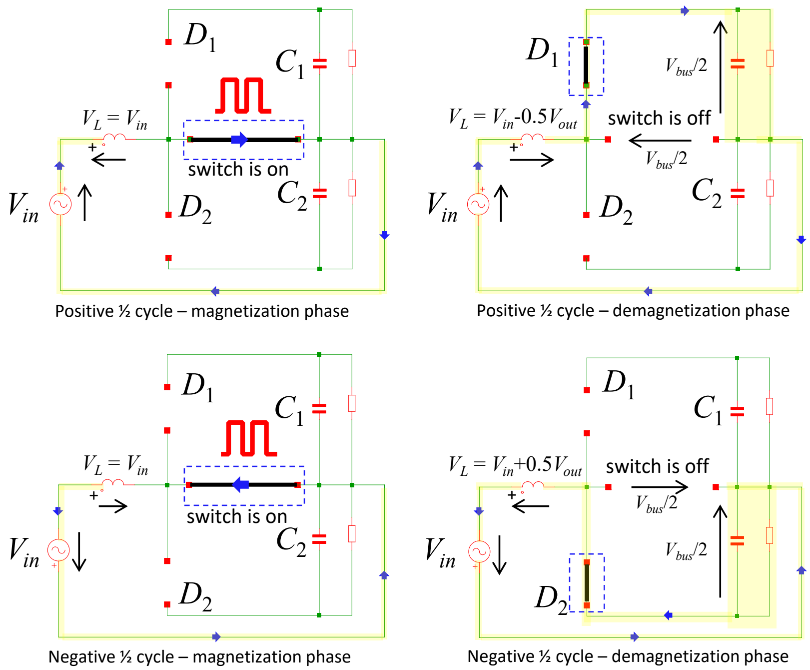

Fig. 2. The bidirectional switch conducts in both directions, depending on the input line polarity.

Diodes D_1 and D_2 can be replaced by two synchronous switches for improved efficiency. In this case, you will need additional logic gates to decode the input line polarity and accordingly route the switching patterns to the synchronous switches placed across D_1 and D_2.

Simulating The T-Type Converter

I have assembled a complete power factor correction (PFC) circuit with LTspice, as shown in Fig. 3, using the variable off-time technique described in reference 2. The circuit is fairly simple to control in this case, and there is no need to sense the input voltage.

The output voltage is regulated with a type 2 transconductance amplifier, automatically compensated by the right-side macro for a crossover frequency of a few hertz. To stabilize this voltage loop, I have first resorted to a SIMPLIS simulation which lets me quickly extract the ac response of a switching converter. However, I have also assembled an averaged model described in the next paragraphs.

The inductor current is sensed via the 0-V dummy source V_1 (see Fig. 3) and mimics what a Hall-effect sensor could deliver. The current is rectified for a negative output and I used the *absolute* (ABS) mathematical function for that purpose.

Analog behavioral source B_1 performs this operation and scales the current with a resistive coefficient R_i. The resulting output voltage then goes through the high-bandwidth current loop built around X_4 whose output drives comparator X_3 for PWM operation. The second input of this comparator receives the timing capacitor sawtooth voltage. The charging current of this capacitor is controlled by the compensator monitoring the error voltage and adjusts the power level delivered by this converter.

This particular example runs with a 110-V input and delivers 400 V for the bus voltage, equally split between capacitors C_1 and C_2 with well-balanced loads. The simulation is reasonable and the 200-ms run took 100 s on my old machine.

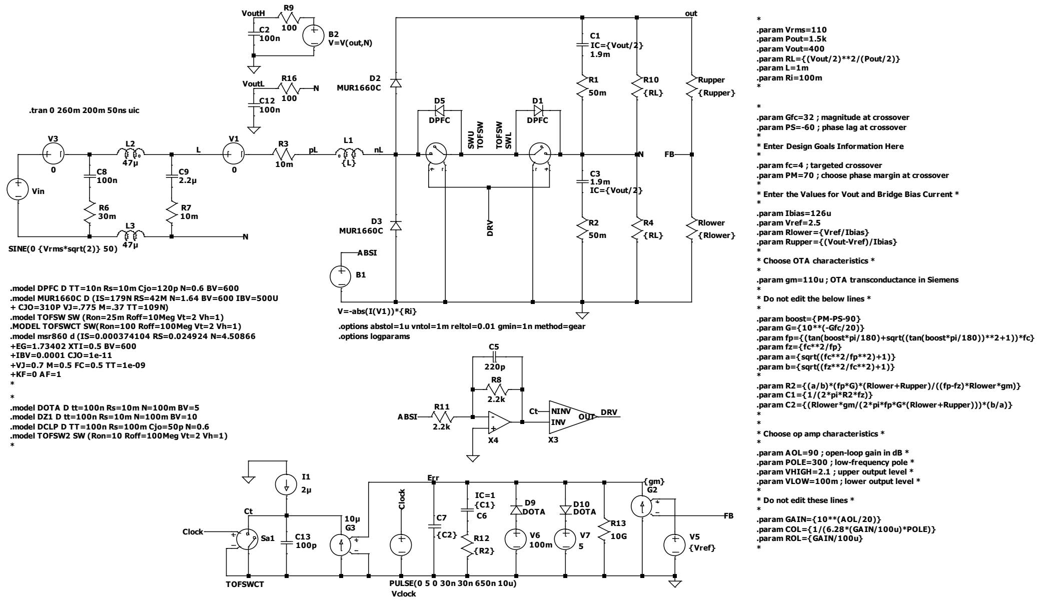

Fig. 3. The 400-V T-type PFC can be simulated with LTspice.

The simulation results are shown in Fig. 4 for this 400-V/1.5-kW converter. The two dc rails are well balanced with a 25-V ripple across each capacitor and the input current exhibits a good total harmonic distortion (THD) of 5.3%. The middle waveform represents the voltage across the inductor which swings through three levels, $V_{bus}/2$, $-V_{bus}/2$ and 0 V.

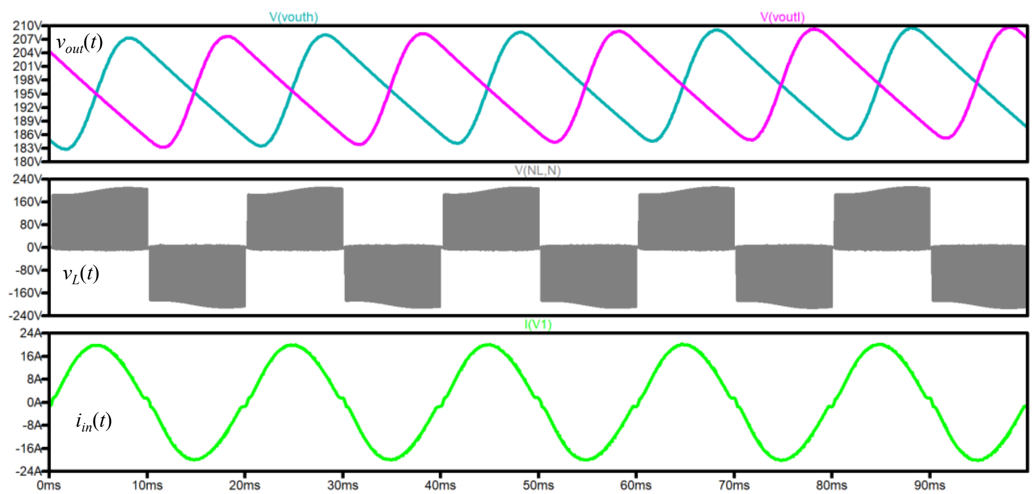

Fig. 4. The voltage across the inductor confirms the three-level type of architecture.

From T-Type Single-Phase To Three-Phase Vienna

The above analysis is relevant because the Vienna rectifier can be broken down into three T-type converters, one per phase. This is something I learned from watching one of Sam Ben-Yaakov's videos.[3] Fig. 5 illustrates how combining these individual T-type circuits leads to the Vienna configuration.

You'll recognize a three-phase diode bridge on the left side and three bidirectional switches feeding a common capacitive bridge. The newly formed converter remains unidirectional but adding synchronous switches across the diode bridge will let you realize a bidirectional inverter. This bidirectional converter is well suited for reinjecting power into the grid, while controlling the reactive power if need be.

I will not go through the operational details of the Vienna rectifiers considering the abundant literature dedicated to this subject. However, I recommend reading references 4 and 5 for an in-depth coverage of three-phase rectifiers.

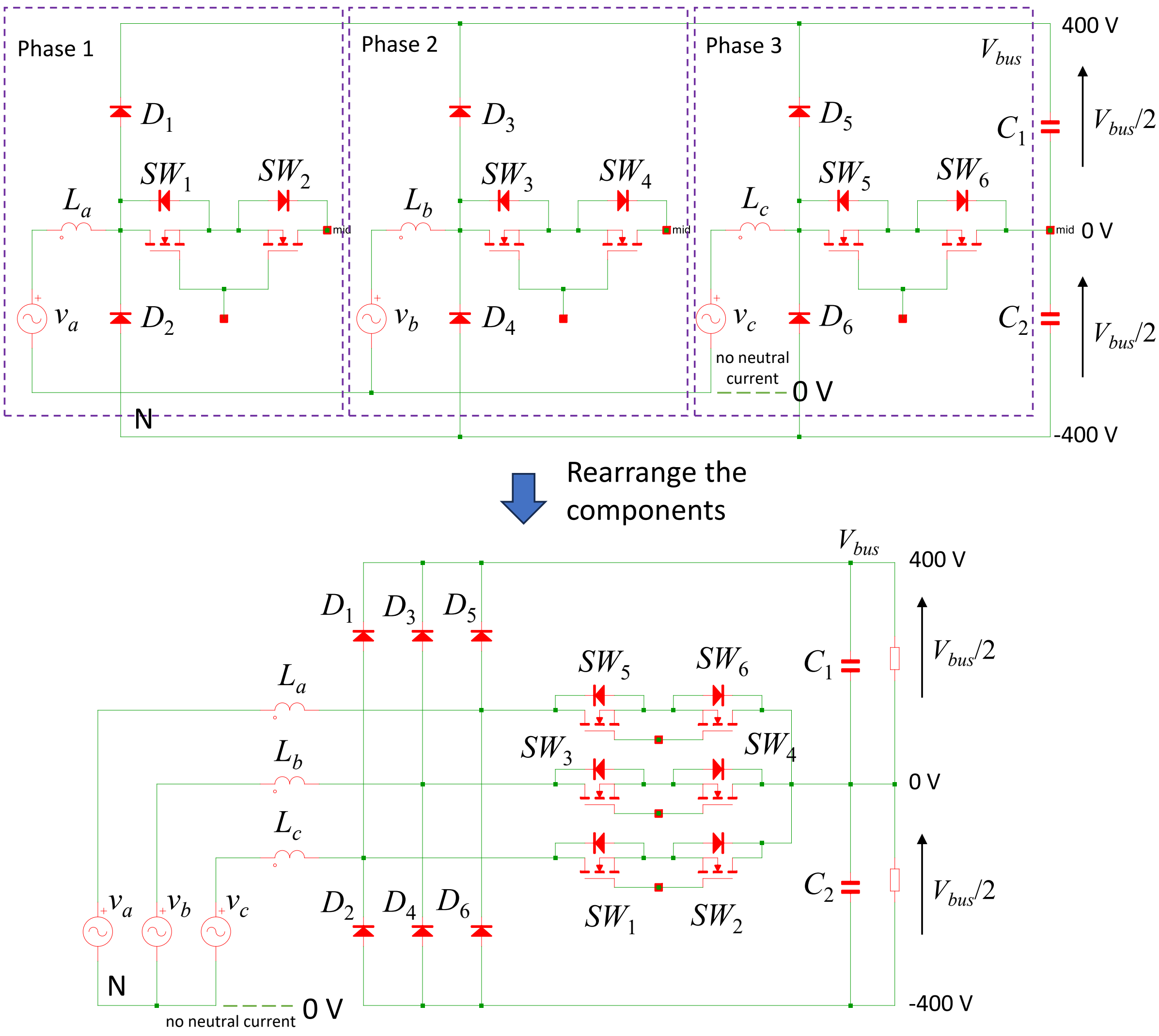

Fig. 5. Gathering three T-type converters and rearranging the layout of the component symbols leads to the configuration familiar as the Vienna rectifier.

In the Vienna structure, the two switches SW_1 and SW_2 (for phase a) are simultaneously driven, which greatly simplifies the control. In my examples, I will use SPWM whose implementation is a center-based, three-phase commutation, identical to SVM type 2. For gaining understanding of these different control types, I recommend reading reference 6, which offers a very comprehensive coverage of these modulation techniques.

Averaged Simulation Of The Single-Phase T-Type PFC

The state-space analysis of the Vienna rectifier is complex, and I will not venture down this path. Rather, I will use the PWM switch model introduced by Vatché Vorpérian in 1986[7,8] and implemented in reference 9 for a three-phase modeling exercise. The difficulty lies in identifying the PWM switches and inserting them in the application circuit. We will first start with an averaged model of the single-phase T-type boost and extend it to the three-phase Vienna in the next paragraph.

During the positive cycle of input source V_{in}, diode D_1 and switches SW_1/SW_2 are active in boosting the voltage. During this time, diode D_2 is blocked. On the contrary, during the negative cycle, diode D_2 and switches SW_1/SW_2 are switching while D_1, this time, is silent. If we gather these subcircuits as in Fig. 6, we can see that two PWM switches will be needed for a single T-type cell.

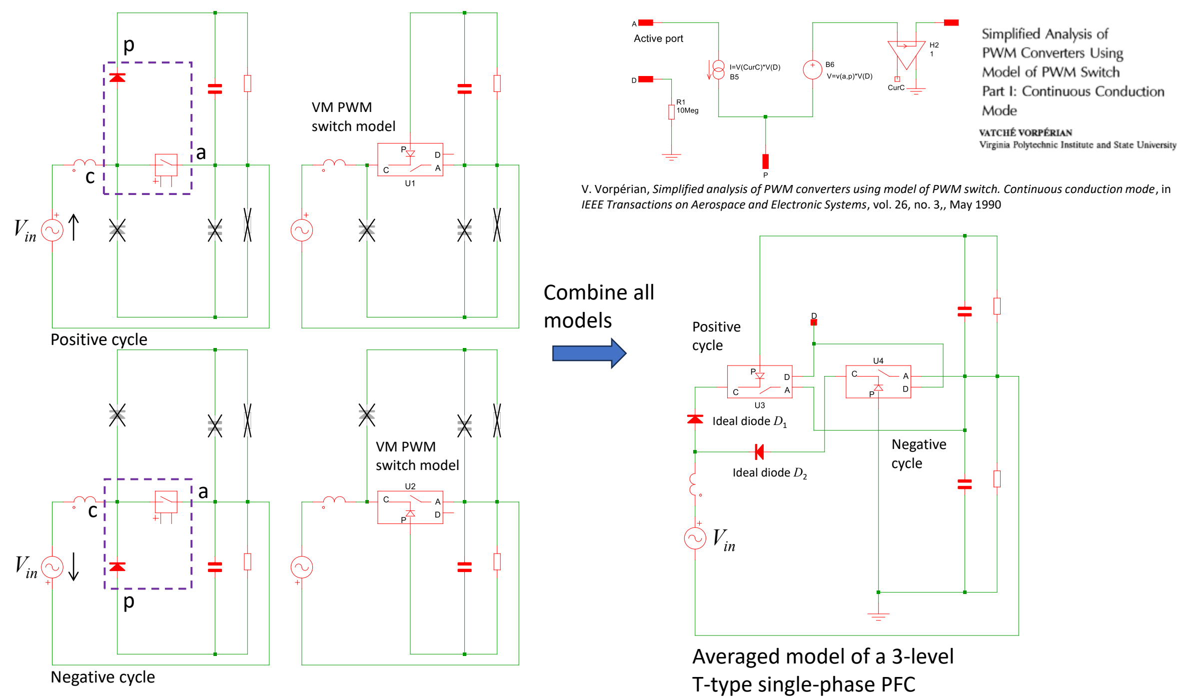

Fig. 6. You first identify a commutating cell during the positive cycle, then a second one during the negative portion of V_{in}. Assemble the two PWM switch models with a series diode and you have the averaged converter model.

For analyzing the control-to-output transfer function of a PFC, we usually choose a dc input voltage equal to the rms value of the ac line at which we want to run the analysis. For instance, if we want to plot the transfer function at a 110-V rms input voltage, we simply dc-bias the averaged model by a 110-V source.

With this information on hand, Fig. 7 shows the typical circuit used for compensating the T-type PFC. You recognize the two PWM switch models to which the modulator section has been added. When running the circuit, always check the important bias points like the bus voltage for instance, and make sure they are within expected limits. If not, it means LTspice has found a wrong operating point, implying useless ac plots.

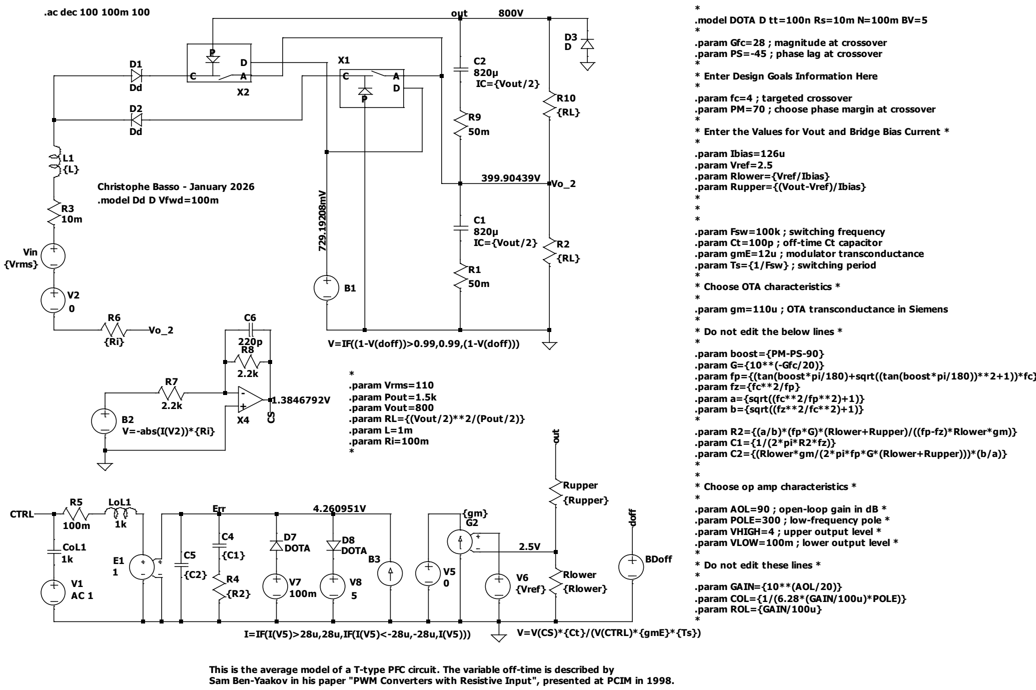

Fig. 7. Averaged models simulate fast for the ac analysis. This is an 800-V inverter and bias points are valid.

After a few seconds, you obtain the ac results displayed in Fig. 8. You first extract magnitude and phase data from the power stage response and enter these values in the macro shown on the right in Fig. 7. The type 2 compensator is automatically designed for the crossover and phase margin goals, 4 Hz and 70° in this case. The compensated loop gain confirms these facts.

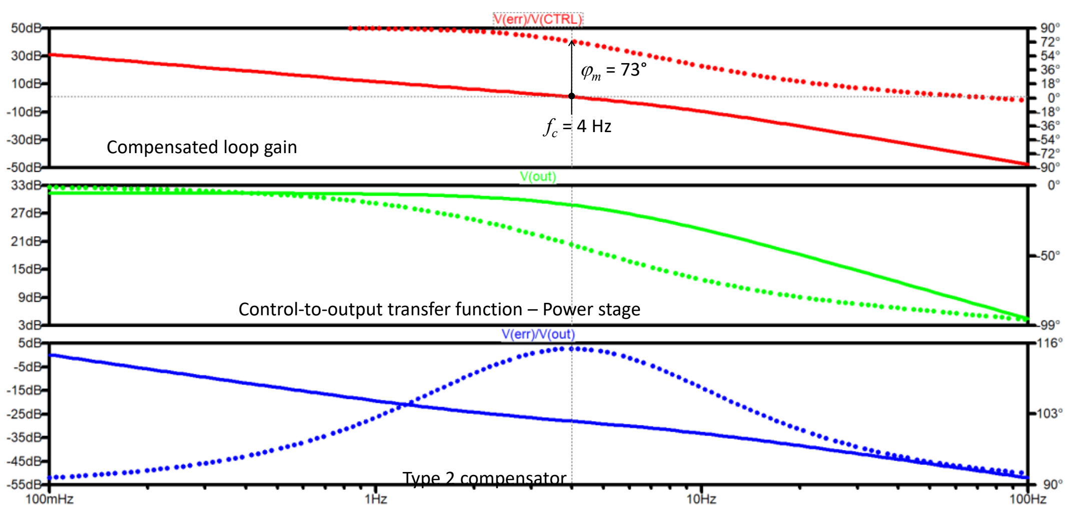

Fig. 8. This ac simulation confirms a 4-Hz crossover frequency at the selected operating point.

I can now run a transient load step using the averaged circuit and compare its response with a cycle-by-cycle version, both converters being identically compensated. The circuit changes a little as we now run a transient simulation with a real sinusoidal source connected to the input, before a front-end EMI filter. Operating the averaged models in transient can be tricky sometimes, as convergence might be at stake with some line/load combinations. In this example, the 800-V output is stepped from 50% to 100% of the 1.5-kW nominal power. Fig. 9 shows how the step load is performed on both dc rails at the same time.

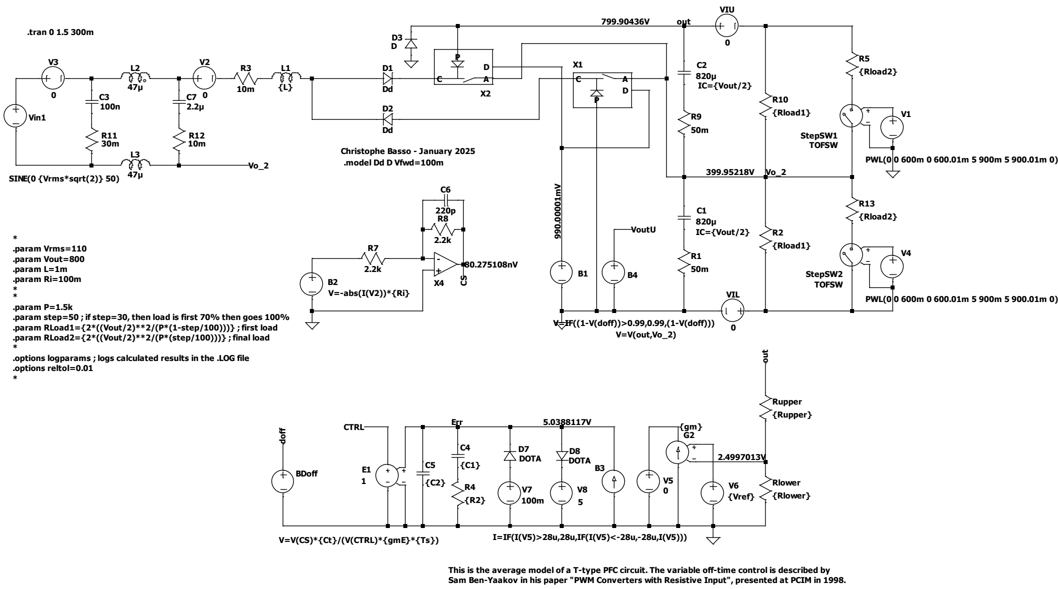

Fig. 9. This averaged model lets you run a transient analysis with a sinusoidal source.

Resistance R_{load1} is loading the converter for 50% of its nominal power. Later on, R_{load2} will come in parallel, loading the converter with 100% of the nominal power.

The switching model from Fig. 10 follows an identical configuration and it is important, for comparison purposes, to be as close as possible to the averaged circuit in terms of selected components.

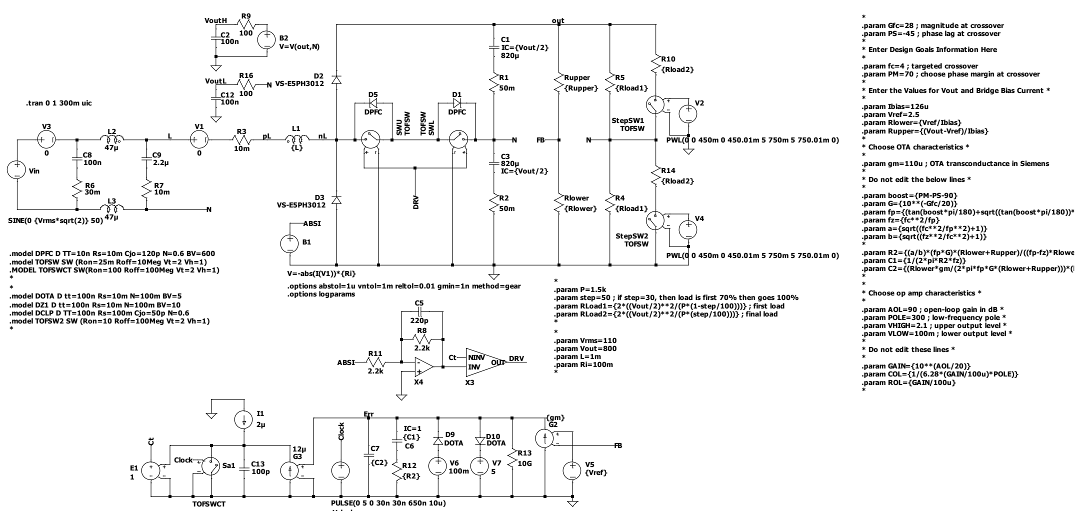

Fig. 10. You can compare the transient response of the averaged model drawn above in Fig. 9 with that of the this cycle-by-cycle, switching model and check that results are close enough.

The simulation of the averaged model is extremely fast for lack of switching component (4 s). The cycle-by-cycle circuit takes a bit more time to complete (380 s) as you need to have all voltages and current well stabilized before applying the output step. The results appear in Fig. 11 and show a very stable response for both averaged and switched models. In principle, I like to superimpose averaged and switching curves to check for a perfect match but LTspice does not support such graphical operations.

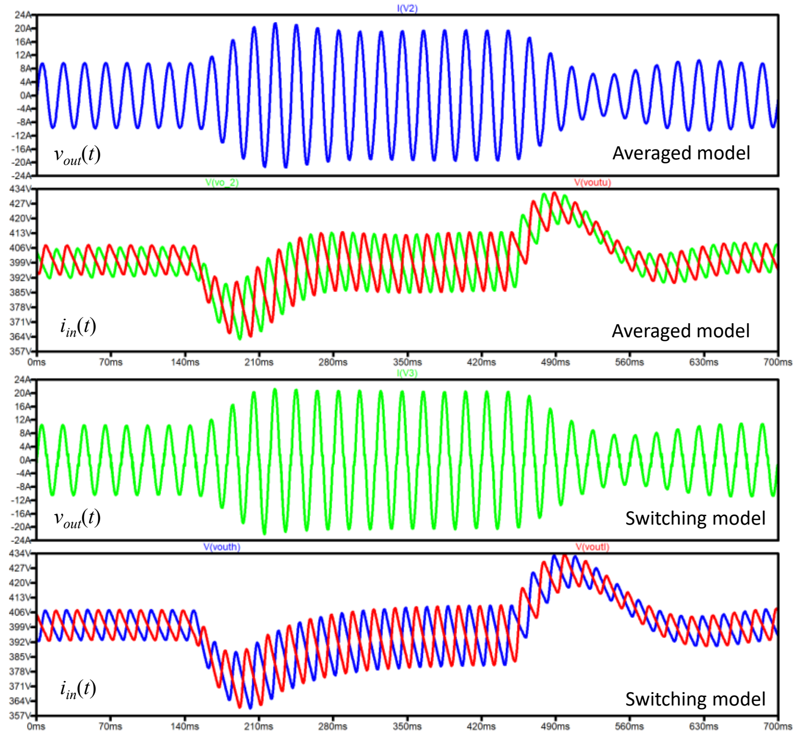

Fig. 11. You can compare the response of the averaged model with that of the cycle-by-cycle version and check that results are close enough.

But even without going through this exercise of superimposing the waveforms in the viewer, I can see that the the two simulations do not match perfectly. Nevertheless the compensation scheme designed with the ac analysis gives excellent results stability-wise with the switching model (that is, the transient response looks good) which is the primary goal here. I have checked the response at 230 V rms and the converter response is also very good with the averaged and switching models.

Averaged AC Simulation Of The Three-Phase Vienna Rectifier

The averaged model of the Vienna rectifier follows the flow detailed in Fig. 6, this time totaling six PWM switch models. The circuit appears in Fig. 12 and now includes the complete SPWM modulation scheme based on *dq0* control.

Needless to say, the burden on the engine for computing the dc operating point can be a challenge. I have tested this circuit with all six PWM switches but also another version with only three of them.

Why can we reduce the complexity? Because we are dealing with three phases whose instantaneous voltages are shifted by 120°. Therefore, depending on the selected input line operating point, the phase voltages can combine different polarities, activating or deactivating a model via its associated diode. The models in series with a blocked diode can simply be temporarily excluded.

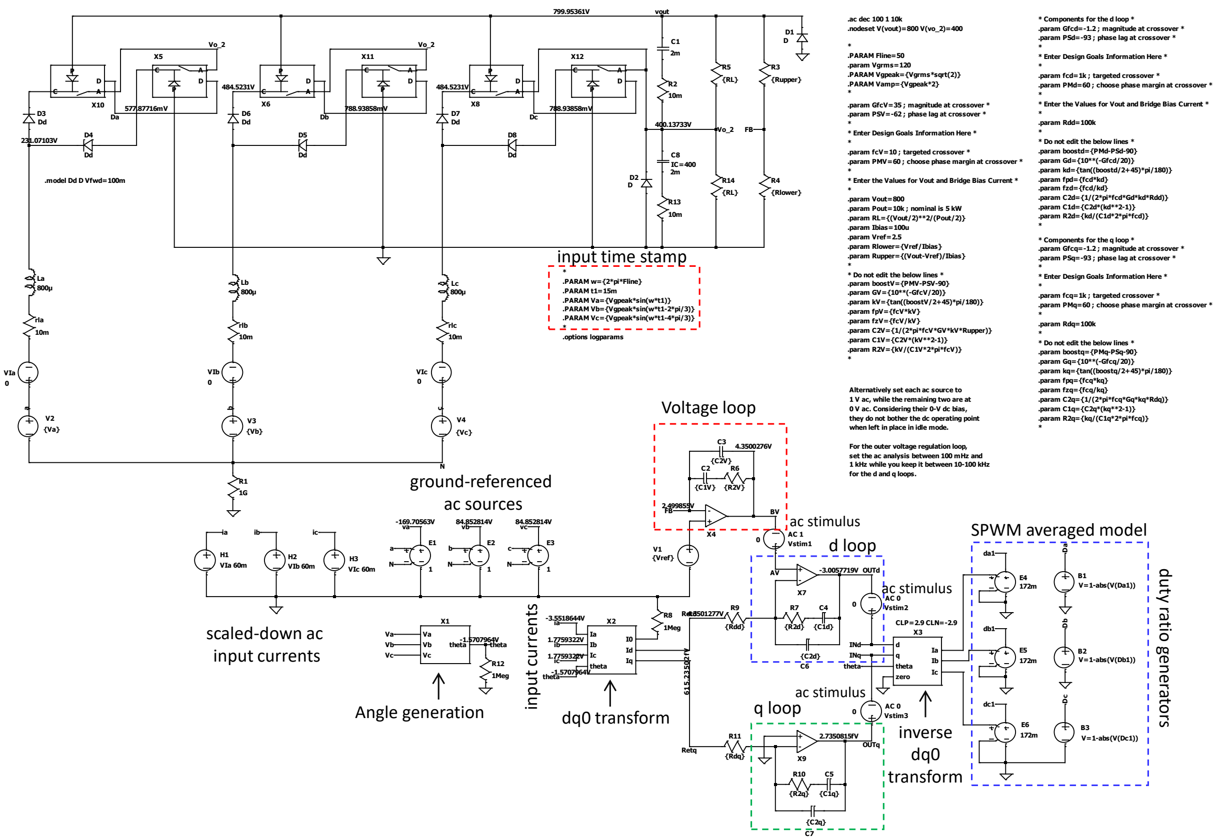

Fig. 12. The averaged model of the Vienna rectifier is quite complicated as it now features six PWM switch models.

If it is easy to choose a dc value for the ac analysis in a single-phase circuit, how do you select the voltages when you have three phases? The trick is to adopt a time stamp t_1 and derive the instantaneous value of each phase at this point. You then assign these values to the dc sources biasing the averaged models. In LTspice, simply insert the following instructions in the schematic:

```
*
.PARAM w={2*pi*Fline}
.PARAM t1=15m
.PARAM Va={Vgpeak*sin(w*t1)}
.PARAM Vb={Vgpeak*sin(w*t1-2*pi/3)}
.PARAM Vc={Vgpeak*sin(w*t1-4*pi/3)}
*
```

I have successfully tested t_1 = 15 ms which gives V_a = -170 V and V_b = V_c = 84.85 V. These values will automatically be passed as parameters to the three dc sources biasing the PWM switch models. As I explained, owing to these combinations, some of the diodes in series with a PWM switch model will either be conducting or blocked, depending on the source polarity. You thus have the possibility to remove some of the unused models and help the SPICE engine to converge better.

In my circuit where only three PWM switch models were active for the 15-ms time stamp, subcircuits X_{10}, X_{11} and X_{12} were deleted. Diodes D_3, D_5 and D_8 were removed while diodes D_4, D_6 and D_7 were shorted. This approach saved me on several occasions when convergence was at stake.

If you decide to explore a different input time stamp where phase voltages would be different, and should you want to delete unused subcircuits, you will have to study which component is active or passive in this mode. For the sake of the example, I have kept all subcircuits in position and it worked well in simulation.

Controlling Active And Reactive Power

As I described in the introduction, there are three active loops in this PFC. One is classically observing the output voltage via an error amplifier, as in any single-phase PFC. One difference here is that there is no 100-Hz or 120-Hz voltage ripple present on the output capacitor. As a benefit, you can extend the crossover frequency f_c beyond the few hertz allowable in single-phase applications. Typical values for a three-phase PFC would be f_c = 80 to 100 Hz for instance.

In a single-phase PFC, the error amplifier output would either drive an inductor current setpoint or change the duty ratio directly via a dedicated modulator. In this three-phase application circuit, the error amplifier will control the active power via the *d*-loop input while another loop involving a third error amplifier monitors the reactive power *q* and keeps it to zero. Explaining how *d* and *q* relate to power is way beyond the scope of this article. However, let me try to explain in a nutshell the basics behind this modulation technique.

Fig. 13 represents the three sinusoidal current waveforms delivered by the grid utility. If you would like to control the three input currents i_a, i_b and i_c, you could certainly think of three distinct PFC loops, each observing the input current and adjusting the current setpoints based on the output power requirements. It is done this way in some cases and it lends itself well to a full analog implementation.

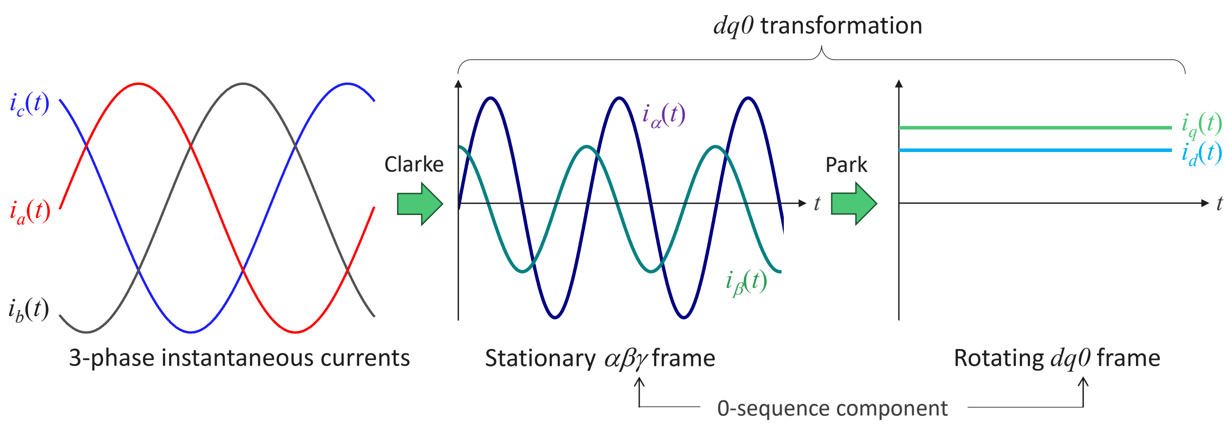

Fig. 13. Controlling the power with three sinusoidal sources complicates the circuitry.

Another approach consists of vector-summing the three input currents to synthetize a single vector, affected by a magnitude and a phase. This new single vector will be represented in a so-called *stationary* plane, characterized by an imaginary y-axis noted β and a horizontal real axis labeled α. So now, rather than observing three variables, we are down to two, the α and β components of the synthesized vector.

The mathematical transformation from a three-dimension rotating abc frame (our three input currents) to a two-dimension stationary frame (the resulting sum vector), is named the *Clarke transformation*, after Edith Clarke,[10] an American electrical engineer, famous for her contributions to our power electronics world in the first half of the twentieth century.

While operating a control loop on a variable setpoint is possible, most of the applications I have seen, resort to an additional transform for generating dc variables labeled *d* and *q* where *d* is for direct axis and *q* is for quadrature axis. This terminology comes from rotating machine theory and I encourage you to dig into the subject should you want to explore three-phase PFC design.

Some details are available in the two seminars I published and available through reference 11. But in short, applying the Park transformation to the vector synthesized by the Clarke process, will lead to extracting the *d* and *q* components of the input currents as continuous values. These continuous values, i_d and i_q, can now be processed by a classical analog or digital loop to control the active and reactive powers.

The flow is described in Fig. 14. It involves trigonometric calculations, implying the need for digital control and a microcontroller. The angle theta is obtained from the input sources via a dedicated phase-locked loop (e.g. a synchronous reference frame PLL or SRF-PLL) and synchronizes the *dq0* process.

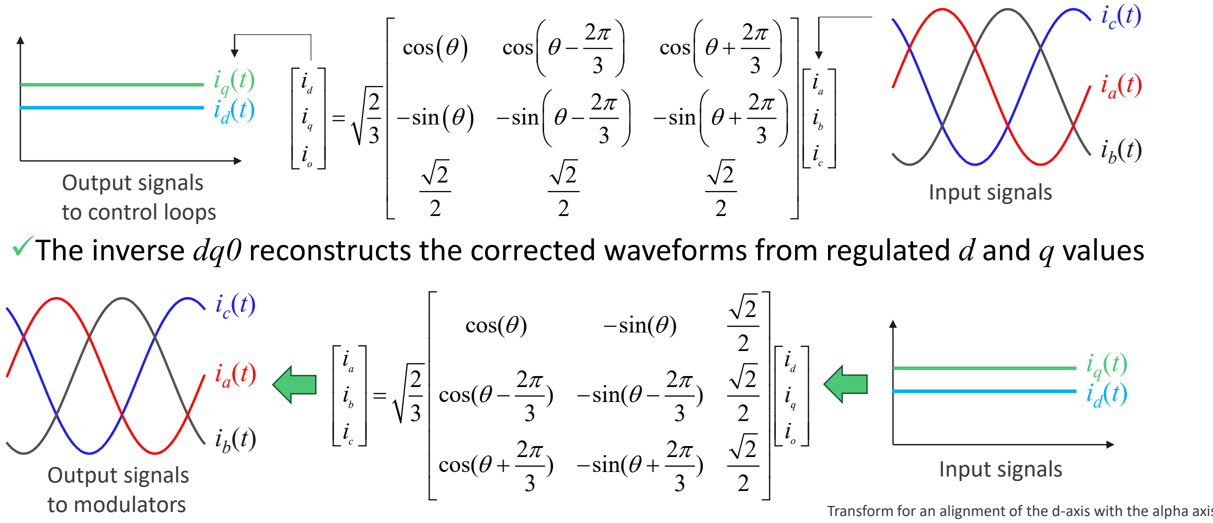

Fig. 14. The dq0 transformation is a power-invariant mathematical tool.

In a classical PFC, you can permanently set *q* to zero or control its value for grid-forming purposes. In that case, you also need to apply the *dq0* transform to the voltage inputs—for obtaining v_d and v_q dc components—then combined with i_d and i_q:

$$\begin{aligned} P &= v_d i_d + v_q i_q + v_o i_o \ [\mathrm{W}] \\ Q &= v_d i_d - v_d i_q \ [\mathrm{VAR}] \\ S &= P + jQ \ [\mathrm{VA}] \end{aligned} \qquad (3)$$

Please note that i_0 and v_0 are so-called 0-sequence components and equal zero in a balanced three-phase system (see part II in reference 11).

AC-Response Of The Vienna Rectifier

In the circuit shown in Fig. 12 (repeated below), you can see three ac sources in series with each error amplifier associated with a particular loop. If we want to sweep the voltage loop, then we turn the ac stimulus V_{stim1} on (AC 1) while the two remaining ones V_{stim2} and V_{stim3} are turned off (AC 0). For the *d*-loop, V_{stim2} is turned on alone and, for the *q*-loop, V_{stim3} is the only active stimulus.

We first extract the control-to-output transfer function of the power stage by plotting V(Vout)/V(AV). The AV node corresponds to the modulator input of error amplifier X_7 in the *d*-loop, while V_{out} refers to the high-voltage bus regulated at 800 V. You read the magnitude and phase data at the selected crossover frequency (80 Hz) and feed the macro for automating the type 2 compensator calculations. The results are given in Fig. 15 and confirm the good compensation strategy.

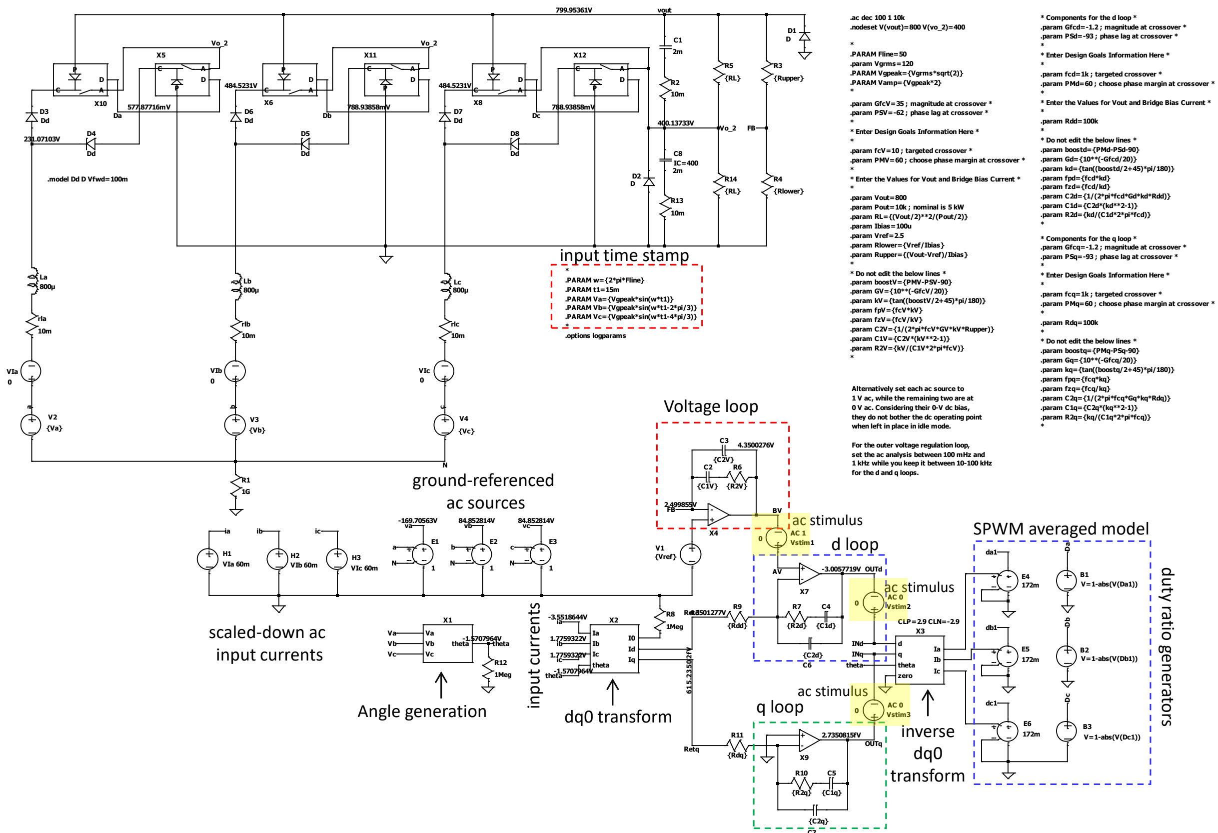

Fig. 12 again. The average model of the Vienna rectifier.

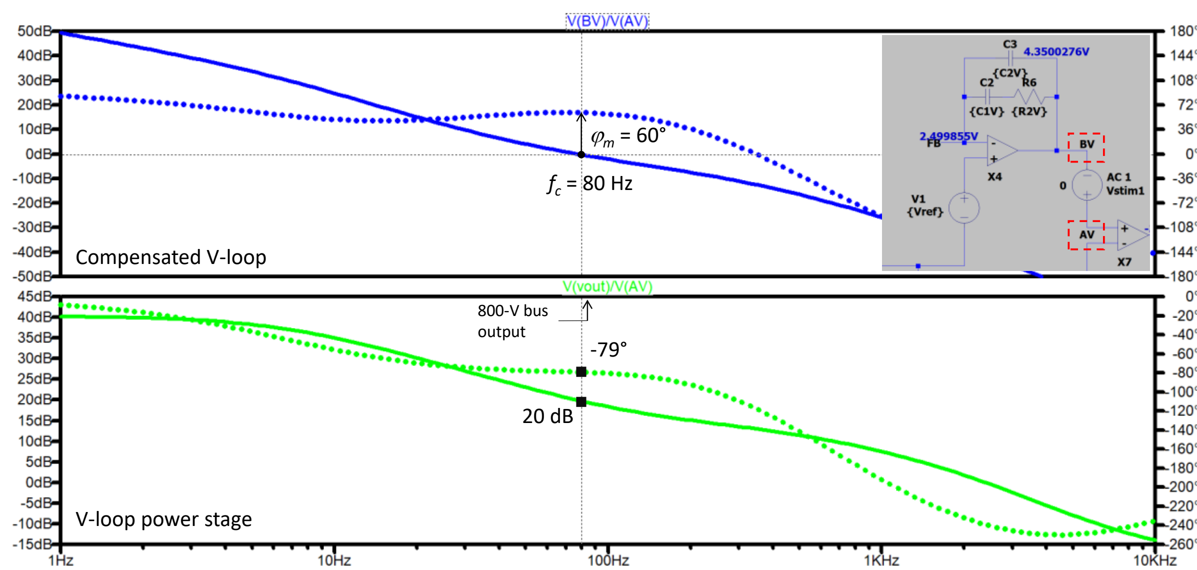

Fig. 15. The voltage loop is compensated for an 80-Hz crossover frequency.

The *d*-loop ac-sweep follows an identical path except that we pushed crossover to 2 kHz in this case. Fig. 16 shows the compensated loop, again, with good phase margin.

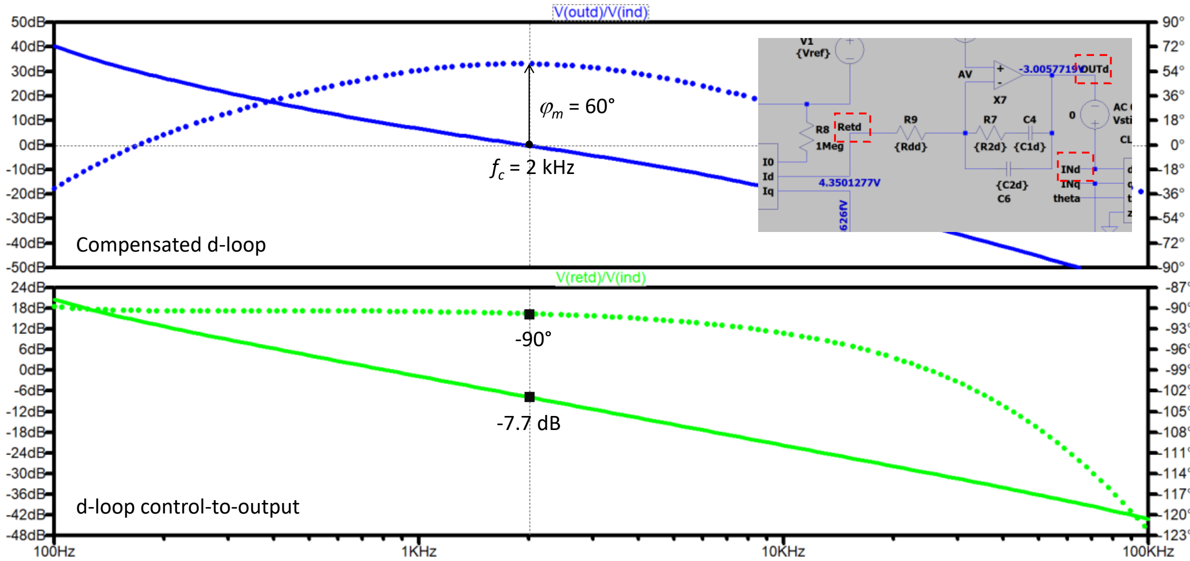

Fig. 16. The d-loop is compensated for a 2-kHz crossover frequency.

Finally, the *q*-loop is also compensated for 2 kHz and it is easy because the *d*- and *q*-loops have identical responses. Fig. 17 confirms the correct compensation scheme with the type 2 compensator.

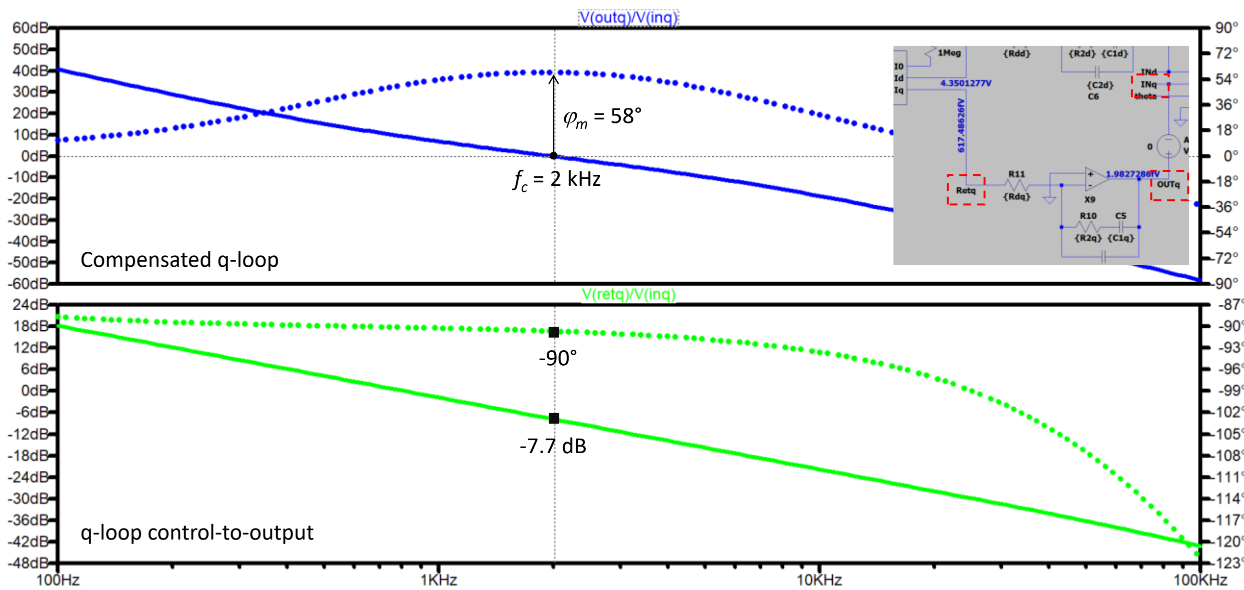

Fig. 17. The q-loop is compensated for an 2-kHz crossover frequency.

The Vienna rectifier is now completely compensated and we can now look at its transient response with sinusoidal input sources.

Sinusoidal Input Generators

Now that the loops are stabilized, we can run a transient analysis to verify the waveforms and check input current distortion. As the PWM switch model is assembled with large-signal equations, you can bias the converter with three sinusoidal generators and check currents and voltages. The simulation is extremely fast for its lack of switching events and that is the great advantage of averaged models (Fig. 18).

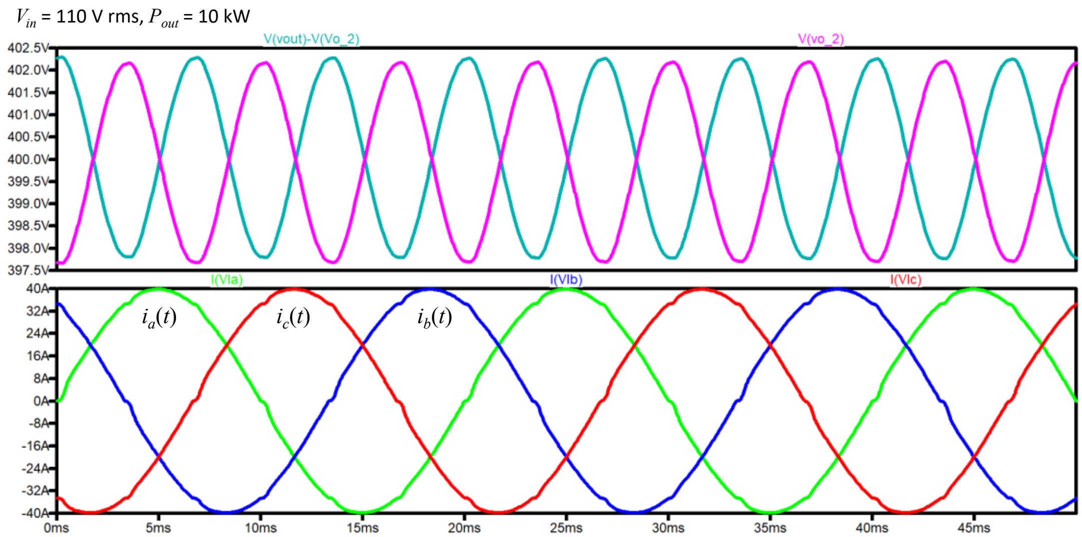

Fig. 18. The input currents are well sinusoidal and both rails remain stable at 400 V.

The total harmonic distortion is determined to be 1.3% at low line. It drops to a theoretical 0.6% at a 230-V rms input voltage. The two dc rails are regulated at 400 V each with a low ripple voltage. It is important to keep these rails well balanced and an additional low-gain loop can be implemented to preserve this equilibrium.

Conclusion

The Vienna rectifier has been the subject of many publications but I could not find a technical paper detailing how to compensate the loops in a simple way. By representing the three-phase Vienna rectifier with six PWM switch models, it is possible to characterize the ac responses of the three loops in a simple and fast way.

All these simulation examples are freely available for download from my webpage.[12] The ZIP file[13] contains more than 200+ ready-made templates covering many different switching converters, including single- and three-phase PFCs.

Acknowledgement

I would like to thank Yang Fu from Shenzhen for the fruitful interaction during the averaged modeling of the Vienna rectifier.

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About The Author

Christophe Basso is a business development manager with Future Electronics, a member of the power team and covering EMEA. Previously, he was a technical fellow with onsemi for 24 years where he originated numerous integrated circuits. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "An Intuitive Guide to Compensating Switching Power Supplies". Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 25 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on compensating power supplies, see the How2Power Design Guide, locate the "Design Area" category and select "Stability". Also, see "Modeling and Simulation". For more on PFC circuits, see the "Popular Topics" category and select "Power Factor Correction".