

SiC Trench-Assisted Planar Technology Enables Performance Gains

[Navitas Semiconductor's](#) fifth-generation GeneSiC technology platform, the high-voltage (HV) SiC trench-assisted planar (TAP) MOSFET technology is said to represent a technological leap over previous generations and is expected to deliver an industry leading 1200-V line of MOSFETs. It complements Navitas' ultra-high voltage (UHV) 2300-V and 3300-V technologies from the fourth-generation GeneSiC platform (see the figure).

The platform achieves a 35% improved $R_{DS(ON)} \times Q_{GD}$ figure of merit (FoM), as compared to the previous generation 1200-V technology. This improvement significantly slashes switching losses, allowing for cooler operation and higher frequency of operation in demanding power stages.

High-speed switching is further fortified by $\sim 25\%$ improvement to the Q_{GD}/Q_{GS} ratio. When paired with a stable high threshold voltage specification ($V_{GS(TH)} \geq 3\text{ V}$), this technology ensures immunity against parasitic turn-on, providing a robust and predictable gate drive even in high-noise environments.

In addition, the fifth-generation technology is said to deliver significant improvement in dynamic performance by optimizing the $R_{DS(ON)} \times E_{OSS}$ characteristic while also integrating a "soft body-diode" technology to further enhance system stability by minimizing EMI and ensuring smoother commutation during high-speed switching cycles.

"AEC-Plus" grade qualification (i.e., results exceeding AEC-Q101 and JEDEC standards) of this generation ensures long-term stability and durability for AI data centers, energy and grid infrastructure applications. Key reliability benchmarks include:

- Extended stress testing: 3x longer duration for static high-temperature, high-voltage testing (HTRB, HTGB, and HTGB-R).
- Advanced switching reliability testing: dynamic reverse bias (DRB) and dynamic gate switching (DGS) to represent stringent fast-switching application mission-profiles.
- Industry-leading stability: lowest $V_{GS(TH)}$ shift over extended switching stress periods for stable long-term efficiency, according to the vendor.
- Extreme gate-oxide reliability: extrapolated gate-oxide failure time exceeding 1 million years at operating V_{GS} at 18 V and 175°C.
- Enhanced cosmic ray resilience: exceptionally low FIT (failure in time) rates, ensuring mission-critical reliability in high-altitude and high-uptime environments

A white paper on trench-assisted planar technology is available for free download from the Navitas website. For further information on this technology, contact the [company](#).

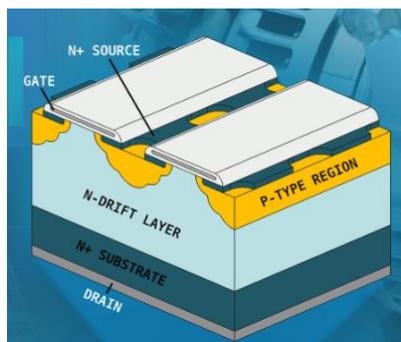


Figure. Navitas Semiconductor's fifth-generation MOSFET platform features the company's most compact TAP architecture yet, combining the ruggedness of a planar gate with best-in-class performance figures of merit, says the vendor. This is enabled by a trench structure in the source region. The end benefit is an increase in the efficiency and lifetime reliability for high-voltage power electronics.