# *A Deeper Look At Current-Steered (Ćuk) Magnetic Circuits*

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Current-steered (Ćuk-class) circuits involve some subtle behaviors of the magnetic component in power-transfer circuits. This article presents and explains those that are significant in converter design with magnetic ripple-current steering. These subtleties rarely appear in any of the power-electronics literature, including major power-electronics textbooks or accessible engineering papers or articles.

In a previous article, I offered an explanation of Ćuk-circuit power recirculation.[1] Current steering is recounted here from reference 1 with embellishment and taken farther to include power input-port voltage range in circuit design. Some other subtle anomalies include Ćuk and DCM resonances and current-notching.

The purpose of this discussion is to give designers a more detailed understanding of Ćuk circuit operation so that they can avoid potential pitfalls in designing Cuk power circuits. For example, it will offer some guidance on sizing of inductor and coupling capacitor based on how power is circulated within the converter, and the effects of input voltage range. With regard to the explanations of resonances and current-notching, recognizing these effects may help designers avoid noise sources.

## *Current Steering*

*Current steering* is associated with its use in the Ćuk "converter," a class of power-transfer circuit topologies that have some common subtle characteristics. All Ćuk-class or current-steered circuits operate with the transductor straddling the magnetic boundary between coupled inductor and transformer behavior. These two behaviors are labeled when winding fields aid as "coupled inductor" and with fields opposing as "transformer".

These are *behaviors* of a multi-winding magnetic component that *structurally* lacks a general name; I call it a *transductor*. The same component can behave as either coupled inductor or transformer yet it has the same structure. In current-steered circuits the transductor straddles the line between the two behaviors within each switching cycle.

Current steering is a circuit technique[2] that is based on bootstrapping from two voltage sources across parallel circuit loops, as shown in Fig. 1.

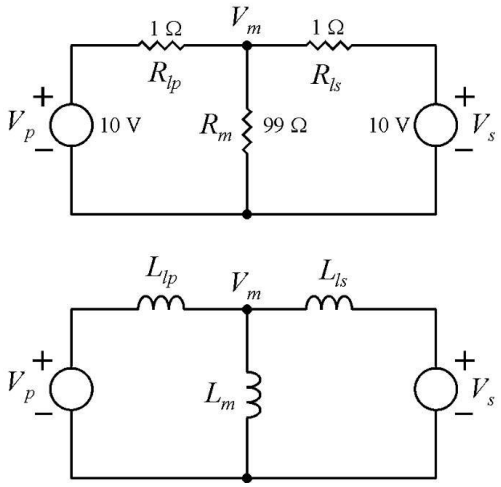



*Fig. 1. The upper resistive circuit is analogous to the lower transductor circuit where two windings are being driven by near-equal voltage sources. A slight change in voltage from $V_p = V_s$ of either causes a large change in total current between the two sources.*

The static component of *field currents* (currents referred to the field by winding turns $N$ as $N{\cdot}i$) of the windings aid as in a coupled inductor, and the ripple components oppose as in a transformer. To understand Ćuk-class transductor behavior we start with a simpler circuit, a resistive divider circuit (Fig. 1, upper) with two equal voltage sources driving resistors $R_{lp}$ and $R_{ls}$ corresponding to leakage inductances and a common (mutual) resistor $R_m$.

Because in a transductor leakage inductances $L_{lp}$ and $L_{ls}$ are typically much smaller than the shared mutual inductance $L_m$ between windings, the corresponding resistive circuit $R_{lp}$ and $R_{ls}$ are much smaller than $R_m$ and connect to it at the center node, forming two voltage dividers with $R_m$.

The currents from the sources flow through $R_m$ in the same direction and aid as in a coupled inductor. A small variation in either $V_p$ or $V_s$ will cause a large change in the fraction of current that each source supplies to $R_m$. If $V_p$ were to increase to 10.1 V, it would raise the voltage at $V_m$ from 9.95 V to 10 V, causing the current through $R_{ls}$ to be zero, and all $R_m$ current would then be supplied by $V_p$.

By raising $V_p$ sufficiently, all $R_m$ current is supplied by $V_p$, and the current through $R_{ls}$ also reverses and flows into $V_s$ with $V_p$ supplying currents through $R_{ls}$, $R_{lp}$ and $R_m$. The circuit behaves like that of a transformer; one source supplies both mutual current through $R_m$ and transfer current to the other side, through $R_{lp}$ and $R_{ls}$.

Similarly, in the lower circuit of Fig. 1, the leakage inductances of the transductor windings are much smaller than the mutual or magnetizing inductance $L_m$. By increasing primary voltage source $V_p$ the voltage at $V_m$ increases, thereby bootstrapping $L_{ls}$ just as $R_{ls}$ was bootstrapped.

The voltage at each end of $L_{ls}$ is the same, causing $i_{ls}$ = 0 A, and its inductance is effectively infinite. Consequently, all variations in magnetizing current (through $L_m$) caused by varying $v_m$ is supplied by the primary winding source. $V_p$ is set relative to $V_s$ by adjusting turns ratio $n$. This *current-steering* effect eliminates winding ripple from the secondary winding, resulting in ripple-free or constant winding current. The same scheme can be implemented for the primary circuit.

In the literature (including reference 3) it is sometimes suggested that by adding an external inductance to adjust the winding voltages that the same result can be obtained, but this is not so. True bootstrapping can only be achieved by an adjustment in the turns ratio between windings so that the source bootstrapping the other has a slightly higher voltage.

## Ćuk-Switch Power Flow

One of the behavioral characteristics of current-steered transfer circuits is recirculating power of the power components. This power flow is consistent with the Ćuk-class of PWM-switch common-inductor (CL, buck-boost, flyback) circuits.

The power requirement of the inductor in buck (CP) and boost (CA) circuits is less than the transfer power between input and output ports because the input port supplies some of it. But in the CL, all transfer power is conveyed through the inductor, and this applies to the Ćuk-class transfer circuits.

The coupling capacitor $C_c$ also must be rated for the full transfer-circuit power. This full-power requirement of the power components is a disadvantage and a tradeoff for the benefit of CCM current at power ports.

With constant voltages and currents at the input ($\pm V_g$, $\pm I_g$) and output ($\pm V_o$, $\pm I_o$) ports and with no power loss within the power-transfer circuit, port power is

$$P_g = V_g \cdot I_g = P_o = V_o \cdot I_s$$

Steady-state power at both ports is constant, and the average power values for the circuit with CCM input and output are

$$\overline{P}_g = P_g \;\; ; \;\; \overline{P}_o = P_o$$

$P_g$ and $P_o$ are the on-time amplitude values for CCM and with the small-ripple approximation. The energy change in the magnetizing inductance $L_m$ of the transductor within a switching cycle of period $T_s$ is

$$\Delta W_L = I \cdot \Delta\lambda = I \cdot (L_m \cdot \Delta I) = I \cdot V \cdot \Delta t$$

$V$ and $I$ are the average CCM values of approximately constant winding voltage and current. The per-cycle energy change in the coupling capacitor is

$$\Delta W_C = V \cdot \Delta Q = V \cdot (C_c \cdot \Delta V) = V \cdot I \cdot \Delta t$$

The $\Delta W$ can be normalized by $T_s = 1/f_s$ as $\Delta W/T_s$ so that $\Delta t/T_s$ becomes either $D$ for the on-time interval or $D' = 1 - D$ for the off-time interval. Then the quantities are expressed as energy per cycle period $T_s$, or power.

Power flow can be illustrated as a block diagram, shown in Fig. 2. The middle block is the power-transfer circuit. Ideally, input and output powers are equal, and the circuit exchange of power with reactances—$P_L$ for $L_m$ and $P_C$ for $C_c$—must be a net zero for each switching cycle. Whatever energy is stored by $L_m$ or $C_c$ (modeled ideally as having infinitely large storage capability) must be exchanged between them per cycle and remain internal to the circuit for steady-state operation.

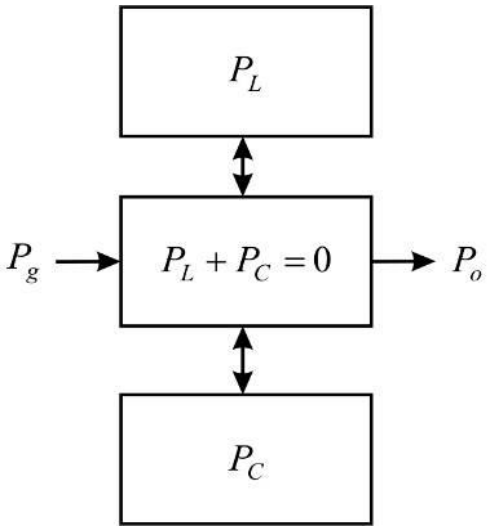



*Fig. 2. Power-flow conservation in lossless transfer circuit.*

The per-cycle energy flows (as per-cycle power) are shown in Fig. 3. Beginning at the upper-left, the input power during on-time is $D \cdot V_g \cdot I_g$ and is input by $L_m$, shown as the flow $P_g \rightarrow P_L$. The Ćuk-circuit primary winding is switched across $V_g$ and the only place input energy can go is into the transductor as part of $P_L$. During off-time, input power (second row) is $D' \cdot V_g \cdot I_g$ shown as $P_g \rightarrow P_C$ and is input instead to coupling capacitor $C_c$. Then the average input power is

$$P_g = D \cdot V_g \cdot I_g + D' \cdot V_g \cdot I_g = V_g \cdot I_g$$

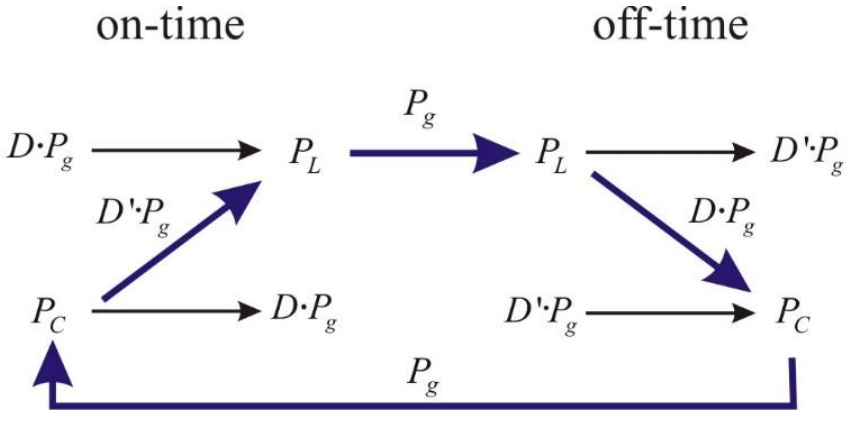



*Fig. 3. Power as energy per cycle shown over a cycle. Input port is to the left and output to the right. Power transfer through $C_c$ as $P_C$ involves both on-time and off-time of cycle, completing a recirculating power loop.*

Similarly, output power during on-time is supplied by $C_c$ ($P_C \rightarrow P_o$, second row) and by the transductor during off-time ($P_L \rightarrow P_o$). These intervals of power add to give the cycle average of $P_o = V_g \cdot I_g = P_g$. During on-time, the secondary circuit outputs $P_o = D \cdot V_o \cdot I_s$ supplied by $C_c$ as it discharges by $I_s$, shown as $P_C \rightarrow P_o$. It flows through $C_c$, the secondary winding, and the output port.

The capacitor also sources on-time power to $L_m$ ($P_C \rightarrow P_L$) from the flow of $I_s$ through the secondary winding. This power is positive (out of $C_c$ as it discharges) and negative during off-time as $C_c$ charges. The on-time power transfer from $C_c$ to windings with $V_g$ across them and conducting $I_s$ from $C_c$ is $D \cdot I_s \cdot V_g$. Applying the circuit steady-state current-transfer relation to $I_s$,

$$D \cdot I_s \cdot V_g = D \cdot \left[ \frac{D'}{D} \cdot I_g \right] \cdot V_g = D' \cdot P_g$$

During off-time $L_m$ transfers power to $C_c$ ($P_L \rightarrow P_C$) with $V_o$ across the windings and conducting $I_g$;

$$D' \cdot I_g \cdot V_o = D' \cdot \left[ \frac{D}{D'} \cdot I_s \right] \cdot V_o = D \cdot I_s \cdot V_o = D \cdot P_o = D \cdot P_g$$

Over the cycle the average power flow between $L_m$ and $C_c$ is $(D' + D) \cdot P_g = P_g$. The power flows of the on- and off-times have opposite polarity for both reactances, but power polarity does not affect power magnitude. The components must be rated to handle the magnitude of power, coming or going.

During on-time, power flowing from $C_c$ back into the transductor from the secondary circuit ($P_C \rightarrow P_L$) combines with power into $L_m$ from $P_g$ ($P_g \rightarrow P_L$), resulting in

$$P_L = D \cdot V_g \cdot I_g + D \cdot V_g \cdot I_s = D \cdot V_g \cdot (I_g + I_s) = D \cdot V_g \cdot I_L \ , \ I_L = I_g + I_s = \frac{I_g}{D}$$

Applying both input and output converter transfer functions,

$$P_L = D \cdot V_g \cdot (I_g + I_s) = D \cdot V_g \cdot \left[ \left( \frac{D'}{D} + 1 \right) \cdot I_g \right] = V_g \cdot I_g = P_g$$

$$P_L = D \cdot V_g \cdot (I_g + I_s) = D \cdot \left[ \frac{D'}{D} \cdot V_s \right] \cdot \left[ \left( \frac{D}{D'} + 1 \right) \cdot I_s \right] = V_s \cdot I_s = P_o$$

The transductor power $P_L$ is equal to the transfer power. When efficiency is included, $P_g > P_o$. The circulation of power in Ćuk-class transfer circuits maintains CCM currents at the cost of inefficiency, for circulating power causes loss within the circuit that is not transferred between ports.

### *Circulation Of Power*

A closer examination of the power flows shows that there is a cyclical *circulation of power*, as shown by the highlighted power transfer paths in Fig. 4. As $P_L$ carries over from on-time to off-time $P_C$ is also carried over from off-time to on-time as the same power ($P_C \rightarrow P_C$);

$$P_C = D' \cdot I_g \cdot (V_g + V_o) = D \cdot I_s \cdot (V_g + V_o)$$

The two expressions are equal because they reduce (by canceling $V_c$ from both sides) to the current transfer ratio based on charge balance. This circulation of power within the circuit between its two reactances completes the power loop and for power balance

$$P_L + P_C = 0 \text{ W}$$

The power-flow diagram in Fig. 4 shows that power is circulating between $L_m$ and $C_c$. The power circulating in this loop is shown by the diagonal transfers between reactances. When summed over the cycle, the average circulating power is

$$P_{circ} = D \cdot I_s \cdot V_g + D' \cdot I_g \cdot V_o = D \cdot I_s \cdot (V_g + V_o) = D' \cdot I_g \cdot V_C = P_g$$

$$V_C = V_g + V_o = \frac{V_g}{D'}$$

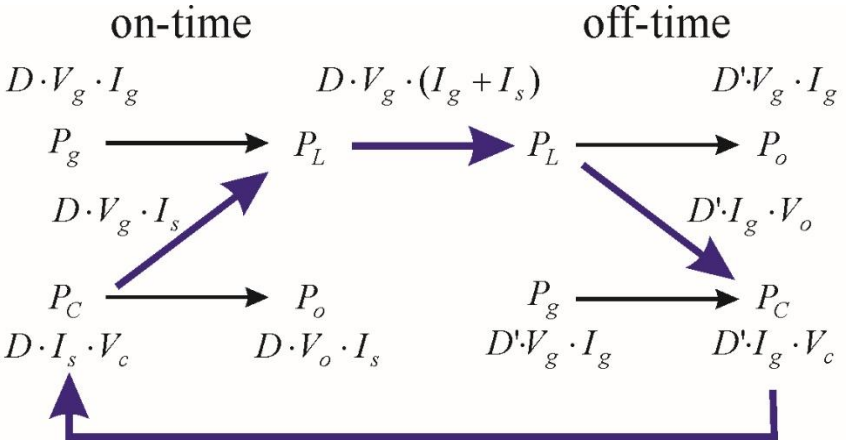



*Fig. 4. Highlighted circulating power in Ćuk-class power-transfer circuits is as much as the transfer power.*

The power that the transductor transfers each cycle is a combination of input-port power and power stored in $C_c$ from the previous cycle, split by $C_c$ voltage. During on-time, power is delivered to the output from $C_c$ while $C_c$ also transfers power through the secondary circuit to the transductor, with $P_L$ split between currents. During off-time, the transductor delivers power to the output while inductor and input transfer power to $C_c$. The power transferred through the circuit between power ports is $P_g$ and equals the circulating power. Hence, the power ratings for both transductor and $C_c$ are $P_g$, the circuit power-transfer rating.

Ćuk-class circuits all have transfer ratios of the form $D/D'$, the same as the PWM-switch CL configuration. The transfer of power from input to inductor during on-time then inductor to output during off-time results in the $D/D'$ characteristic. The power-flow diagram (Fig. 4) for the Ćuk circuit shows this same behavior, though included with it is the parallel transfer from $C_c$, which makes both port waveforms CCM.

## *Reactance Power Ratings Over $V_g$ Range*

The power ratings of transfer power $P_g$ for the transductor and coupling capacitor from the ideal analysis are complicated somewhat in actual design by *ranges* of $V_g$ and $V_o$ or $I_s$ over which the transfer-circuit can be operated. Usually the transfer-circuit converter output is a fixed voltage or current with a maximum power specification, and only the range of $V_g$ need be taken into design consideration given max $P_o$. $V_g$ has an input voltage range of

$$V_g \in [V_{g\min}, V_{g\max}]$$

Average power is

$$\overline{P} = V \cdot \bar{i}$$

$V = V_g$ is constant. Thus average current is $\overline{i_G}$ averaged over the cycle. (The RMS current only applies if both voltage and current are varying in time.) Average total $i_G$ is related to the on-time current amplitude $I_g$ as

$$I_g = \bar{i}_G / D$$

During on-time or off-time intervals, current amplitudes vary because of current ripple, but if the small-ripple assumption holds, this amplitude is approximately the average of the current over the on- or off-time interval. The Ćuk-class circuit average input power from the power-flow graph is thus

$$P_g = D \cdot V_g \cdot I_g = V_g \cdot (D \cdot I_g) = V_g \cdot \bar{i}_G$$

At constant input power $\bar{i}_G$ will vary inversely with $V_g$ so that if $V_g$ has a range of

$$r = \frac{V_{g\max}}{V_{g\min}} = \frac{\bar{i}_{G\max}}{\bar{i}_{G\min}}, \text{ constant } P_g$$

so does $\bar{i}_G$. However, the transductor is fixed in structure and must be designed to accommodate both $I_{g\max}$ and $V_{g\max}$ though neither occur at the same time. Because of these inverse ranges, the transductor (and capacitor) must be overdesigned. The goal is to derive a formula for the required design power given a range of $V_g$.

If the circuit design is specified to exceed some minimum efficiency $\eta$ then the maximum average input design power is $P_o/\eta = P_g$, and

$$\bar{i}_g = \frac{P_g}{V_g}$$

The input current range is thereby determined. Ordering the extreme values to correspond with those in $V_g$, it is

$$\bar{i}_g \in [\bar{i}_{g\max}, \bar{i}_{g\min}]$$

If $\eta$ is constant with power, then the maximum output power will correspond to maximum input power: a voltage-source output at the maximum $\bar{i}_s$ or a current-source output, at the maximum $V_o$. The resulting maximum average $P_o$ and a chosen minimum $\eta$ yields the maximum average $P_g$, but not the *design* $P_g$ of $P_{gd}$.

$\bar{i}_{g\max}$ occurs at $V_{g\min}$ and sets transductor wire size. At $V_{g\max}$ the converter controller reduces $D$ to maintain $\Delta\lambda$ at the maximum $\Delta\lambda$ of the transductor. For maximum $P_o$ the maximum $P_g$ at any operating-point within the ranges of these variables is constant ($I_g$ is average amplitude of the on-time current) at

$$P_g = (D \cdot V_g) \cdot (\bar{i}_g + \bar{i}_s) = (D \cdot V_g) \cdot \left(\frac{\bar{i}_g}{D}\right) = D \cdot V_g \cdot I_g$$

For the *design power* rating of the transductor, the voltage and current factors must be at the range maximums:

$$P_{gd} = (D_{\min} \cdot V_{g\max}) \cdot \left(\frac{\bar{i}_{g\max}}{D_{\max}}\right) = V_{gd} \cdot I_{gd}$$

The $D$ values for the Ćuk circuits are found from the transfer equations by solving them;

$$D = \frac{M}{M+1} = \frac{V_o/V_g}{V_o/V_g + 1} = \frac{V_o}{V_g + V_o}$$

Then at the extrema required by design

$$D_{\min} = \frac{V_o}{V_{g\max} + V_o} \;;\; D_{\max} = \frac{V_o}{V_{g\min} + V_o}$$

$V_{gd}$ is maximum at $V_{g\max}$ and $I_{gd}$ is maximum at $V_{g\min}$; the $D$ values are derived from these voltages. The design formula for $P_{gd}$ is simplified by substituting for $D$;

$$P_{gd} = (D_{\min} \cdot V_{g\max}) \cdot \left(\frac{\bar{i}_{g\max}}{D_{\max}}\right) = \left(\frac{D_{\min}}{D_{\max}}\right) \cdot (V_{g\max} \cdot \bar{i}_{g\max}) \Rightarrow$$

$$P_{gd} = \frac{V_o + V_{g\min}}{V_o + V_{g\max}} \cdot P_{g\max}$$

Maximum power can be expressed at minimum $V_g$ as

$$P_g = V_g \cdot \bar{i}_g = V_{g\min} \cdot \bar{i}_{g\max} = (V_{g\max}/r) \cdot \bar{i}_{g\max} = P_{g\max}/r$$

Or equivalently, at the maximum-$V_g$ operating-point

$$P_g = V_g \cdot \bar{i}_g = V_{g\max} \cdot \bar{i}_{g\min} = V_{g\max} \cdot (\bar{i}_{g\max}/r) = P_{g\max}/r$$

Then the expression for $P_{gd}$ simplifies to a design formula for the power rating of each reactance;

$$P_{gd} = \frac{V_o + V_{g\min}}{V_o + V_{g\max}} \cdot \left(\frac{V_{g\max}}{V_{g\min}}\right) \cdot P_g \quad \Rightarrow$$

$$\frac{P_{gd}}{P_g} = \frac{1 + \dfrac{V_o}{V_{g\min}}}{1 + \dfrac{V_o}{V_{g\max}}}$$

The power-ratio formula makes explicit how many times greater the power rating of the reactances must be than that of the maximum specified input power. This power-rating rationale can be applied to other types of power-transfer circuits by substituting their $M(D)$ function and carrying out a similar formula derivation.

The capacitor rating is easier to derive. The rated voltage must exceed $V_{g\max} + V_{o\max}$. The rated current is the RMS current through the capacitor which can be derived from $D$, $D'$, $I_g$, and $I_s$. During on-time, the current is $I_s = I_g \cdot (D'/D)$, and is $I_g$ during the off-time. The current waveform is a bipolar square-wave having RMS value

$$\tilde{i}_c = \sqrt{D \cdot [I_g \cdot (D'/D)]^2 + D' \cdot I_g^2} = I_g \cdot \sqrt{D'/D} = \sqrt{I_g \cdot I_s}$$

Insight into power flows in the Ćuk-switch simplifies a causal understanding of its behavior and results in useful component power formulas.

The other current-steered PWM-switch configurations have the same general power-flow scheme except that input and output port terminals are exchanged in various combinations. For instance, the SEPIC configuration is a Ćuk with swapped output terminals, the Ćuk-switch CA (zeta) circuit has swapped input terminals, and the inverse Ćuk-switch CA swaps terminals at both ports.

### *Other Ćuk-Class Anomalies*

For dynamics and control considerations, the circulating power between reactances constitutes a resonant circuit, that of the *Ćuk resonance*. Ideally, the Ćuk frequency is at 0 Hz and does not exist, but when leakage inductances of actual transductors are included, they resonate with $C_c$ at the frequency and impedance of the total leakage inductance (winding to winding) and $C_c$.

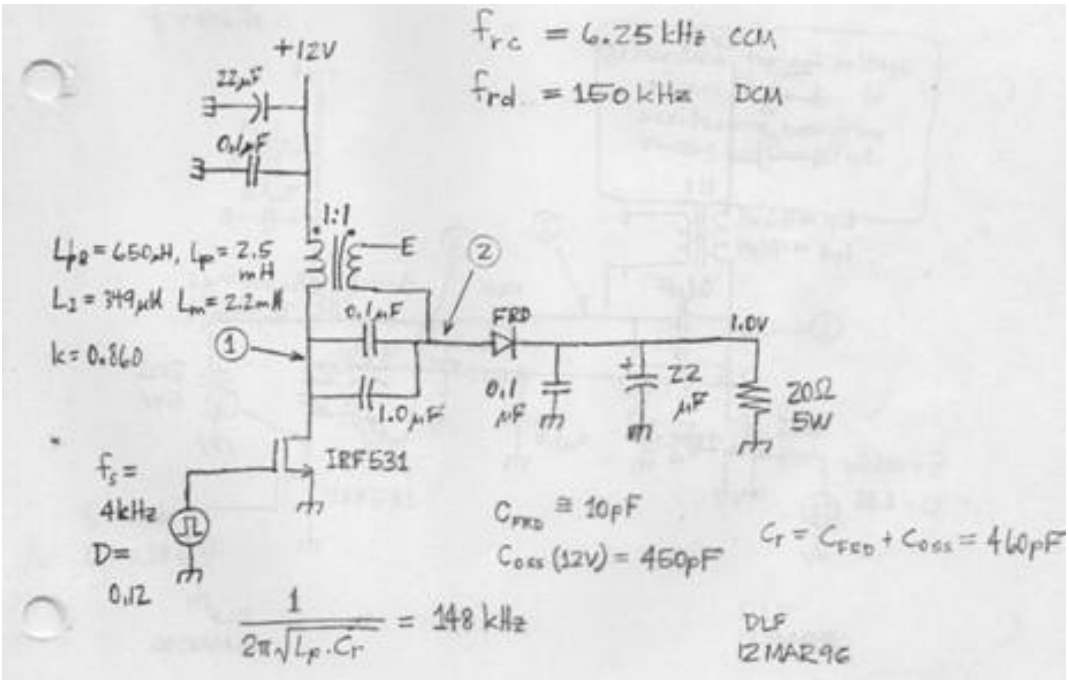
The circulating power is the power exciting the resonance. The Ćuk resonance can be damped with resistance in series with $C_c$ which is typically a large capacitor, often an electrolytic type having large series resistance that damps the resonance.

Besides the doubling of ratings of power components to handle both transfer and circulating power, current-steered transfer circuits also require $C_c$, an additional capacitor that must be large enough so that the voltage ripple across it is negligible. For this article, it was assumed to be "large" in capacitance and also have a voltage rating that is the sum of the port voltages.

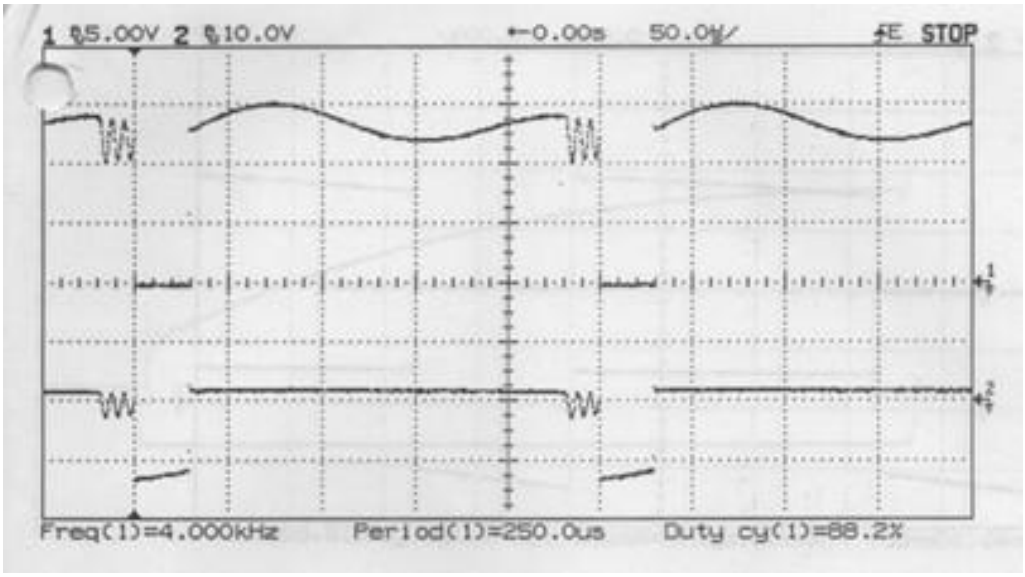
Aluminum electrolytic capacitors first come to mind, but they have relatively large series resistance, resulting in significant power loss at higher power. Plastic film capacitors are usually used instead, but they are large and costly.

An ideal capacitor with no series resistance poses a different problem, that of resonance with $C_c$ and the leakage inductance of the transductor. Series resistance in $C_c$ tends to damp it, and a compromise tradeoff between low power loss and undamped *Ćuk resonance* confronts the designer.

Another subtle behavior in Ćuk-class transfer circuits is another resonance besides the Ćuk resonance, shown in Fig. 5. There is no way to avert the power-switch off-capacitance, and it resonates with the transductor. In the Fig. 5 case, it fails to appear when the circuit is operated at a normal switching $f_s$ = 50 kHz. It appears when the circuit becomes DCM, and this can occur for other parameter values, not only for low switching frequency.




*(a)*




*(b)*

*Fig. 5. At an artificially low switching frequency of 4 kHz, both the Ćuk resonance at $f_{rc}$ and the higher $f_{rd}$ from the off-time MOSEFT $C_{ds}$ and $L_p$ resonance (noted in (a)) are evident in the oscillograph (b) before on-time commences.*

Last but not least there is the more common yet subtle *current-notch* problem that occurs in isoĆuk (isolated Ćuk-class) transfer circuits. Fig. 6 shows the basic isoĆuk topology—the isolated PWM-switch common-inductor (CL) transfer circuit with primary and secondary current steering. When on-time of the transfer circuit ends, Q switches off, and the only path for primary current $i_p$ is through the lower primary-ripple winding.

During on-time both windings are driven by a voltage of close to $V_g$—the primary winding from the supply and the ripple winding $i_{rp}$ from $C_{cp}$. At Q shut-off $i_p$ and $i_{rp}$ are opposing each other! The voltages across the primary-side windings have also changed and current is now being transferred to the secondary windings. The upper secondary winding delivers $i_s$ to the output while the secondary ripple winding charges $C_{cs}$.

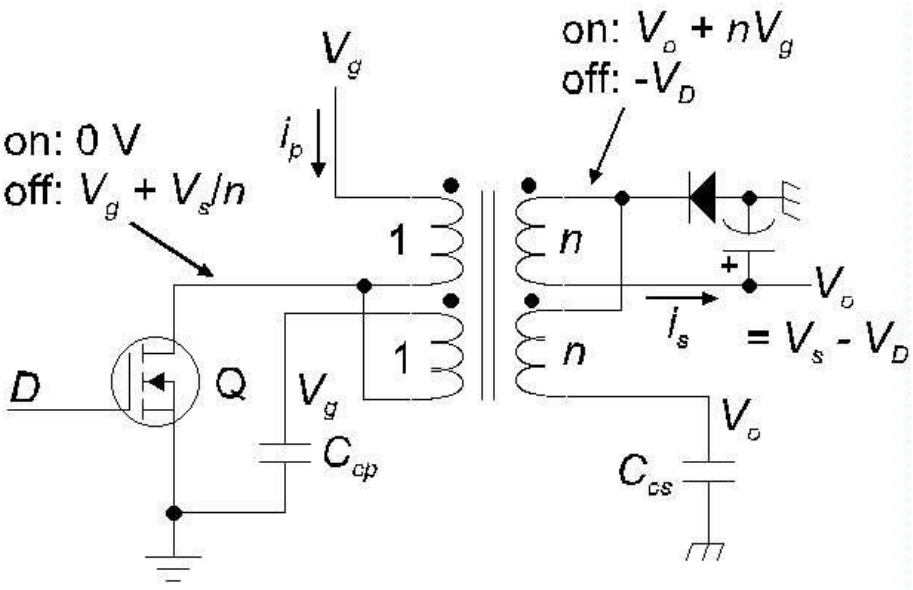



*Fig. 6. Basic topology of the isoĆuk isolated PWM-switch common-inductor (CL) transfer circuit with current steering on both primary and secondary sides of the circuit.*

What happens on the primary side is that the center-tap voltage rises until the voltage across both leakage inductances is reversed and they both deflux. The primary-side windings are bifilar wound with high coupling. Their leakage inductances are close to equal in value, causing them to deflux at the same rate until the current is zero at the $i_p$ notch in Fig. 7.

Then $i_r$ reverses and charges $C_{cp}$ from $V_g$ through the upper winding that continues to conduct $i_p$ unidirectionally. The current notch appears at the input port and defeats the quest for ripple-less port currents. It is fixed by adding a series inductance to the input port of $i_p$ so that the effective leakage inductance for $i_p$ is much larger than for $i_r$. The port side defluxes more slowly than the ripple-winding leakage inductance, and the $i_p$ notch is essentially removed.

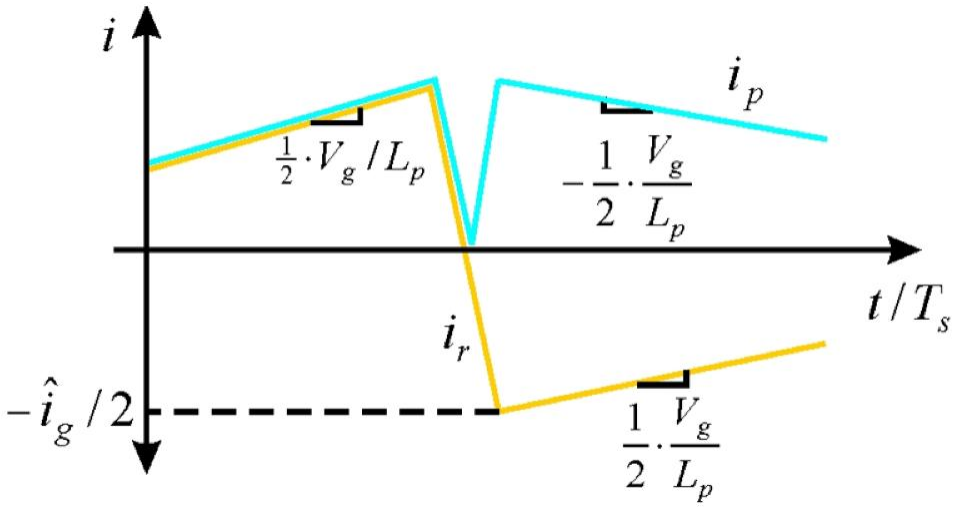



*Fig. 7. Current notch in primary current $i_p$ when ripple current $i_r$ in primary-side ripple winding reverses, and the leakage inductances of both windings deflux at equal rates together to zero before $i_r$ reverses. A current notch can also occur on the output.*

The additional input-port series inductance is a ripple eliminator through $i_p$-notch elimination, but this is not the same ripple reduction as current-steering! The additional inductor also contributes some ripple reduction simply as an inductor but it does not effect the bootstrapping of current-steering which requires a turns-ratio adjustment of $n \neq 1$ so that the winding absorbing the ripple can increase the transductor center-node to the same voltage as the source of the ripple-free winding.

What is also sometimes overlooked is that in the circuit of Fig. 6, the upper primary and secondary windings behave toward each other as a coupled inductor—that of the basic Ćuk topology—while the lower ripple-steering windings on primary and secondary sides function as a transformer. They have the same voltages at their dotted ends, indicating a transformer, and the coupled-inductor windings have the opposite voltages of a flyback circuit at their dotted terminals.

If the two pairs are not integrated onto a common core, then each of them as a discrete magnetic component can be optimized as inductor or transformer; the magnetic design optimizations are not the same! The design tradeoff is reduced magnetics count versus optimized magnetics components.

## Closure

The more subtle behaviors of Ćuk-derived circuits go beyond Ćuk-class circuit simulations[3] and can cause design-related failures in performance. Analytical knowledge of these detailed behaviors is an advance toward avoiding them and in understanding in detail how the magnetic component functions in ripple-current steering.

**References**

1. "Understanding Power Flow In Cuk Converters" by Dennis Feucht, How2Power Today, December 2015.
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## About The Author

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