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Fast AC Line Dropout Detection Can Enhance AC-DC PSU And System Performance

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Ac utility power is often unsteady, and brief outages can lead to IT system resets, data loss, or malfunctions. This makes rapid ac fault detection crucial for supporting continuous power flow, identifying power failures in a timely manner, and preventing prolonged downtime, particularly in servers and industrial equipment.

In server PSUs, rapidly detecting ac loss allows for a safe and energy-efficient ride-through of the fault event, especially when the outage duration doesn't exceed one cycle of the line frequency. Additionally, it ensures safe IT system operation during extended ac sags and facilitates orderly shutdowns or smooth transitions to backup power, which prevents critical data corruption.

In managing ac line transient fluctuations, the PSU, for its part, must maintain a holdup time (HUT) sufficient for a smooth transition to a backup energy source. As noted in reference 1, fast ac fault detection can drastically reduce this transition time. Furthermore, establishing a link between the ac fault detector and the IT equipment—allowing for a PSU load control when the ac feed status is abnormal—presents significant opportunities to enhance both PSU and system performance.

Detection methods based on the usage of a virtual signal monitoring the integrity of the actual ac input are suitable for consistent ac signal parameters, which rarely occur in real-world applications. Because these digital methods involve measuring the ac RMS voltage, frequency, and phase to create a reference signal, they require a mandatory time delay to complete the process. This measurement typically takes at least one cycle of the line frequency, which causes lags in conditions where frequency and magnitude are variable. Furthermore, the actual specified ac wave distortion creates additional challenges in the implementation of the virtual sinusoidal signal approach.

This article examines the implementation of fast analog ac dropout detection and discusses the associated benefits for PSUs and the IT systems they power. We begin by explaining the operation of the basic fast ac fault detection technique. We then discuss how the ac sag detection time can be shortened and how feeding the ac fault signal to the IT system allows for the usage of fast-blow fuses, while reducing their potential tripping. Such fuses are capable of quick circuit breaking during overcurrent, minimizing equipment damage, and preventing fire hazards.

We then show how ac dropout detection enables the use of smaller bulk filter capacitors or, alternatively, achieves higher PSU efficiency with existing capacitor sizes. This involves using the fault signal generated by the improved ac fault detector to temporarily throttle back the power consumed by the load. Finally, we demonstrate how usage of this technique can support ac redundancy in a 2+0 PSU configuration when an ac feed fails, and the load exceeds the power rating of a single module.

Fast AC Fault Detection

One efficient method for fast ac fault detection is used in the SmaRT (Smart Ride Through) technique, whose benefits are described in reference 2. This technique was originally introduced to improve ac dropout ride-through conditions for server power supplies and to minimize the PSU bulk capacitor size.

The detector functional block diagram is shown in Fig. 1. In this arrangement, the sensed rectified ac voltage is divided down and filtered of switching noise with the R1-R2-C1 network. The detector operates by comparing this signal against a dc threshold, V_{REF}. A logic signal is generated when the comparator pulse duration exceeds a predetermined time. This duration is monitored using a high-frequency clock counter, as shown in Fig. 1.

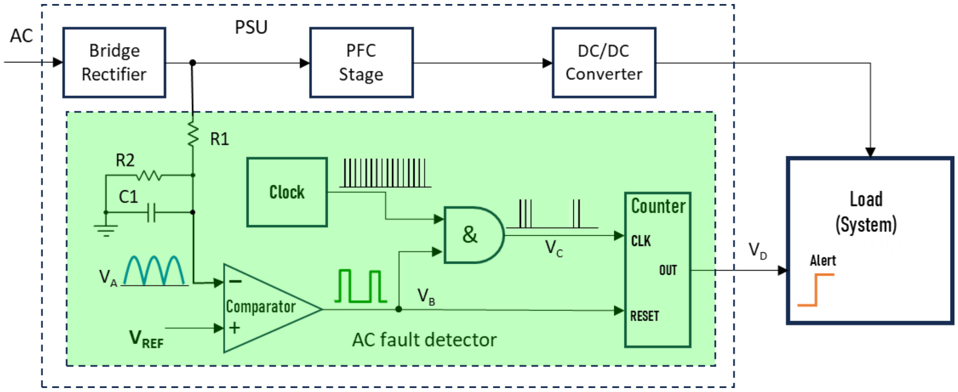
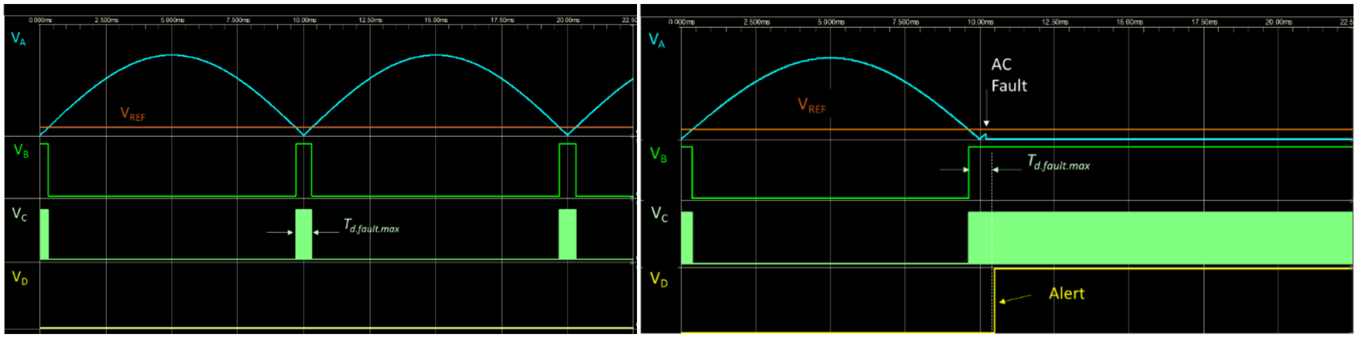


Fig. 1. Ac fault detector functional block diagram (highlighted in green).

The terminal count signal is asserted once the counter reaches its preset or maximum value. The operational waveforms are illustrated in Fig. 2. Under normal operating conditions (Fig. 2a), the comparator pulse duration does not exceed the preset value, and the Alert signal remains low (deasserted). When the comparator pulse duration exceeds the preset value:[1]

$$T_{d.fault.max} = \frac{\sin^{-1} V_{REF}/V_m}{\pi f}$$

where V_m is the ac voltage magnitude, and f is the line frequency, the PSU asserts the Alert signal (V_D in Fig. 2b—in this and subsequent timing diagrams, the alert signal is shown active-high for illustrative purposes).



(a)

(b)

Fig. 2. Ac fault detector operational waveforms. In normal operation (a): the instantaneous ac line voltage remains below the threshold for less than $T_{d.fault.max}$. When the Alert signal is asserted (b), the instantaneous value of the ac voltage remains below the threshold for longer than the time interval $T_{d.fault.max}$.

The lower the V_{REF} level, the faster the ac fault can be detected. In real applications, for noise immunity, V_{REF} can be reliably set between 5% and 10% of the lowest operating voltage magnitude. So, assuming the worst-case $V_{REF}/V_m = 0.1$ and min line frequency $f_{min} = 47$ Hz, we find that $T_{max} = 0.678$ ms, so the determined $T_{d.fault.max}$ value can be considered the maximum time of ac dropout detection.

In the ac sag case, the worst-case detection time will include the time of the instantaneous rectified ac voltage exceeding the dc threshold $t = (\pi - 2\sin^{-1} V_{REF}/V_m)/2\pi f$ which brings the maximum sag detection time:

$$T_{d.sag.max} = (\pi + \sin^{-1} V_{REF}/V_m)/2\pi f$$

close to a half cycle of the ac line frequency (T/2).

Since the PFC stage of a PSU operates over a wide range of instantaneous input voltage levels, the ac voltage sags that do not reach zero may represent a thermal or input fuse overstress issue. When slow-blow fuses are used and the detection time of those sags does not exceed a few tens of milliseconds, such overstresses won't occur, and the detection time not exceeding, say, a period of line frequency can be considered acceptable.

Accelerated AC Sag Detection

In some cases, when a fast-blow input fuse is selected to provide rapid IT equipment protection and prevent fire hazards by quickly cutting power, ac line sag detection can prevent the fast-blow input fuse from unnecessarily acting, which would require operator involvement for the fuse replacement. For such a case, a slightly modified ac line sag detection technique with a higher sampling rate can be used.

Since the Earth ground isolated standby (housekeeping) supply is practically available in all PSUs powering IT equipment applications, the ac sag and dropout detection can be obtained by processing the line signal right at the ac input. To shorten the detection time interval, we need to increase the number of times per cycle the ac signal is measured for digital conversion, i.e., to increase the sampling rate.

This can be achieved by monitoring a proxy signal representing the following function, equal to a sum of the absolute values of the original signal and its derivative:

$$F(x) = |V_m \sin x| + |V_m \cos x\,|$$

where V_m is the monitored signal magnitude, x is the instantaneous phase at time t, $x = 2\pi f t$. This function has a period of $\pi/2$, which allows for sampling the ac signal at a double rate as compared to the rectified ac voltage signal shown in Fig. 2. This reduces the worst-case sag detection time to T/4.

If the $\sin x$ signal represents the divided ac input voltage signal, the $\cos x$ component can be obtained from it by simple differentiation, i.e., by processing this signal at a very low power level via an op-amp-based derivative amplifier, similar to the technique used for accurate ac voltage peak detection.[4] This process of obtaining the proxy signal is illustrated in Fig. 3. In that case, absolute value networks acting as full-wave rectifiers[5] and a summing amplifier will generate the signal *F(x)* given above.

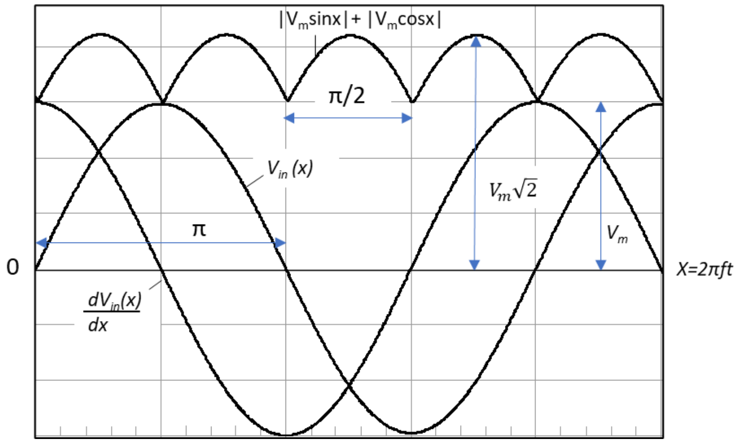


Fig. 3. Reducing the worst-case sag detection time to T/4 (x = π/2) by processing the sum of the absolute values of the original signal $V_{in}(x)$ and its derivative $dV_{in}(x)/dx$. Monitoring the proxy signal can double the sampling rate of the supply's instantaneous ac voltage.

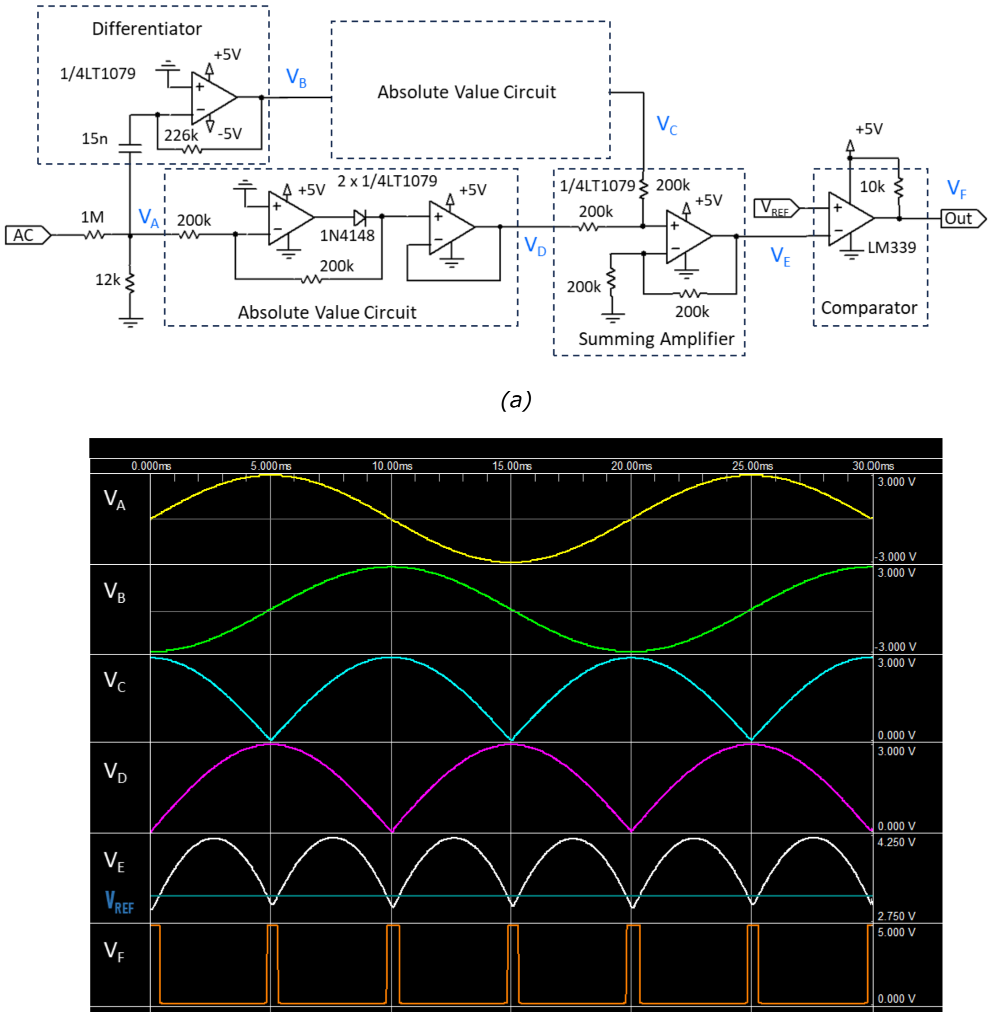
The example of a network realizing the analog portion of such a detection technique, employing general-purpose components—micropower dual or quad op amps LT1078 /LT1079—is given in Fig. 4a; the timing diagrams illustrating its operation are shown in Fig. 4b.

The minimums of the function are achieved at $x = k\pi/2$ and are equal to the sinusoidal signal magnitude V_m (as shown in the Fig. 3 diagram). This means that the reference voltage V_{REF} must be set above that level. Equating $F(x)$ to the reference level yields the detection time as a function of V_{REF}:

$$T_{d.fault.max} = \cos^{-1}\left\{0.5 \cdot \left[\sqrt{2 - (V_{REF}/V_m)^2} + V_{REF}/V_m\right]\right\}/\pi f$$

For example, at $V_{REF}/V_m = 1.1$, f = 47 Hz, the ac fault detection time equals 0.72 ms. This analog circuit arrangement can be used to control a single counter IC, as shown in Fig. 1.

If the direct and differentiator signal paths are separated, a dual counter IC needs to be employed. Since usage of such an ac sag detection technique is associated with a parts count increase and greater complexity, it may be reasonable to consider packing the accelerated sag detection network into an integrated circuit. In practice, to provide a fixed gain, a differentiator circuit can be slightly modified by adding an input resistance and a feedback capacitor.[4]



(a)

(b)

Fig. 4. Ac fault and accelerated sag detection network employing general-purpose components—micropower dual or quad op amps LT1078 /LT1079 (a) and timing diagrams illustrating its operation (b). Signal V_F in this network matches signal V_B in Fig. 2.

Enhancing PSU- And IT System Performance

In the case when the input voltage drops to zero, the inlet energy supply gets interrupted, and the required V_{cc} level at the PSU dc-dc converter input is provided only by the bulk capacitor. To minimize the bulk capacitor voltage dip, the power consumed by the load also needs to be minimized. To make this happen, the PSU load must be equipped with a power management function that is capable of significant momentary power reduction. This process needs to be activated by an external (in our case -Alert) signal.

Since the detector provides about a period of ac line frequency warning of the ac power loss, it can act as an extra Power OK signal with extended power down warning time. The simplest direct use of the ac loss advanced warning is for the prevention of data loss in case of power outages.

This prevention can be achieved if the PSU holdup time can be used, for example, for the writing of data to non-volatile memory. This could prevent data loss after a power outage in devices like a PC or smart TV, in which a sudden power loss disrupts the writing of data to non-volatile memory or causes cache corruption.

In IT systems with fast ac loss detection and a battery backup (BBU) module, the PSU holdup time requirement can be drastically reduced, and the BBU module can be activated within a fraction of a millisecond after ac fault detection, which allows for significant PSU efficiency increase.[1] Such an increase can be derived from the increase of a minimum dc-dc converter supply voltage:

$$V_{c.min}/V_{c0} = \sqrt{1 - 2t_{HUT(BBU)}P_o/(Eff \cdot V_{c0}^2 \cdot C)}$$

where $t_{HUT(BBU)}$ is the required holdup time, which in the BBU case does not exceed 1 ms, V_{c0} is the nominal supply voltage equal to the initial cap voltage, P_o is the output power, which in this case can be assumed equal to maximum, Eff is the dc-dc stage efficiency, and C is the bulk cap value.

In terms of availability, activating the BBU module by the Alert signal makes such a power delivery arrangement equivalent to the online double-conversion UPS, which provides continuous, high-quality, and conditioned power with zero transfer time to batteries, ideal for sensitive IT equipment.

In IT installations containing minor, non-critical peripheral equipment and operating with more efficient standby (offline) UPSs, PSUs must have a holdup time (t_{HUT}) varying from one-half to a full ac cycle. In such IT systems, the ac fault signal can be utilized to control the PSU load. This approach can be used to achieve a smart, enhanced ride-through during an ac fault condition. In that case, the minimum supply voltage can be increased because the energy that needs to be delivered to the load is lower than in the conventional case.

The waveforms illustrating the processes in the PSU supplying power to the IT system are shown in Fig. 5 for a one-cycle dropout case. The consumed power reduction process is defined by an IT system architect and can start, for example, with instantaneous cooling fan power interruption (t_1), followed by CPU and memory throttling (t_2), reducing CPU speed (clock frequency), and restricting data transfer rates. This sequence is illustrated by the output power timing diagram in Fig. 5 (blue trace).

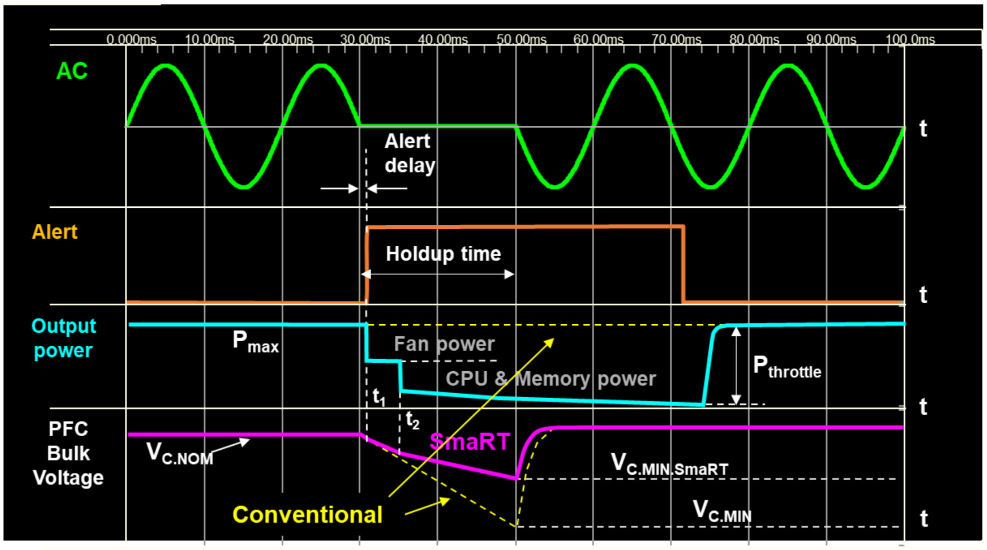


Fig. 5. The increase of a minimum dc-dc converter supply voltage with smart ride-through. When the consumed power drop process starts (t_1), the capacitor discharge slows down, and the cap voltage reduces at a lower rate (pink trace) than in the conventional case, resulting in a higher minimum supply voltage.

From a PSU module perspective, when the consumed power drop process starts (t_1 in Fig. 5) the capacitor discharge slows down, and the cap voltage reduces at a lower rate. The discharge rate additionally drops at the moment t_2 and continues dropping as long as the Alert signal stays asserted, and there is room for further power reduction (throttling). This makes the resultant dc-dc converter supply voltage at the end of the t_{HUT} interval higher (the PFC bulk voltage diagram in Fig. 5—pink trace) than in the conventional case characterized by a fixed output power level (yellow dashed lines). The exact minimum operating supply voltage for the SmaRT technique can be calculated by using the equation:

$$V_{c.min.SmaRT} = \sqrt{V_{c0}^2 - 2P_{o.avg}t_{HUT}/(Eff \cdot C)}$$

where $P_{o.avg}$ is an average consumed power over the HUT interval:

$$P_{o.avg} = \frac{1}{t_{HUT}} \int_0^{t_{HUT}} P_o(t)dt$$

The more throttling can be applied, the more power reduction the Alert signal can create, and the lower the average power within the HUT interval. This allows PSU customers to relax the HUT requirements in the power supply spec by lowering the HUT cert power level and warrants higher $V_{C.MIN}$ and PSU efficiency.

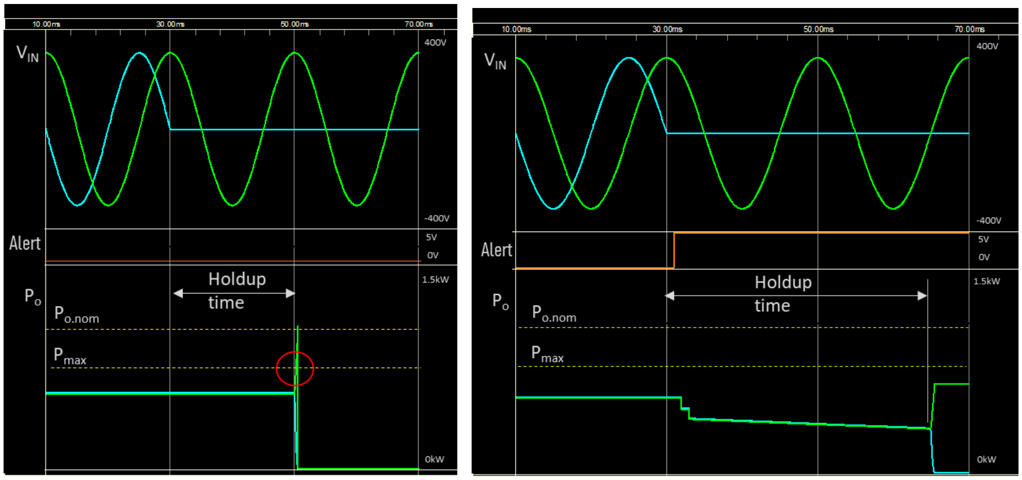
As an alternative to the $V_{C.MIN}$ and PSU efficiency increase, the reduced $P_{o.avg}$ level (at fixed t_{HUT} and $V_{C.MIN}$) allows for the bulk cap size reduction:

$$C_{SmaRT} = \frac{P_{o.avg}t_{HUT}}{Eff(V_{c0}^2 - V_{c.min}^2)}$$

This option opens an opportunity for PSU size and cost reduction.

Another potential benefit of activation of the power management function by the Alert signal could be the increase in the reliability of the IT system receiving power from two ac feeds and operating in a so-called 2+0 PSU configuration. Such a PSU configuration in servers means two power supply modules are installed and active simultaneously, with both sharing the electrical load to maximize power capacity rather than providing module redundancy.

Besides lower cost achieved via usage of a lower power-rated PSU as compared to a 1+1 config, a potential benefit that such a power arrangement provides is supporting the ac redundancy. In a conventional 2+0 arrangement, if one ac feed fails, for example, due to a tripped circuit breaker, the system will shut down after the HUT interval because the remaining unit cannot support the full load. This process is illustrated in Fig. 6a.



(a) *(b)*

Fig. 6. PSU modules' behavior in a 2+0 system configuration. In the conventional case, when one ac feed fails, the power subsystem will shut down after the HUT interval because the remaining unit cannot support the full load (a). In the smart ride through case, the IT system gets the signal to control the consumed power and extended HUT for power reduction, which can keep it active (b).

In a SmaRT case, failure of one ac feed triggers the process of power reduction. If over the warning time interval, the consumed power can be sufficiently reduced (Fig. 6b), the IT system remains active and will be able to reach its full performance without operator involvement once the failed feed is activated. To make this happen, the minimum throttle power must meet the following condition:

$$P_{thr} \geq P_{o.nom} - P_{max}$$

where $P_{o.nom}$ is the nominal power consumed by the system before ac fault, P_{max} is the maximum PSU module rating (Fig. 6). The HUT interval in this case after fast throttling takes over, allows for additional power reduction executing a slower, graceful degradation of service (Fig. 6b). Such a power delivery arrangement presents the option of powering of an IT system with cheaper, smaller size and lower-power-rated PSUs. Such a system configuration supports full performance when both ac feeds are active and reduced performance when one ac feed is down.

Summary

The presented analog networks contain general-purpose components that are capable of detecting ac dropouts in sub-millisecond time intervals and ac sags within a quarter-period of line frequency. Establishing a link between the ac fault detector and the IT equipment—allowing for a PSU load reduction when the ac feed status is abnormal—presents significant opportunities to enhance both PSU and system performance.

In IT systems with offline UPS, the smart ride through an ac dropout condition allows for PSU efficiency increase by raising the minimum operating voltage of the dc-dc converter or, alternatively, bulk capacitor size reduction.

In IT systems with fast ac loss detection and BBU module, the PSU holdup time requirement can be drastically reduced and the BBU module can be activated within a fraction of a millisecond. This allows for significant PSU efficiency increase and bulk cap size reduction.

Fast ac fault detection opens an opportunity for increasing the reliability (availability) of the IT systems receiving power from two ac feeds and operating in a 2+0 PSU configuration. If, over the warning time interval, the consumed power can be sufficiently reduced, the IT system will remain active when one of the ac feeds fails. It will then be able to reach its full performance once the power is restored.

Such a power delivery arrangement presents a power delivery architecture option of an IT system with cheaper, smaller-sized, and lower-power-rated PSUs. Such a system configuration supports full performance when both ac feeds are active and reduced performance when one ac feed is down.

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About The Author

Viktor Vogman is currently retired from Power Conversion Consulting where he applied his skills as an analog design engineer specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

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