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Rad-Hard SiC MOSFETs Pave The Way For Megawatt-Scale Space Applications

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NASA mission architectures from Artemis to crewed Mars transit are driving spacecraft electrical power requirements from tens of kilowatts toward the megawatt class. At those power levels, mass-efficient power management and distribution demands bus voltages well above what current high-power spacecraft bus architectures, typically capped at 270 V, can support. Unfortunately, no space-qualified semiconductor can switch reliably at the voltages those missions require.

Silicon carbide (SiC) MOSFETs offer the breakdown voltage, on-resistance, and thermal conductivity to fill that gap. However, commercial SiC devices are acutely vulnerable to heavy-ion single-event burnout (SEB) and single-event gate rupture (SEGR), limiting practical space derating to roughly 250 V. To overcome these limitations, CoolCAD Electronics is developing radiation-hardened SiC MOSFETs that combine hardening-by-design layout techniques with process-level modifications, validated at Texas A&M University Cyclotron Institute and Brookhaven National Laboratory.

Test results for the new SiC devices demonstrate SEB thresholds above 900 V under linear energy transfer (LET) conditions exceeding 40 MeV·cm²/mg and total ionizing dose (TID) tolerance above 300 krad(SiO_2). Such performance enables derated operating voltages above 300 V, opening the path to compact high-power electric propulsion systems that silicon and gallium nitride cannot address.

This article begins by reviewing projected power requirements for some pending NASA missions and discusses their implications for power rail voltages in spacecraft electrical systems. It also highlights the reliability concerns that motivate use of SiC power switches. Some background is then provided on the different classes of radiation that semiconductors are subjected to in space and tested against. The vulnerabilities of SiC power devices to SEB and SEGR are noted, as are the advantages of SiC for total dose radiation.

A comparison of commercially available silicon MOSFETs, GaN HEMTs and SiC MOSFETs, highlights the tradeoffs of the different power semiconductors with respect to flight heritage, radiation hardness, and voltage ratings, helping to explain further why SiC is promising for space. This section also notes the vulnerabilities CoolCAD seeks to overcome.

The article then explains the principles the company is applying to make SiC MOSFETs rad hard by design and by process. The test methods and setups used to verify TID and SEE performance of CoolCAD's SiC MOSFETs are then described. Finally, the test results obtained for CoolCAD's devices are presented, and their implications for device usage are discussed.

The Power Ambition Of Modern Space Missions

NASA's near-term missions are already pushing power levels that dwarf anything previously launched. The Gateway Power and Propulsion Element, slated for launch as early as 2027, carries a 60-kW solar electric propulsion system. Mars architecture studies call for transfer vehicles in the 400-kW to 2-MW range, a figure NASA Glenn researchers describe as the practical floor for crewed interplanetary transit on a tolerable timeline. These are not aspirational numbers; they follow directly from orbital mechanics, mission duration, and life-support mass budgets.

The implication for power electronics engineers is direct: the switching transistors at the heart of every power management and distribution (PMAD) converter must handle higher voltages, higher currents, and more accumulated radiation dose than any space-qualified part available today. Every aspect of PMAD design flows from the capabilities and limitations of the power semiconductor at its core.

Why High Voltage Is The Only Practical Path

When mass is the engineering constraint, voltage is the designer's primary lever. At constant power, doubling the bus voltage halves the current and reduces resistive losses. More importantly, it reduces the conductor cross-section required to carry that current.

For a fixed resistive loss fraction, copper conductor mass scales roughly with the square of current at fixed power. For a 400-kW propulsion system, the difference between a 270-V bus and a 1,000-V bus translates to

hundreds of kilograms of harness mass, a figure that is far from negligible when every kilogram of payload imposes launch cost in the tens of thousands of dollars.

The same voltage-scaling argument applies to Hall-effect thrusters, the workhorse of solar electric propulsion. High-power Hall thrusters operate at individual discharge voltages of 300 V to 800 V, and the PMAD converter driving them must switch efficiently at those voltages. The current workaround is stacking multiple lower-voltage silicon MOSFETs in series to reach the required voltage rail.

That approach introduces gate-drive synchronization complexity that degrades system reliability. Fewer devices with inherently higher blocking voltage is always the better engineering solution, and SiC is the material that makes it achievable.

The Radiation Challenge For Power Semiconductors

Space radiation arrives in three principal forms. Total ionizing dose (TID) accumulates from chronic exposure to gamma rays, X-rays, and protons, damaging oxide charge trapping sites and shifting device thresholds over a mission lifetime (Fig. 1). Displacement damage dose (DDD) results from protons and heavy ions displacing lattice atoms, degrading minority carrier lifetimes and bulk mobility.

Then there are single-event effects (SEEs) which arise from individual high-energy heavy ions traversing the device in microseconds. Of the three, SEEs present the most operationally dangerous threat to high-voltage power MOSFETs, because a single ion strike can destroy a device that has accumulated no measurable TID degradation.

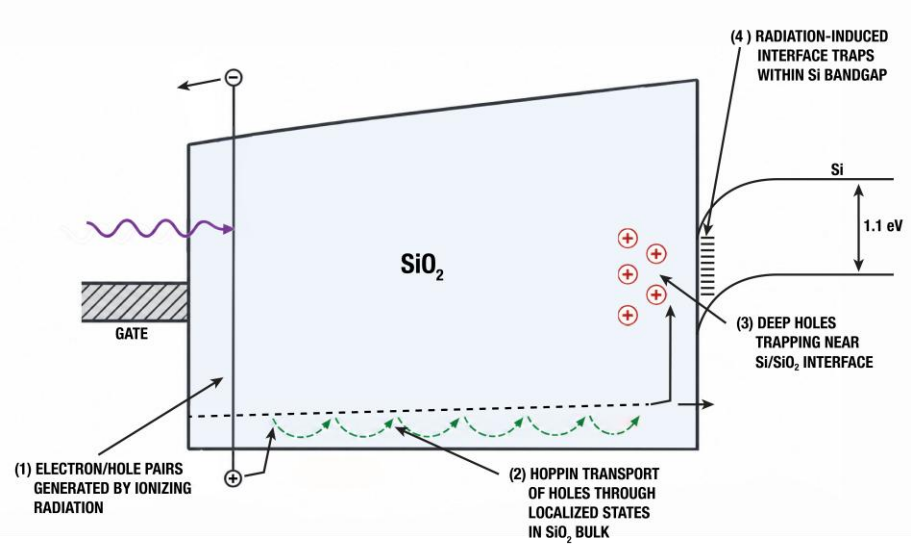


Fig. 1. Cross-section of the SiO_2/SiC gate stack showing the four primary TID mechanisms: (1) electron-hole pair generation by ionizing radiation, (2) hopping transport of holes through localized states in SiO_2, (3) deep hole trapping near the Si/SiO_2 interface, and (4) radiation-induced interface trap generation within the Si bandgap. Positive oxide charge and increased interface state density shift threshold voltage and degrade on-resistance over accumulated dose (see the reference).

When a heavy ion passes through the depleted drift region of an off-state MOSFET, it deposits a dense column of electron-hole pairs, a plasma tube, along its track. The electric field across the drift region immediately sweeps the plasma, generating a transient current pulse. If the device is biased above the SEB threshold voltage, this transient triggers regenerative impact ionization in the parasitic bipolar structure inherent to the MOSFET.

The resulting thermal runaway produces localized temperatures that can exceed the SiC melting point in microseconds, burning a conductive filament through the device. This is single-event burnout, and it is the dominant failure mechanism for SiC power MOSFETs in the space environment.

Single-event gate rupture (SEGR) is a related and equally dangerous failure mode. The intense electric field generated by the ion-induced plasma in the drift region couples capacitively through the gate oxide, producing

a field spike that can rupture the SiO_2 dielectric. SEGR damage is often latent: the gate oxide is weakened without immediately shorting, making it particularly insidious for long-duration missions where cumulative heavy-ion fluence builds up over years.

Total Ionizing Dose: Where SiC Starts With An Advantage

SiC's 3.26-eV bandgap and higher atomic displacement threshold give the bulk semiconductor substantially more inherent TID and displacement damage tolerance than silicon. Electron-hole pairs generated by ionizing radiation in SiC and in SiO_2 grown on SiC have a lower probability of hole trapping, contributing to low net oxide-trapped charge, and the larger bandgap reduces the magnitude of threshold voltage shifts at equivalent dose. Bulk SiC material tolerates well above 1 Mrad(Si) without measurable carrier mobility degradation.

The gate oxide complicates this picture. SiC MOSFETs use SiO_2 gate dielectrics that accumulate interface traps and oxide-trapped charge under TID exposure just as silicon MOS devices do. Commercial SiC MOSFETs from major manufacturers typically exhibit threshold voltage shifts and on-resistance increases of 10% to 20% at doses of 100 krad(Si) to 300 krad(Si).

Properly engineered gate oxides with nitridation and controlled interface chemistry can push TID tolerance above 300 krad(SiO_2). SiC junction field-effect transistors (JFETs), which eliminate the gate oxide entirely, achieve inherent TID tolerance above 300 krad(Si), at the cost of normally-on behavior that complicates converter design.

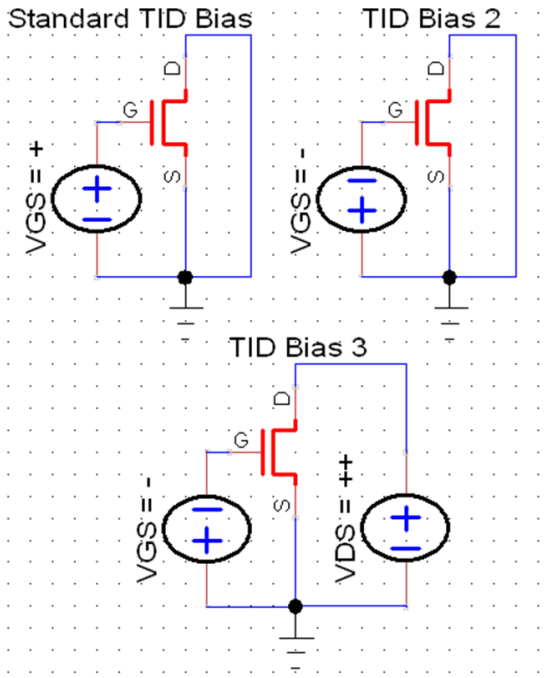


Fig. 2. The three test circuit configurations used for Co-60 gamma TID characterization. Standard TID bias stresses the gate oxide under positive gate bias to accelerate hole trapping. TID bias 2 applies a reversed gate polarity to characterize the relative contributions of interface trap generation versus oxide-trapped charge to the observed threshold voltage shift. TID bias 3 adds a simultaneous high-voltage drain bias to stress the gate oxide under conditions representative of off-state blocking during irradiation.

Silicon, Gallium Nitride, And Silicon Carbide: A Practical Comparison

Three semiconductor families are competing for the high-power space PMAD application: silicon, GaN, and SiC. Each occupies a distinct trade space, and none currently satisfies all requirements simultaneously.

Silicon remains the TRL-9 baseline. Radiation-hardened silicon MOSFETs and IGBTs carry decades of spaceflight heritage and MIL-PRF-19500 qualification infrastructure. The problem is voltage. The most capable space-qualified silicon MOSFET commercially available is rated at 200 V with 45-mΩ on-resistance at 29 A. That ceiling limits silicon-based PMAD systems to approximately 10 kW on a conventional bus architecture.

Stacking silicon devices to reach 600-V or 1,000-V equivalent rails adds synchronization complexity, reduces mean time between failures, and consumes significant board area and mass. Silicon's fundamental critical field of roughly 0.25 MV/cm versus SiC's 2.5 MV/cm means no process improvement will close the voltage gap.

GaN lateral high-electron-mobility transistors offer a compelling radiation profile. Because lateral GaN HEMTs lack both a gate oxide and the parasitic bipolar junctions present in vertical MOSFET structures, they are inherently immune to both SEGR and SEB. Flight heritage data indicates GaN HEMTs surviving above 1 Mrad(Si) TID with minimal parametric shift. The fundamental limitation is voltage.

Commercial radiation-tolerant GaN HEMTs are available to 650 V, with experimental devices slightly above that. For a 1,000-V PMAD bus, a 650-V rated part derated 50% for critical missions yields only 325 V of usable headroom, barely adequate for Gateway-class missions and wholly inadequate for multi-hundred-kilowatt Mars transit architectures. GaN's thermal conductivity of 1.3 W/(cm·K) to 1.7 W/(cm·K) on silicon substrates also limits power density at the kilowatt scale.

SiC occupies the voltage space neither silicon nor GaN can reach. SiC MOSFETs are commercially available at blocking voltages from 650 V to 3,300 V, with experimental devices demonstrated above 10 kV for terrestrial use.

The Baliga figure of merit, which captures the on-resistance versus blocking voltage tradeoff, favors SiC by a factor of 200 to 300 over silicon at equivalent voltage ratings, meaning equivalent on-resistance at ten times the blocking voltage. SiC's thermal conductivity of 3.7 W/(cm·K) to 4.9 W/(cm·K) is three times that of silicon and more than twice that of GaN on silicon substrates, allowing higher power dissipation per unit die area under the tight mass and volume constraints of space converters.

The disadvantage relative to GaN is the gate oxide and the vertical design with a larger active volume, which reintroduces susceptibility to SEB and SEGR. Engineering that vulnerability out of SiC without sacrificing the electrical performance that makes the material attractive is the core problem CoolCAD Electronics is solving.

Hardening SiC MOSFETs By Design And Process

Radiation hardening of SiC MOSFETs requires simultaneous optimization at the layout, circuit, and process levels—what the radiation-effects community calls hardening by design (HBD) and hardening by process (HBP). The trade space is real: modifications that suppress SEB and SEGR typically increase on-resistance, shift threshold voltage, or reduce switching speed. Finding the Pareto-optimal point that maximizes radiation tolerance without unacceptable electrical performance penalty requires tightly coupled TCAD simulation, device fabrication, and radiation characterization in an iterative loop.

At the layout level, cell geometry controls the electric field profile in the drift region during a heavy-ion strike. Source-to-body contact spacing, cell pitch, trench depth and sidewall angle, and p-shield implant depth all influence how the peak field distributes during an ion event. Layouts that spread the peak field away from the gate oxide and body-drain junction reduce the probability of initiating the regenerative bipolar or other thermal mechanisms that lead to burnout.

At the process level, p-body doping concentration and profile, SiO_2-SiC interface passivation chemistry, and drain extension doping interact to set the SEB threshold. CoolCAD uses its proprietary CoolSPICE simulation platform to explore this multi-dimensional design space computationally before committing wafers, reducing development cycle time and enabling systematic optimization.

Fabrication is conducted through commercial SiC foundry arrangements that allow design-rule modifications unavailable in standard commercial SiC power device process flows. This small-lot, design-flexible approach is well suited to the low and medium production volumes NASA programs require, a practical consideration for program affordability on missions where custom parts are essential but high-volume manufacturing economics do not apply.

Co-60 TID Test Infrastructure And Results

TID testing was performed using a Co-60 gamma source at a dose rate of approximately 2 rad(Si)/s, which is within the range specified by MIL-STD-883 for dose-rate-sensitive oxide characterization (Fig. 3). Devices were biased under representative operating conditions during irradiation, with gate and drain currents monitored continuously at each accumulated dose step.

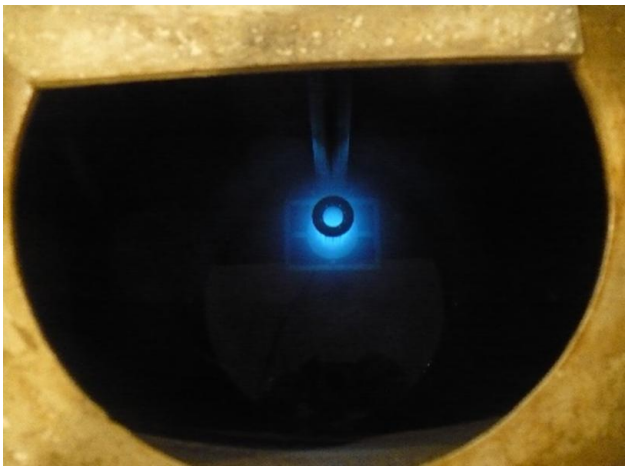


Fig. 3. Co-60 gamma irradiation source used for TID characterization. The Cherenkov radiation (blue glow) is visible around the cobalt rods, which are stored submerged in a water pool and elevated to a fixed irradiation height during testing. The approximately 2-rad/s dose rate used in these experiments is consistent with standard TID qualification protocols. CoolCAD operates this facility to measure bulk trap densities and threshold voltage shifts across accumulated dose levels.

The Co-60 test campaign's primary metric, threshold voltage shift as a function of accumulated dose, is plotted in Fig. 4. CoolCAD's radiation-hardened SiC MOSFETs hold ΔV_TH to approximately 0.35 V at 120 krad(Si), a modest negative shift that compares favorably with the 0.5-V to 1.0-V shifts typical of commercial SiC devices at equivalent dose. That improvement traces to the hardened gate oxide, where controlled interface chemistry and dielectric engineering reduce the oxide-trapped charge and interface states that would otherwise drive V_{TH} negative as holes accumulate near the SiO_2-SiC interface under bias.

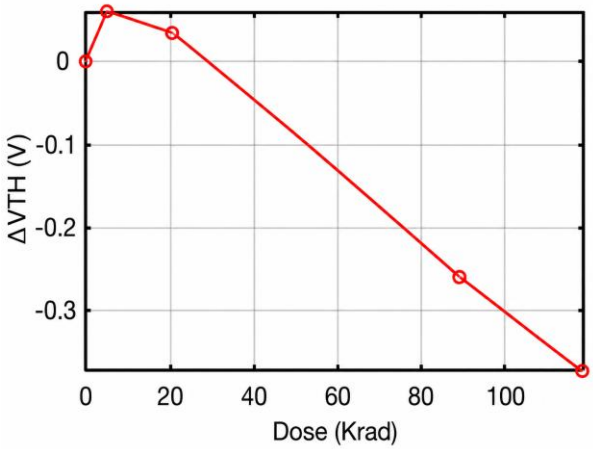


Fig. 4. Threshold voltage shift (ΔV_TH) as a function of accumulated TID dose at V_{GS} = 20-V gate bias. CoolCAD's new-generation radiation-hardened SiC MOSFETs show a modest negative threshold voltage shift of approximately 0.35 V at 120 krad(Si), significantly lower than commercial SiC devices, which typically exhibit 0.5-V to 1.0-V shifts at equivalent dose. The controlled oxide interface chemistry and gate dielectric engineering are the primary contributors to this improved performance.

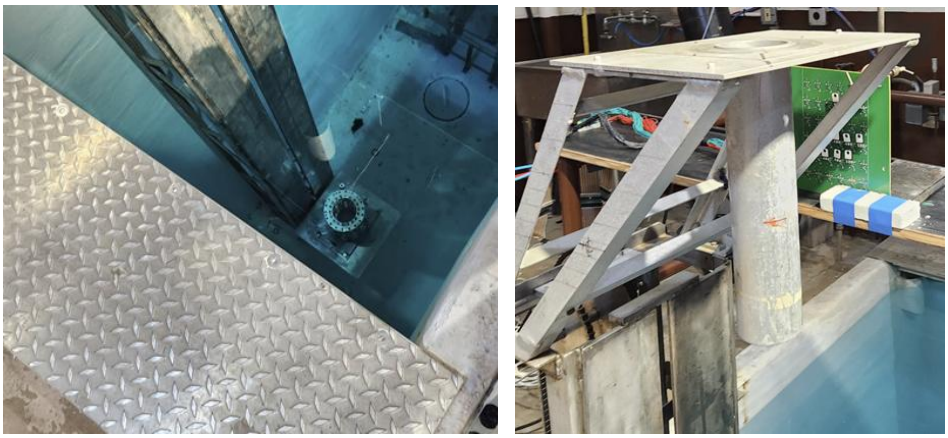
Gate and drain leakage current were monitored continuously during each run including the final ~40-krad increment of the dose run to confirm that oxide charging does not compromise off-state blocking, with the setup shown in Fig. 5. Gate leakage under V_{GS} = 20 V and V_{DS} = 0 V held at stable nanoampere levels throughout that final dose increment, with the measurement noise attributed to test cabling rather than device behavior.

Drain leakage under V_{GS} = 0 V and V_{DS} = 1,100 V likewise showed stable off-state blocking over the same interval. Together, these results indicate that the threshold voltage improvement in Fig. 4 is not achieved at the

expense of oxide integrity or high-voltage blocking capability, both of which matter as much as V_{TH} stability for a converter-qualified part.

That in-situ monitoring was performed using the fixture shown in Fig. 5. An elevator platform and grating (5a) lower the device board to a fixed height above the Co-60 pool for each irradiation run. This is a repeatable geometry that holds dose rate constant across the campaign and lets devices be retrieved and rebiased between measurements without disturbing that alignment.

The multi-device test board and its bias and monitoring circuitry (5b) remain mounted at the pool edge throughout the run. They apply the gate and drain conditions needed to hold devices in a representative operating state while logging leakage current at each accumulated dose step.



(a) (b)

Fig. 5. CoolCAD's device-under-test fixture positioned at the Co-60 pool for TID irradiation runs. The elevator platform and grating (a) used to lower devices to the source at a fixed irradiation height. The multi-device test board and bias/monitoring circuitry mounted at the pool edge (b) for continuous in-situ gate and drain current monitoring throughout each dose step.

Heavy-Ion Test Infrastructure And Methodology

Before heavy-ion testing can begin, CoolCAD has to determine which ion species and beam energies will stress the device the way a worst-case galactic cosmic ray strike actually would. That depends on where each candidate ion deposits its peak linear energy transfer (LET) as it slows down passing through the device stack, since a strike that peaks above or below the active drift region will not exercise the burnout and gate-rupture mechanisms the hardening effort is meant to address.

Fig. 6 plots the calculated LET versus depth for the ion species under consideration, tracing their range through CoolCAD's SiC device stack from the overlayers down through the epilayers and into the substrate. Species and energies are selected so peak LET falls within the active drift region, typically 5 to 30 µm deep. This range replicates the worst-case strike geometry a galactic cosmic ray would present in orbit. This calculation, rather than the nominal beam energy alone, guides selection of the ions used in the heavy-ion test campaign described in this article.

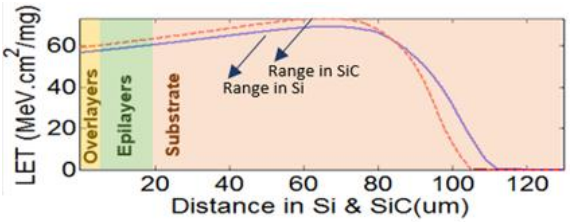
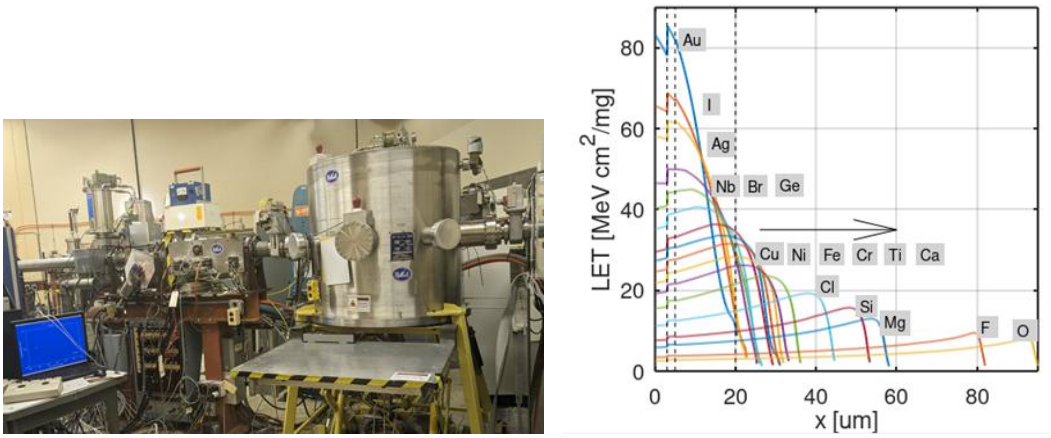


Fig. 6. Calculated LET vs. depth profile in SiC showing ion range through the device stack: overlayers, epilayers, and substrate. Ion species and energies are selected to deliver peak LET within the active drift region, typically 5 to 30 µm deep, replicating galactic cosmic-ray worst-case strike geometry.

Heavy-ion testing was performed at the Brookhaven National Laboratory (BNL) Tandem Van de Graaff facility using chlorine ions at approximately 18 MeV·cm²/mg LET in SiC and calcium ions at approximately 25 MeV·cm²/mg. Additional measurements were performed at Texas A&M University Cyclotron Institute (TAMU CI) using neon, argon, silver, and xenon beams to characterize the LET dependence of SEB threshold across the range relevant to the galactic cosmic ray spectrum (Figs. 7 and 8).



(a) (b)

Fig. 7. Texas A&M University Cyclotron Institute beam line end station used for high-LET heavy-ion irradiation (a). The facility delivers ion beams from neon through xenon, providing LET coverage from approximately 3 MeV·cm²/mg to above 60 MeV·cm²/mg in SiC. Calculated LET vs. depth profiles (b) for the available suite of ions. Ion species and energies were selected to deliver peak LET within the active SiC drift region, targeting depths of 5 to 30 µm corresponding to the epilayer thickness of the devices under test.

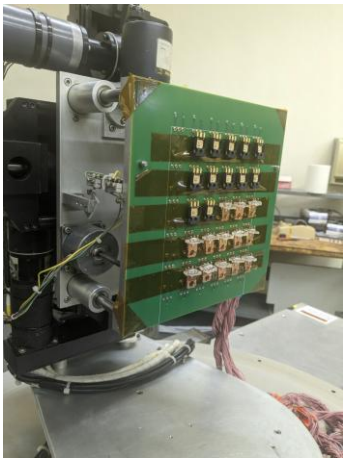


Fig. 8. Multi-device test board loaded with CoolCAD SiC MOSFET die-under-test (DUT) mounted at the beam line end station at BNL. Multiple devices are irradiated per run under active bias, with each device independently monitored for drain current transients indicative of SEB onset. The modular board design allows rapid device swaps between runs and supports in-situ parametric measurements without removing the board from the beam line vacuum interface.

Test Results And Demonstrated Performance

CoolCAD's radiation-hardened SiC MOSFETs demonstrate SEB thresholds above 900 V at LET values exceeding 40 MeV·cm²/mg. This represents a greater than 40% improvement in hardness relative to equivalent commercial SiC MOSFETs, which typically exhibit SEB onset below 600 V under the same ion conditions. Applying NASA's standard 50% derating criterion for critical missions, a device with a 900-V SEB threshold yields a derated operating voltage above 450 V.

For non-critical missions where 25% derating is acceptable, the same device supports operating voltages above 675 V. This compares directly against the approximately 250-V practical ceiling for commercial SiC and the 200-V ceiling for space-qualified silicon.

TID characterization using cobalt-60 gamma irradiation shows less than 0.4-V threshold voltage shift at 100 krad(Si) and parametric compliance through 300 krad(SiO_2), meeting the dose requirements of most GEO and lunar orbit mission profiles. Displacement damage characterization at proton fluences above 10^{12} p/cm² shows no measurable on-resistance degradation, consistent with SiC's inherently high atomic displacement threshold.

Wafer-level yield across the hardened process runs has been above 95%, with device-to-device variation in threshold voltage, $R_{DS(ON)}$, and BV_{DSS} within 1% of median. This uniformity indicates the hardening process modifications are well controlled and do not introduce the parametric outliers that would compromise circuit design margin in a converter application.

Conclusion

The transition from kilowatt-class to megawatt-class spacecraft power is not a distant aspiration; it is the near-term engineering requirement of NASA missions already in development. Silicon cannot deliver the blocking voltage. GaN cannot reach the bus voltages that high-power SEP and NEP architectures require. Commercial SiC cannot survive the heavy-ion radiation environment at the voltages those same architectures demand.

But as test results presented here demonstrate, radiation-hardened SiC MOSFETs that combine layout optimization, process-level hardening, and rigorous characterization at particle accelerator facilities are the only near-term path to space-qualified switching devices capable of operating above 400-V to 600-V derated bus rails. The results demonstrated by CoolCAD Electronics validate that this path is technically feasible, process-controlled, and within reach of a qualification timeline compatible with Gateway follow-on and Mars precursor mission schedules.

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For Further Reading

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About The Author

Akin Akturk is co-founder of CoolCAD Electronics, an ISO 9001-certified company located in Greenbelt, Md., with strong ties to the University of Maryland and a portfolio of NASA, DARPA and Department of Defense programs spanning more than two decades. Akin's research and engineering work spans performance and thermal modeling of nanoscale MOSFETs, planar and three-dimensional integrated circuits, and non-isothermal device behavior from cryogenic temperatures to hundreds of degrees above room temperature. In addition, he is a recipient of the NASA Tech Brief Award for his design of a hybrid AlGaN-SiC photodiode for deep ultraviolet photon detection. Akin holds M.S. and Ph.D. degrees in electrical and computer engineering from the University of Maryland, College Park. For more information, visit the company website.

For more on rad-hard power semiconductors see How2Power's Space Power section.