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Commentary

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Scaling AI Infrastructure: The Critical Role Of ISOP Power Architectures In 800-VDC Ecosystems

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Modern data centers' power requirements are changing dramatically due to the rapid growth of AI workloads. As GPU platforms such as NVIDIA's Vera Rubin push rack power from 200 kW toward the 1-MW level, traditional 48-V busbar power distribution becomes physically and economically impractical because of massive conduction losses. Current can exceed 4,000 A in the 48-V busbar before reaching the server boards.

To address these increasing current levels, the industry is transitioning to an 800-Vdc power distribution architecture. This approach enables high-voltage dc to be delivered directly to server boards, significantly increasing power capacity while reducing copper requirements and improving overall efficiency.

One of the major challenges in the new 800-V ecosystem is the efficient conversion of high-voltage dc to the intermediate bus voltages of 12.5 V or 6 V required by POL voltage regulators powering AI processors, without needing an additional 800-V to 48-V conversion stage. Traditional single-stage topologies with such high step-down ratios result in transformer complexity and limited efficiency.

However, there is an alternative, modular approach to converting 800 V to 12.5 V or 6 V in a single stage: the input-series-output-parallel (ISOP) architecture. Because of its various advantages, ISOP has emerged as the leading architecture for meeting the stringent efficiency, thermal, and power density requirements of next-generation AI factories.

This article describes the structure, operation and benefits of the ISOP architecture, particularly with regard to its implementation using gallium nitride (GaN) power devices in multikilowatt modules. EPC's ISOP converter reference designs and evaluation boards are used to demonstrate the performance capabilities of such converters in designs that produce the desired 12.5-V or 6-V output. ISOP's advantages with regard to simplification of magnetics design and thermal management are highlighted.

What Is An ISOP Converter And How Does It Work?

The ISOP architecture is a modular approach that employs multiple identical isolated dc-dc converter modules, typically based on the LLC resonant topology. In this configuration, the inputs of the modules are connected in series and the outputs in parallel. This setup provides an elegant way to scale both the input voltage and the output current at the same time. For a system with M modules, each module only has a fraction of the total input voltage (V_{IN}/M) and processes a fraction of the total output power (P_{OUT}/M).

A key advantage of using LLC-based modules in an ISOP string is their inherent self-balancing capability. By selecting an appropriate magnetizing-to-resonant inductance ratio (L_m/L_r), the converter gain remains nearly constant at resonance. This provides a robust solution that is insensitive to component tolerances and eliminates the need for complex control algorithms for voltage and current sharing.

Furthermore, the modular architecture enables PWM interleaving among the LLC modules. Interleaving significantly reduces output current ripple; for example, while a single LLC module produces approximately 754-A peak-to-peak ripple, a four-module interleaved ISOP reduces it to just 37 A, greatly reducing the output bus capacitance requirement.

For example, in an 800-Vdc bus system using eight modules such as the EPC91123 reference design, each module handles only a 100-V input. This modular LLC-based approach is inherently self-balancing, allowing the system to operate efficiently without the need for complex control algorithms for voltage and current sharing.

Why ISOP Is Important: The GaN Advantage

Another key advantage of the ISOP architecture is its ability to utilize low-voltage GaN power transistors. In conventional two- or three-level converters operating from an 800-V bus, designers are typically limited to 3.3-kV silicon carbide (SiC) or 650-V GaN devices. In contrast, the ISOP configuration reduces the primary-side voltage stress, enabling the use of 150-V-rated GaN FETs.

The 150-V GaN devices, such as the EPC2305, offer a significantly better figure of merit (FOM) than their higher-voltage counterparts. Their extremely low gate charge (Q_g) and output charge (Q_{oss}) dramatically reduce both conduction and switching losses. As a result, the converter can operate efficiently at switching frequencies around 1 MHz, enabling smaller magnetic components and higher power density.

Detailed comparative studies show that this approach significantly reduces total primary-side switch losses in a 6-kW module:

- Performance gap: An eight-module ISOP implementation using 150-V GaN (EPC2305) achieves a total primary-side switch loss of only 6.8 W. In contrast, a single-module LLC using 1.2-kV SiC devices results in a loss of 15.9 W.
- Footprint optimization: The physical size of the primary-side solution is also dramatically reduced. The GaN-based ISOP implementation requires only 240 mm² of board area, compared to the 630 mm² required for the SiC-based alternative.

How ISOP Improves Magnetics, Thermal Management, And Power Density

Beyond improving power switch efficiency, the ISOP architecture also simplifies the mechanical and magnetic design of the power system. A traditional high-stepdown converter (800 V to 12.5 V) requires a complex transformer turns ratio of 16:1. In contrast, an eight-module ISOP system requires only a 4:1 turns ratio. This simplification enables compact planar transformers to be integrated into multilayer PCBs, reducing leakage inductance and increasing power density.

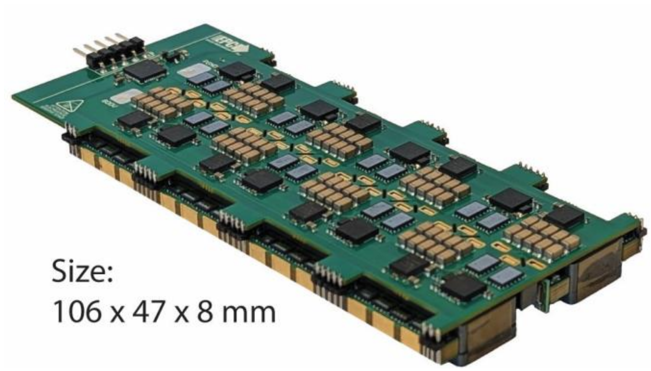
Thermal management is also greatly improved. The ISOP architecture distributes losses across multiple modules over the board area instead of concentrating heat in a single power stage, eliminating thermal hotspots and enabling efficient top-side cooling with liquid-cooled cold plates or high-performance heatsinks. In addition, the modular architecture allows PWM signals to be interleaved.

Interleaving the eight modules significantly reduces output current ripple, relaxing the requirement for bulky output bus capacitors. At the same time it improves overall electromagnetic interference (EMI) performance by reducing high dv/dt voltage transitions.

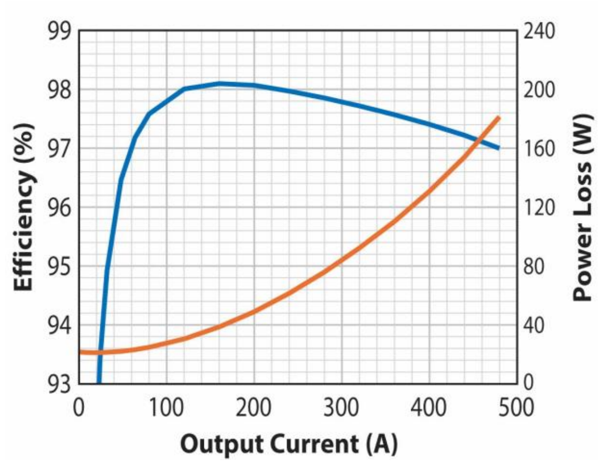
Applications In Modern AI Ecosystems

The primary application of the ISOP converter is as an intermediate bus converter (IBC) on AI server boards. The industry is currently evaluating 6-V and 12-V intermediate bus architectures. A 12-V bus reduces power distribution losses on the server board, while a 6-V bus enables highly efficient single-stage conversion to the sub-1-V core voltages required by AI processors.

This technology has already demonstrated impressive performance. The EPC91123 is an eight-module, 6-kW ISOP 12.5-V converter with an ultra-low profile of just 8 mm and peak efficiency exceeding 98% (Fig. 1).



(a)



(b)

Fig. 1. The EPC91123 evaluation board is a 6-kW, 800-V to 12.5-V ISOP converter. The board is pictured here (a) along with a graph of its efficiency and losses over load (b).

This compact form factor of the EPC91123 is critical for the limited space available on AI server boards, where power delivery must coexist with dense compute hardware and advanced liquid-cooling systems.

The conversion of 800 V to 6 V at the 6-kW power level results in an output current of 1000 A, creating a significant challenge for synchronous rectification (SR). To address this, EPC has introduced the Gen 7 GaN family, including the EPC2370 (18 V) and EPC2378 (25 V) FETs. These devices are optimized for ultra-low conduction and switching losses, with the EPC2370 offering a typical $R_{DS(ON)}$ of just 280 μΩ.

Choosing an 18-V rating for the EPC2370 is critical for 6-V output applications. In a center-tapped transformer secondary, the preferred configuration for minimizing SR losses, the voltage stress across the SR FET is approximately $2 \times V_{OUT}$. At a nominal 6-V output, the SR FET sees about 12.5 V. With a ±10% variation in the 800-V bus voltage, this stress increases to 13.8 V.

A 15-V FET provides insufficient voltage margin, whereas the 18-V EPC2370 satisfies typical derating requirements and offers a 22-V transient rating for additional design margin. A high-density 6-kW, 800-V-to-6-V ISOP module using these devices is designed to achieve 98% peak efficiency and 97% full-load efficiency in a compact 140-mm × 120-mm footprint (Fig. 2).

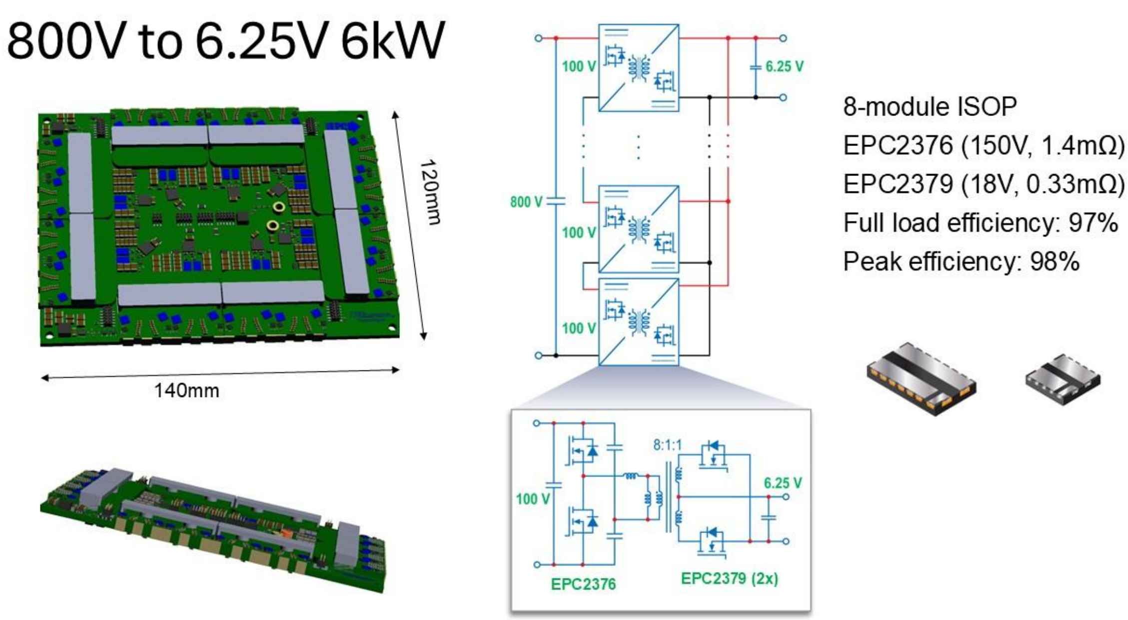


Fig. 2. An 800-V to 6-V demonstration board.

The Future Of ISOP Architectures In 800-V AI Data Centers

The ISOP architecture greatly simplifies the mechanical and magnetic design of the power system. In a conventional, single-stage 800 V-to-12.5 V converter, the transformer turns ratio is 16:1:1; in an eight-module ISOP converter (Fig. 3), it is a much simpler 4:1:1. This enables the use of planar transformers integrated into multilayer PCBs, reducing leakage inductance and increasing power density.

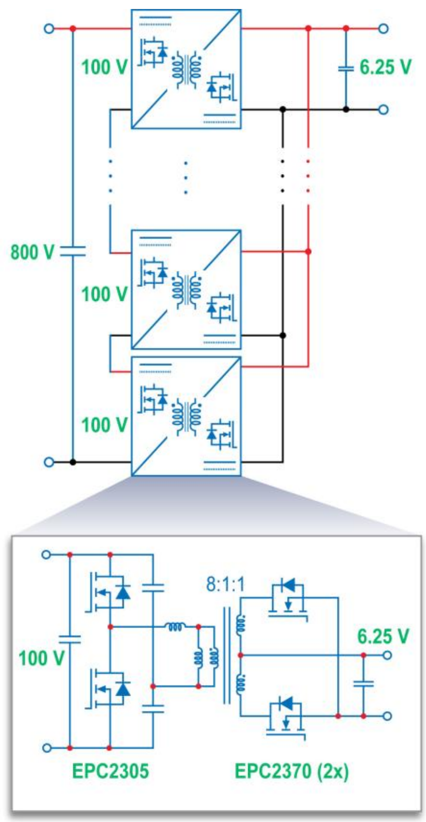


Fig. 3. An eight-module ISOP. This architecture simplifies the design of the transformer, reducing the turns ratio from 16:1:1 as it would be with a traditional, single power converter stage to 4:1:1 in an eight-module ISOP configuration.

Thermal management is also improved by distributing losses across multiple modules, eliminating thermal hotspots. This distributed architecture is especially important for the limited space available on server boards, where power delivery must coexist with aggressive liquid-cooling systems. As AI infrastructure approaches 1 MW per rack, the ISOP architecture based on high-performance GaN FETs is well positioned to support the next generation of high-density power delivery.

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About The Author

Maurizio Di Paolo Emilio is director of Global Marketing Communications at EPC (Efficient Power Conversion), where he manages worldwide initiatives to showcase the company's GaN innovations. He is a prolific technical author of books on GaN, SiC, energy harvesting, and data acquisition and control systems, and has extensive experience as an editor for technical magazines and online publications in power electronics, wide bandgap semiconductors, and embedded systems. Maurizio is a telecommunications engineer and holds a Ph.D. in physics from the University of L'Aquila.

