The Case Of The MOSFET Failure

by Paul L. Schimel, PE

I recently had a fun problem come across my desk. It's a common sequence of events. My customer built a power converter, they used my MOSFETs in the converter. The converter failed, the failure took out the MOSFET.

Having been through a few of these sorts of things, I know the difficulty firsthand, as a customer, as a vendor and as a senior FAE existing between the two, having done the design work firsthand both as a customer and as an FAE.

To get to the root cause, there is a lot of information that needs to be shared on many levels. Do the engineers in the failure analysis (FA) lab understand the commutation of the power converter? Likely not. Do they understand the waveforms? Can they discern a fast dv/dt event coupling into C_{ISS} through C_{RSS} when C_{OSS} charges up quickly to the full blocking voltage? No.

And this is not because they are junior, malfeasant or silly. The hard working engineers in the FA lab are looking at bondwires, polysilicon structures, gate runners, metallization, oxides, bond wire toe and heel stresses. Nowhere in that work is there a discussion of the commutation of the power converter, waveforms, topology or measurement technique.

The customer's sense of urgency can vary between hot and cold on these matters. There is generally urgency about most any failure analysis work (it tends toward hot). The customer has their own tracking and expedite mechanism, the FA lab has their own computer to schedule their work, and the two computer systems don't talk or coordinate.

Moreover, the customer has a product that they wish to sell and a schedule to produce said product and accomplish this. Normally when the FA is requested, the schedule is impacted negatively. This often gives rise to a lot of high level involvement. "We want answers and we want them now" a voice bellows from the corner office, where there is a clear understanding of the time to market expectations and the cost of a schedule slip.

As an engineer, I never really had the luxury of requesting and/or expediting an FA. I never assembled an escalation committee or got my board of directors involved. The pressure was on us engineers to comprehend, measure, re-design and overcome—and we did. But times are different. Kinder, gentler operation has assigned business metrics to every facet, and the components labs are long gone as a matter of cost reduction.

"Just figure it out, dammit!" is no longer hollered by experienced leaders at the 11th hour standing over a sweaty bench. The senior engineers that would help with these complex issues on the bench are gone and there was no succession plan to replace them.

Under these canons, the world looks a lot different today from that bench. Factor in a few 30-minute leadership training seminars that deliver both Narcissus and a hand mirror, and the root cause may not be as forthcoming as it once was. The path of least resistance might well be to just blame somebody else. A component perhaps? The component caused the failure……like the spoon caused the weight gain.

So the customer had a failure, the FA lab gets a hot request with no other information. What comes next? That's easy. In the absence of any other input, the result very likely reads something like this on the first page of the FA report "EOS: Electrical Overstress; The device was subject to too much voltage, too much current, or both". Which is a stunning affirmation that the device is broken. There is no root cause embedded, no lexicography to obfuscate, and no "least untruthful" response.

Again, in defense of the FA lab, they were sent two things. A failed device often resembling a hunk of charcoal and a big dose of urgency. On that event horizon, one would be hard pressed to offer a conclusion of any more depth or gravitas than simply EOS.

But what about the other information? When I looked into this FA case, I requested schematics from the customer. Initially the answer was no. But after some persuasion, and the suggestion that not sharing the information will simply return "EOS" results on the FA report, I did manage to get a schematic. I then requested waveforms, to which I was told that the circuit was only simulated, and it looked good. Again, I had to explain

© 2018 How2Power. All rights reserved. www.How2Power.com

the request, then tell how to minimize loop area in the measurements and capture best possible V_{DS}, V_{GS}, I_D on the rising and falling edges, look for any ringing, look for any abnormal operation, etc.

Prior to my request, the customer hadn't done this. But without this data, how could *anyone* find the root cause of the claimed failure? Could we even be certain that it *worked* and there was a change in behavior that we surmised as a fail?

So the customer captured the waveforms, and they did it right. Nice to see that. Admirable. And this is where I chose to take a different path.

My big giant computer that tracks my progress would rather not have me in the FA lab and I'm certain there's a policy about that. But without my foray into the FA lab we would only have apples talking to oranges underscored by urgency. There is no one in the equation that can map what is happening on the schematic to what is happening on the waveforms to the MOSFET surface to the epitaxial layer. The customer is likely not a device physics expert familiar with the intimate details of the specific MOSFET process. The FA engineer is likely not familiar with the customer's converter or waveforms. There is a clear hole in the equation. A need for a cosmic interposer to interface between the two and "gap fill" in modern softcover management speak.

So I responded. Device physics is not my strongsuit, but I've done my share of device-level design work, integration, test, and much more than my share of bench-level power converter design at most any power level imaginable. I took the schematic and waveforms into the FA lab and sat down next to the top engineer. I cited the computer tracking number on the case. We had the failed device. We took a couple of pictures of the "as received" condition, then decapped, etched, and ground the part.

What we saw was absolutely no sign of reflow in the die attach solder, no voiding, no slow melting effects. This ruled out a linear mode failure where the device had a high V_{DS} and a high I_D for a long time. We were also able to rule out slow V_{GS} transitions and the resultant heating (for example, if the rise and fall times of the gate were 200 ms). This heating would have caused the die attach solder to melt before the top surface source connections had a catastrophic failure. We were seeing the opposite. The die attach solder was untouched (and in this case I had the original X-ray image of the part as shipped as per the various applicable DLA and MIL specifications governing the device and build protocol).

As I was reasoning through this, I saw the FA lab engineer's attitude transition from being bothered by my presence to being grateful. Although it took him a few moments to discern, I hadn't come to rush him and ask "is it done yet" like everyone else. I had come to help.

In the end, what we had left was a topside failure, right under the source bondwire connections to the die. The heel of the connection was still basically intact, the toes ended in a crater that blew through the top layers clear down into the epi. The source wires showed heating, but they were still connected. The FA engineer explained that this is common. The heel often fails last. He correlated it to some wedge bonding machine that I haven't seen, and he spoke of it with a feel and experience level that made me a believer. The man has been working in the FA lab as long as I've been working on the bench.

And I continued reasoning. The waveforms showed very fast commutation on the working device in operation. This particular MOSFET family has higher Rg' than other families. The gate artwork looked fine. There was no catastrophic burning at the gate terminations, the metal, or the gate runners. So this was likely not a gate overvoltage event. The waveforms showed a nice V_{GS} with fast risetime and little to no ringing or overshoot. There were no objective indicia of V_{GS} stress either in the circuit or on the die.

But the fast commutation…….was it then possible that the fast charging of the C_{OSS} of the MOSFET at the turn-off coupled through C_{RSS} into the gate structure? There is a logical path for this, and with fast enough dV/dt on C_{OSS}, it is possible to couple charge through C_{RSS} into the gate (see Fig. 1). This is why most MOSFETs specify a V_{DS} dv/dt speed limit in the datasheet. And R_G' is slightly higher, so even with a good driver and lowest dynamic and static offstate impedance at the gate source terminals, there is some series resistance in the circuit. While the gate connection to the driver may show no nuisance turn-on, the R_G' may allow this on the internal gates.

Is that possible? Yes. And if it did occur, I'd expect to see the MOSFET turning back on briefly during the fast commutation. There would be a fast glitch drop in V_{DS} while it was supposed to be climbing to the rail voltage. That would cause a lot of dissipation in a short time. Very high current. A switchthrough event.

© 2018 How2Power. All rights reserved. www.How2Power.com

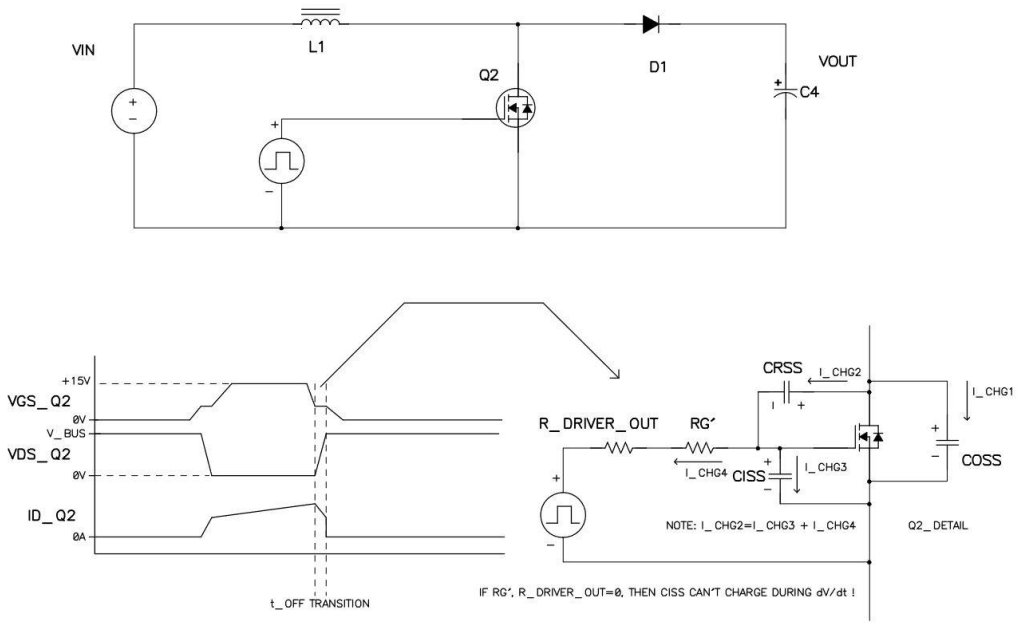

Fig. 1. The Cdv/dt turn-on path that causes false turn-on in a MOSFET.

The waveforms for the new MOSFET that was installed in the failed converter don't show this at all. But does that mean that it wasn't there ever? Maybe the new MOSFET (from which the requested waveforms were gathered) had a higher V_{TH} than the failed device, maybe the test circuit was running at room temp while the failure occurred at high temp (where V_{TH} is lower and the device is more susceptible).

The other possibility is that the source metallization of the MOSFET had a higher resistance. Recall, the source metallization is the stuff that shorts the BE junction of the intrinsic NPN in most any cross section. While we assume that this is zero, what if it were a nonzero resistance? By the same coupling mechanism, the fast commutation could couple charge into the base of this intrinsic NPN through C_{RSS}. If the metallization resistance were high, this could cause the BE junction to turn on (see Fig. 2).

At this point the gate command would mean absolutely nothing. The MOSFET would turn on uncontrollably at this instant. This too could cause the fast heating and topside damage. Modern MOSFET designs guard against this heavily. There is purposed metal over both the N and P well to short this BE junction as source terminal of the device.

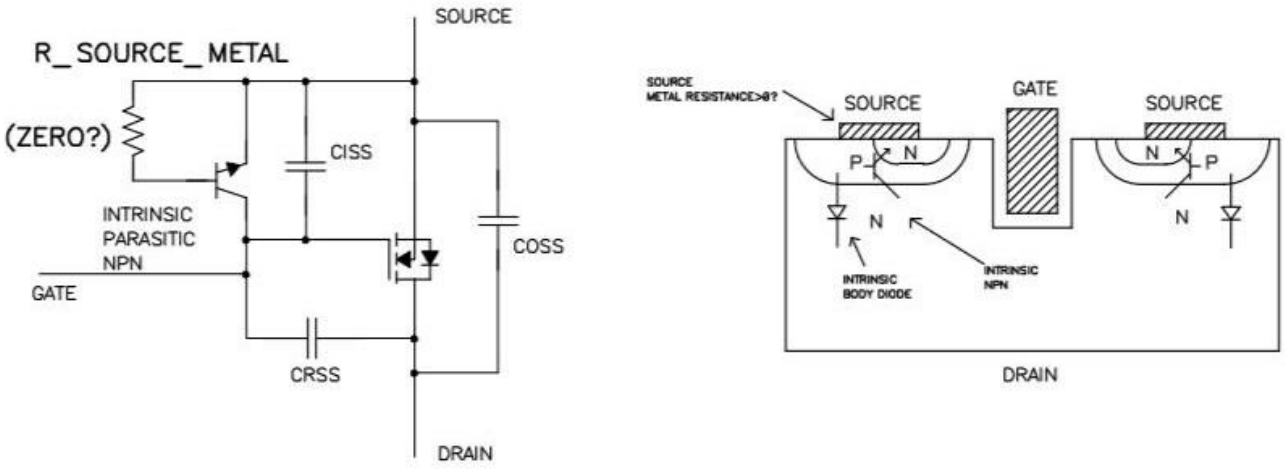

Fig. 2. A parasitic NPN device in a MOSFET, BE shorting resistance and turn-on path.

© 2018 How2Power. All rights reserved. www.How2Power.com

It is also possible that the circuit saw a condition for which it was not protected by design. This particular converter had no means of output current sense. If the output were shorted, the only means of detection would be measuring the inductor saturating. (The inductor had a powdered iron core with perm around 150; therefore V/L would rise to as much as 150x the original di/dt on saturation.) In this circuit, the MOSFET would have to turn on into the saturated inductor, with several hundred nanoseconds of interrupt time, capture the event and begin a turn-off sequence. In that time, the current would skyrocket to well beyond design parameters.

I reasoned through these possibilities to see the FA engineer's utter delight. Delight in that I actually cared enough to sit down and map die-level pictures of possible circuit problems, failures and root causes. I captured my reasoning in a preliminary report and responded to the customer's urgency. We did ultimately find out that there had been a couple of errors in connecting the circuit that placed momentary reverse polarity across the input.

Without this effort, this FA report also would have read "EOS" and little more. And that's not the FA lab's fault. First off, they weren't given any information other than a blown device. Secondly, the engineers in the FA lab really don't know how the circuit, application, controller, input and output works on the customer's bench. I'm glad to have helped with the problem and hopefully my big giant computer keeper will wax bitwise simpatico with my verboten effort of helping the customer in a post-sales support matter. Or perhaps there's a drone strike scheduled in some dark corner of the data matrix and some anonymous shock therapy involved once the system gains true omnipotence. The telltale precursor to this will be, of course, more assigned training in "the system".

I have to say that it was truly rewarding to take a detailed look and some investigative actions into the failed device. It was just plain cool to correlate stuff that happened at angstrom levels to stuff that can be seen on an oscilloscope. I can't imagine too many device physicists or subject matter experts get the chance to make these connections. And that's too bad. I'd like to see the FA team augmented to include actual applications and system understanding. I have also seen instances where the failure was in fact caused by a device problem. But the tendency to leap to that conclusion is modern baggage in a system that doesn't look beyond itself, one where Narcissus would have a private reflecting pond.

About The Author

Paul Schimel is a lifelong innovator with an untiring commitment to engineering excellence in both the practical and theoretical aspects of power electronics and related mixed-signal, mixed-mode and mixed-domain design and control work. He is a licensed PE bringing over two decades of formal experience to his customer base and internal resources. He is familiar with most DOD, MIL, UL, NFPA70, DOD and IEC standards and how they are tested and passed.

Schimel attended the School of Electrical Engineering at the University of Illinois at Urbana Champaign, where he earned a BSEE degree while specializing in power electronics. After this, he spent eight years in successful design engineering roles in consumer equipment including power supply design for projection and direct view televisions and telecommunications equipment including ring generators, battery rectifiers/eliminators, dc-dc converters, and UPSs—both switch-mode and ferroresonant.

Schimel then moved on to applications engineering where he has spent the last 15 years on power management support and design work. He has assisted successful designs from milliwatts to megavolt-amps and from IC/device design to prototype stages to finished end equipment. Applications ranging from industrial to automotive to full radiation hardened designs. "When I find a design or problem to be impossible, I go see Paul, he figures it out" expounds one of his 20-year peers in the industry.

Do you have any comments on this column? If so, share them with the editor.

© 2018 How2Power. All rights reserved. www.How2Power.com